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Analysis of Design Parameters that Affect the Performance of Multi-site Vertical Probe Cards

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Overview

- Motivation
- Objective
- PDN Impedance
- PDN Elements & Simulation Results
- Summary & Conclusion

Motivation

- **Customer**
  - Power plane requirements for high pin count multi-DUT probe cards (Mobile Processor, Memory, …etc.) specifically,
  - DC Resistance
    - Why is it important? How does it effect performance?

      Related directly to voltage drop

      Sensitive to Site to site design variation.
  - Input Impedance
    - Why is it important? How does it effect performance?

      Directly related to noise (SSN and crosstalk)

      Parameters are inductance and decoupling cap value & location.

      Vary from site to site due to sites orientations

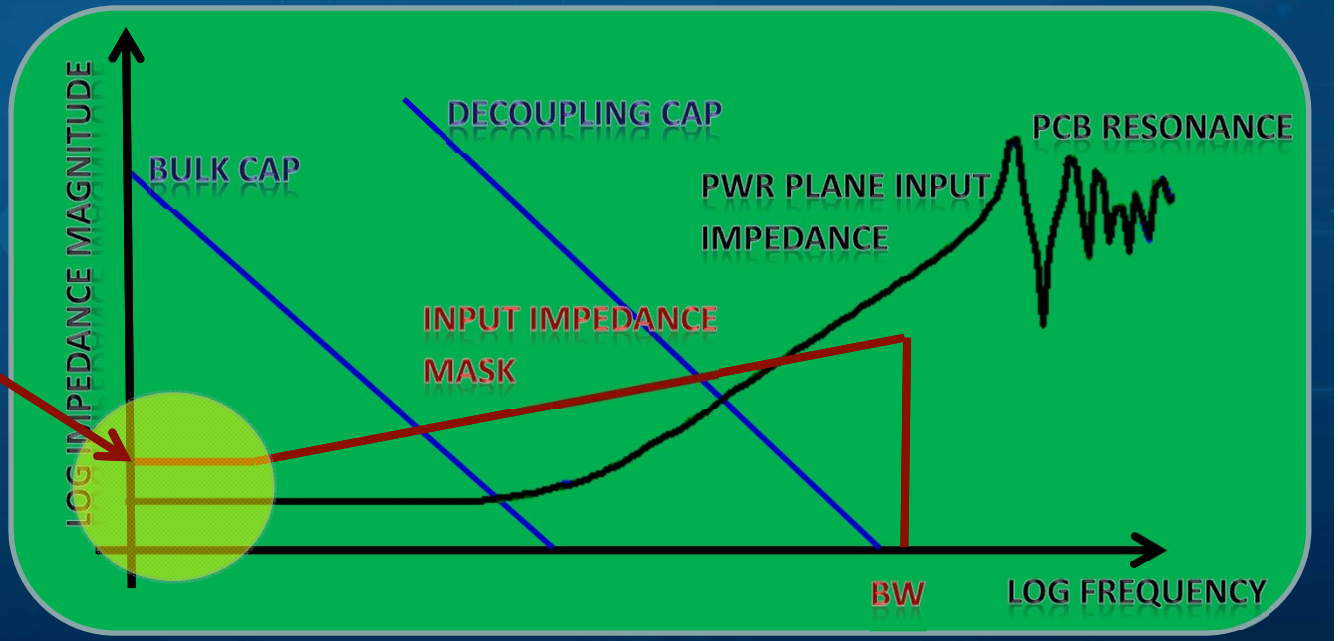
Objective

- **Study Interconnect parameters that contribute to:**
  - DC path resistance
  - Input impedance
- **Find optimum design that minimizes DC path resistance & input impedance**
  - Design elements & variables
- **Tools Used**
  - ANSYS HFSS
  - ANSYS SIwave
  - Agilent ADS

PDN impedance calculation

- **Maximum allowable voltage drop**
  - Minimum DUT operating voltage
  - Maximum supply current
  - Target path resistance

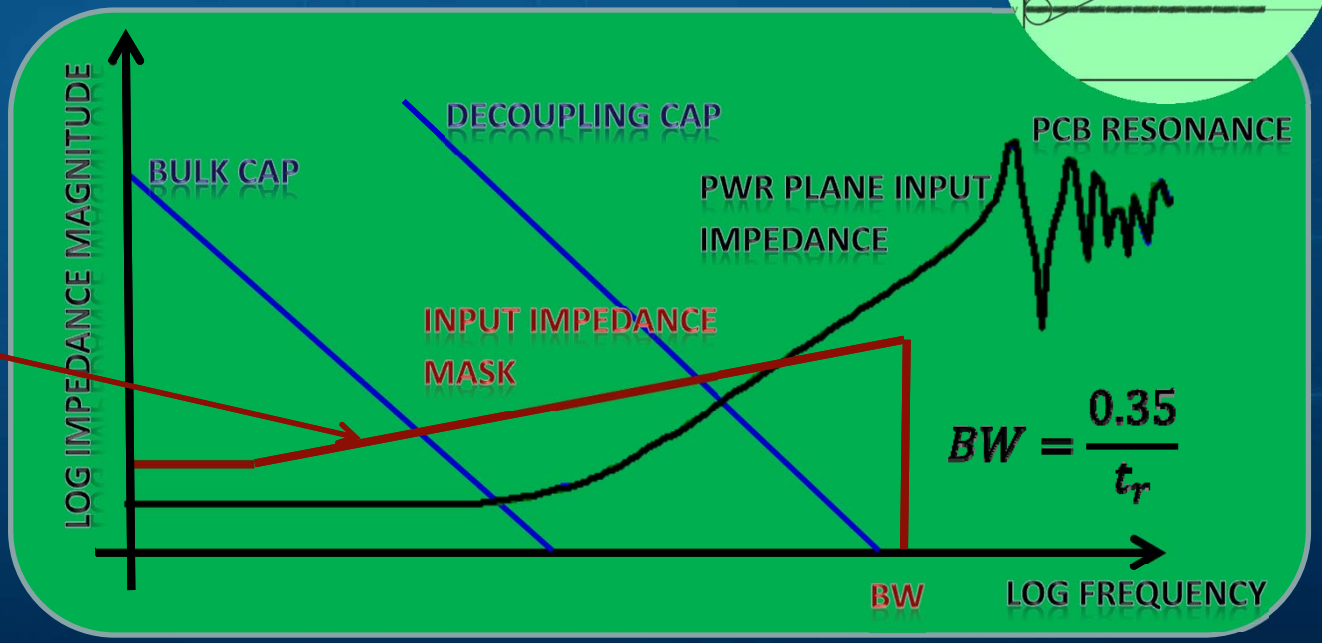
$$R = \frac{V_{Supply} - V_{min}}{I_{max}}$$



PDN impedance calculation

- **Maximum noise allowed**
  - Maximum voltage ripple
  - Transient current
  - Bandwidth

$$Z_{PDN} \leq Z_{target} = \frac{V_{ripple}}{I_{transient}}$$

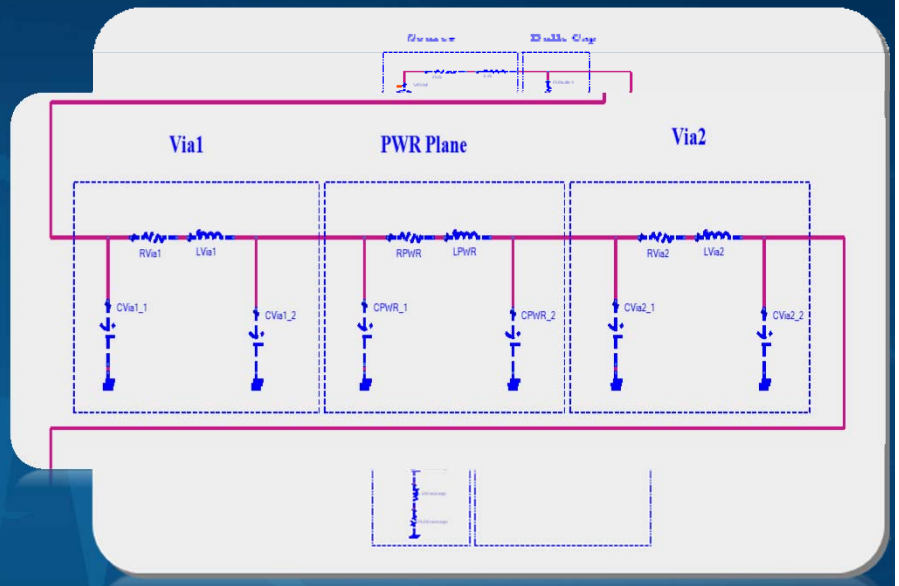


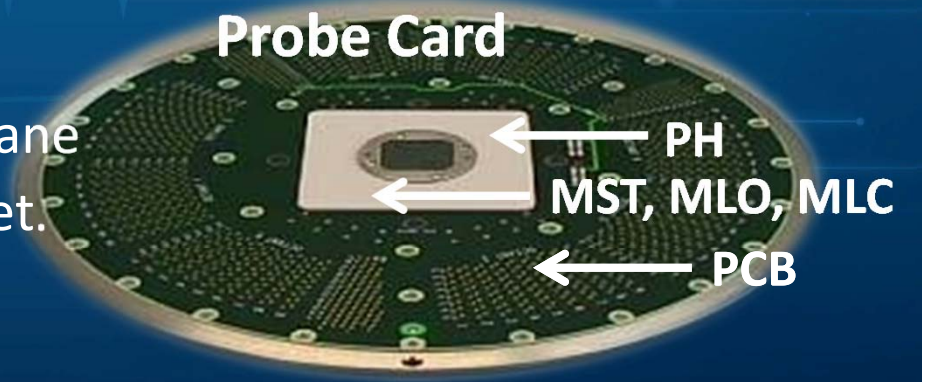
PDN impedance calculation

- **Faster current delivery**
  - Decoupling caps location
  - Minimize trace inductance
- **Low resistance & inductance for return path**
  - Loop resistance
  - Loop inductance
  - GND coupling

PDN Elements

- **Source (tester)**
- **Bulk & Decoupling Caps**
- **Inductors & Ferrite Beads (LPF)**
- **PCB Via**
  - Via diameter, length & plating
  - Via location to GND via
  - No of via connection
- **PCB PWR Plane**
  - Size (thickness, length, width)
  - Location of PWR plane wrt GND plane
  - No of PWR planes for each PWR net.
  - PWR Plane shape

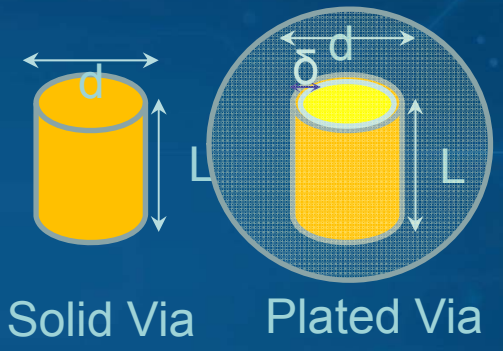


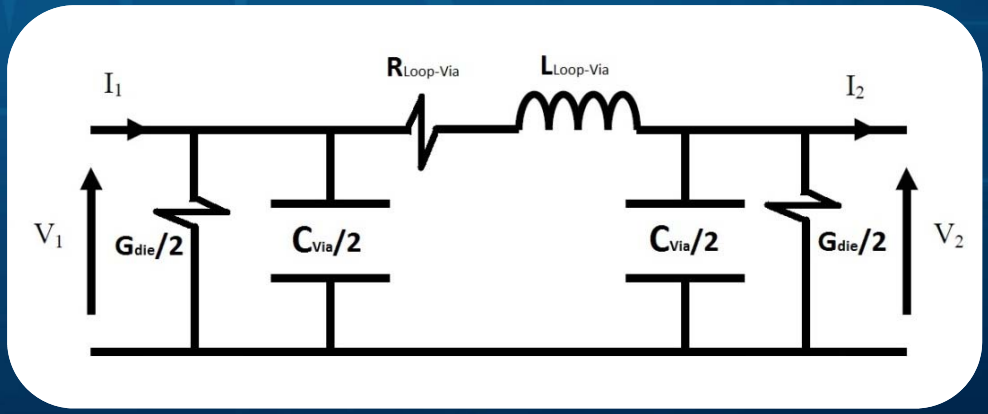


PDN Elements

Via Equivalent Circuit

- **Low Frequency Model**
  - Length
  - Plating
  - Distance from GND via
  - Number of connections
- **High Frequency Model**
  - Skin effect
  - Proximity effect



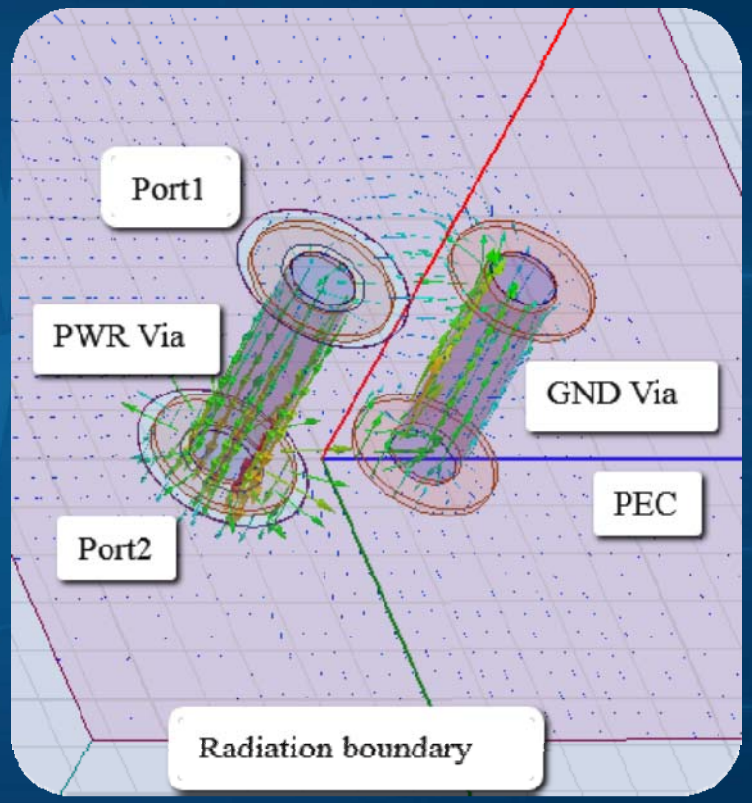


PDN Simulation Results

Via Simulation

Case1

- Single PWR via & GND via with the following conditions:
  - Constant via length 40 mils
  - Constant via plating thickness 1mil (Cu)
  - Via diameter (=6,8,10 and 12mils)
  - Via spacing =3 x via diameter
  - Solder pad diameter or keep-out = 2x via diameter



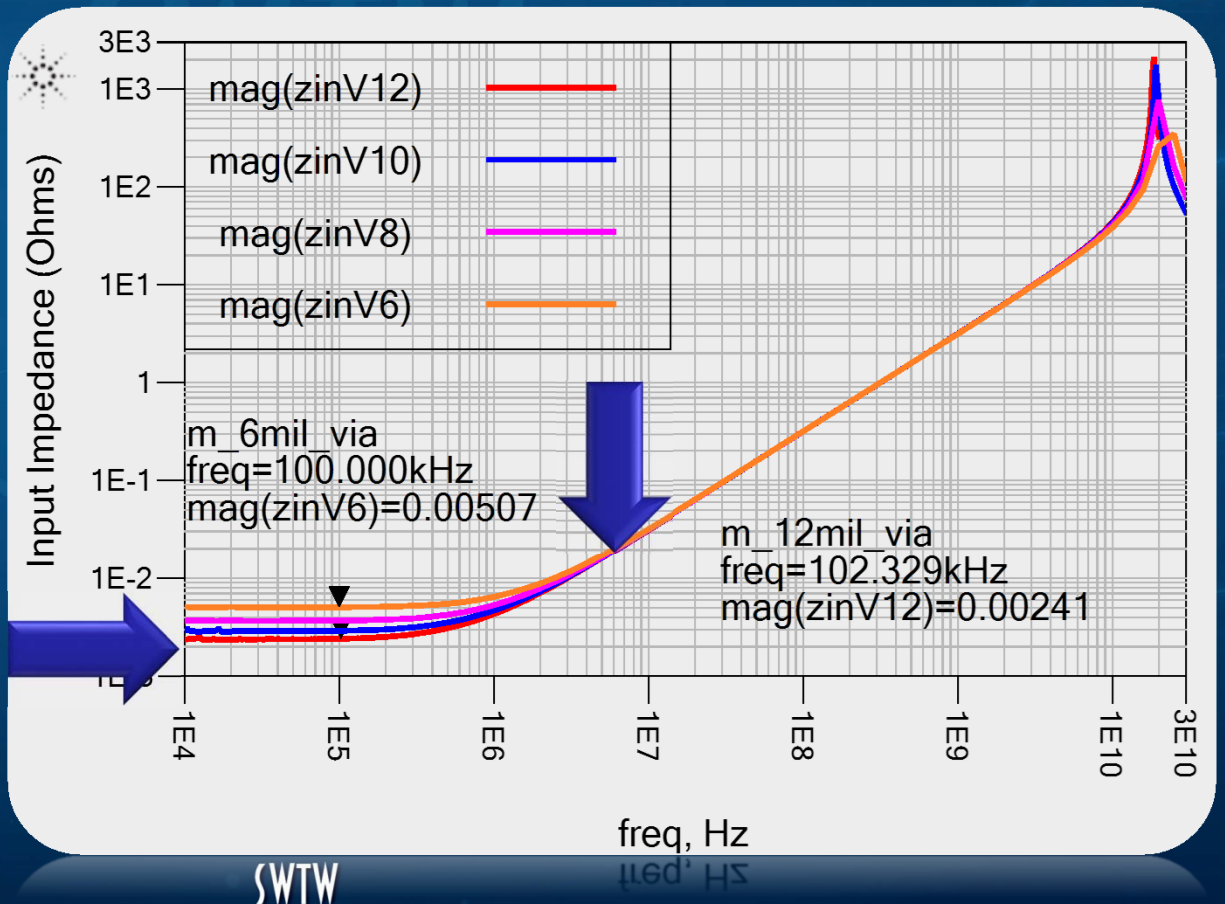
PDN Elements & simulation Results

Via Simulation

Case1

No Change in Inductance or Capacitance

Resistance Increase



PDN Simulation Results

Via Simulation

- **How much path resistance changed?**
  - $R = \frac{\rho l}{A} \quad A = 2\pi\delta r + \pi\delta^2$ $\qquad \frac{R_1}{R_2} = \frac{r_2}{r_1}$

R is inversely proportional with via diameter

- **How much inductance changed?**
  - $L_{Loop} = 2L_{self} - 2M$ $\qquad L_{Loop} = \frac{\mu\, l}{\pi}(ln(S/r) - 1/4)$

If (S/r) is constant, loop inductance and coupling capacitance stay constant

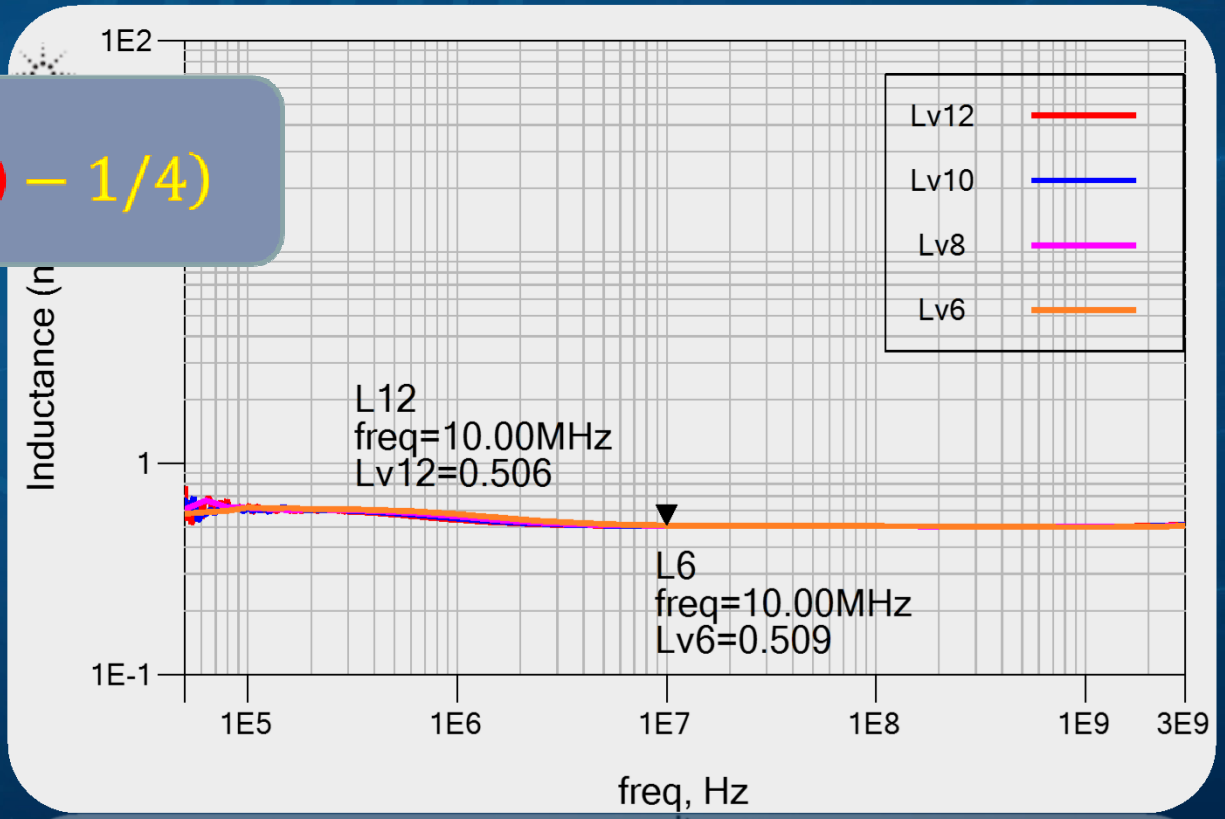
PDN Simulation Results

Via Simulation

Case1: Single PWR via & Single GND via

$$L_{Loop} = \frac{\mu\, l}{\pi}(ln(S/r) - 1/4)$$

No Change in loop Inductance



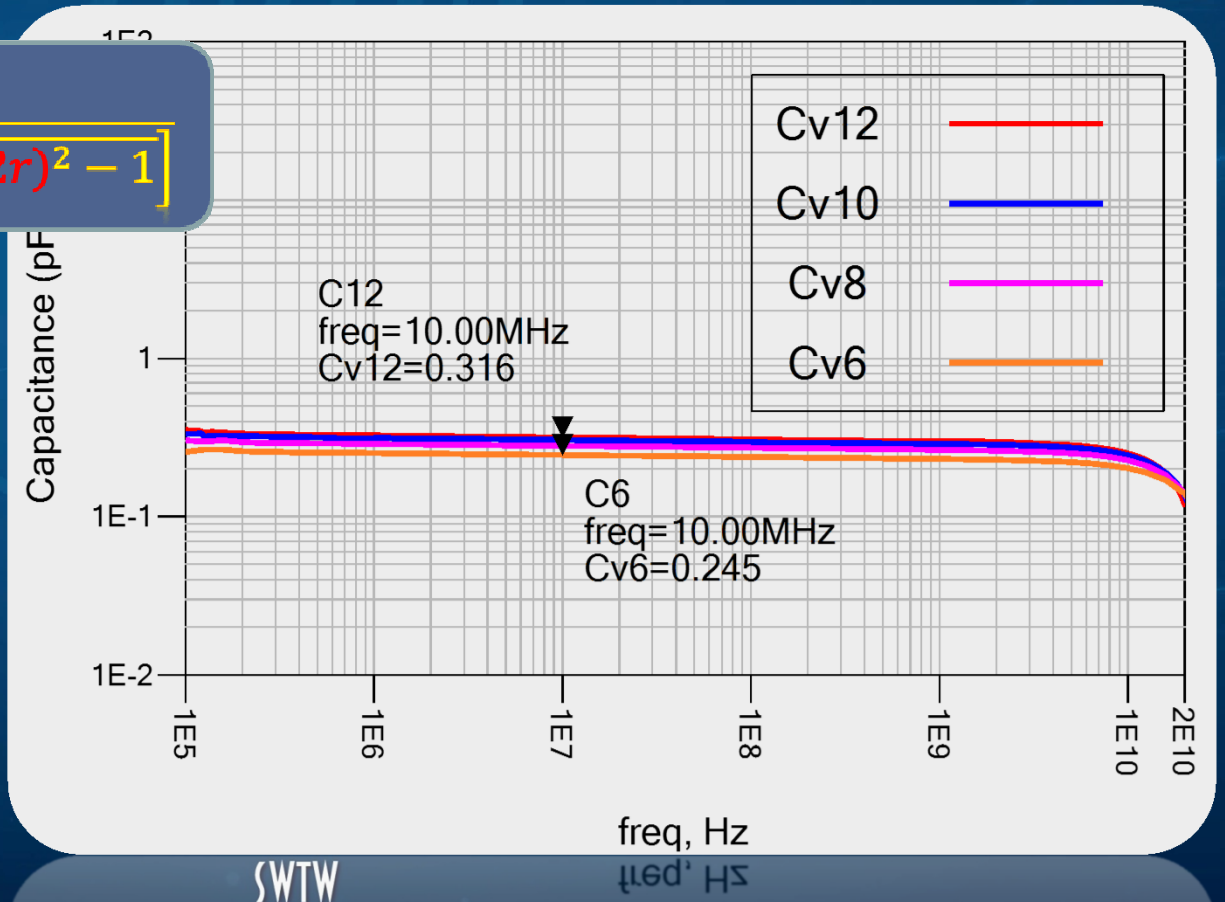
PDN Simulation Results

Via Simulation

Case1: Single PWR via & Single GND via

$$C = \frac{\pi \epsilon l}{2} \frac{1}{\left[ln(S/2r) + \sqrt{(S/2r)^2 - 1} \right]}$$

No Change in Coupling Capacitance

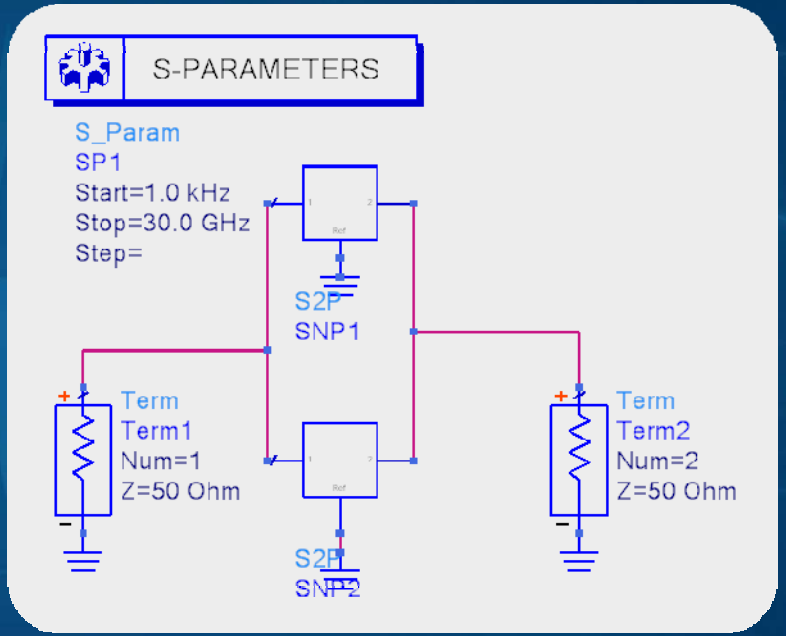


PDN Simulation Results

Via Simulation

Case2

- Two 6mil via Vs single 12mil via:
- Use a single via (PWR-GND) structure s-parameter obtained by ANSYS-HFSS
- Use Agilent ADS for complete system simulation
- Assumption: No coupling between the two via system

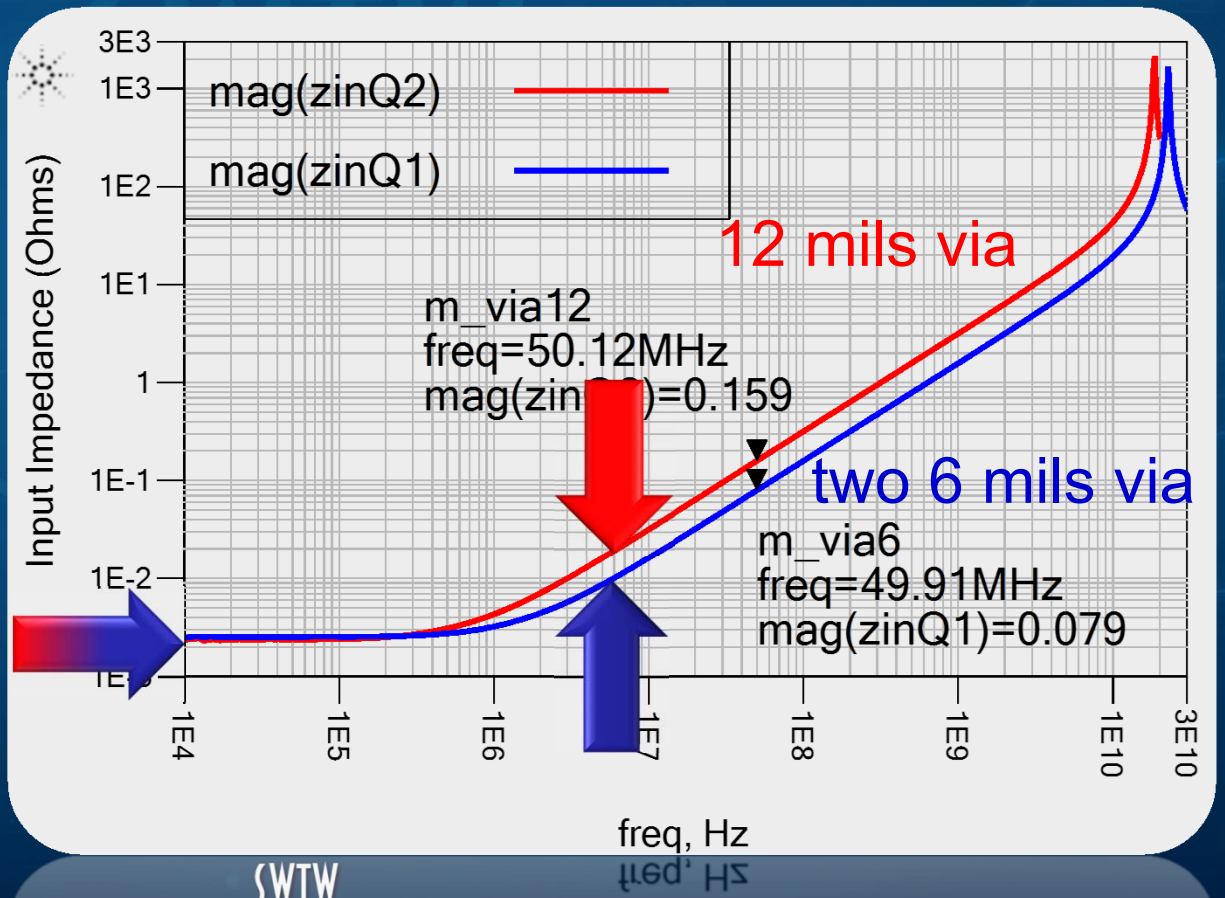


PDN Simulation Results

Via Simulation

Case2

~50% Impedance reduction with two 6 mils via



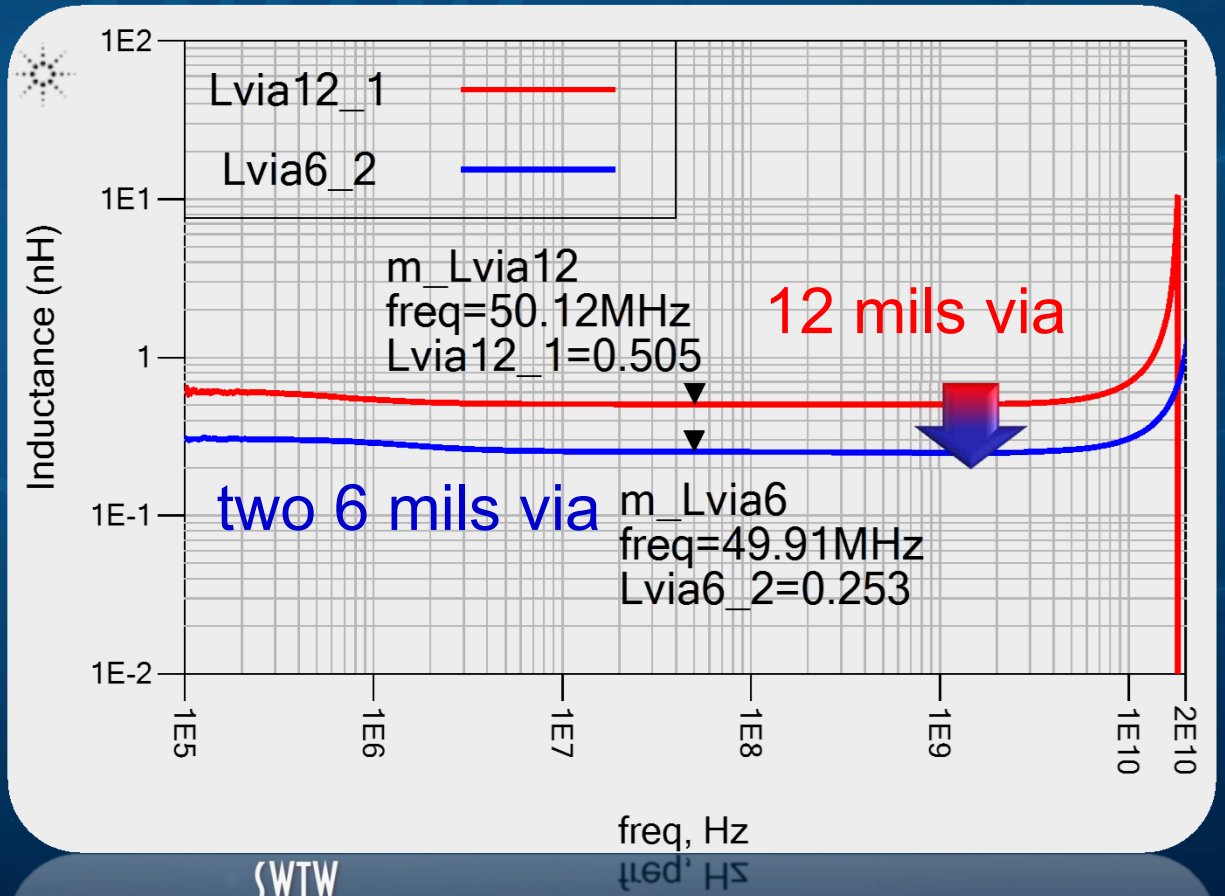
No Change in Resistance

PDN Simulation Results

Via Simulation

Case2

Inductance dropped by ~50%

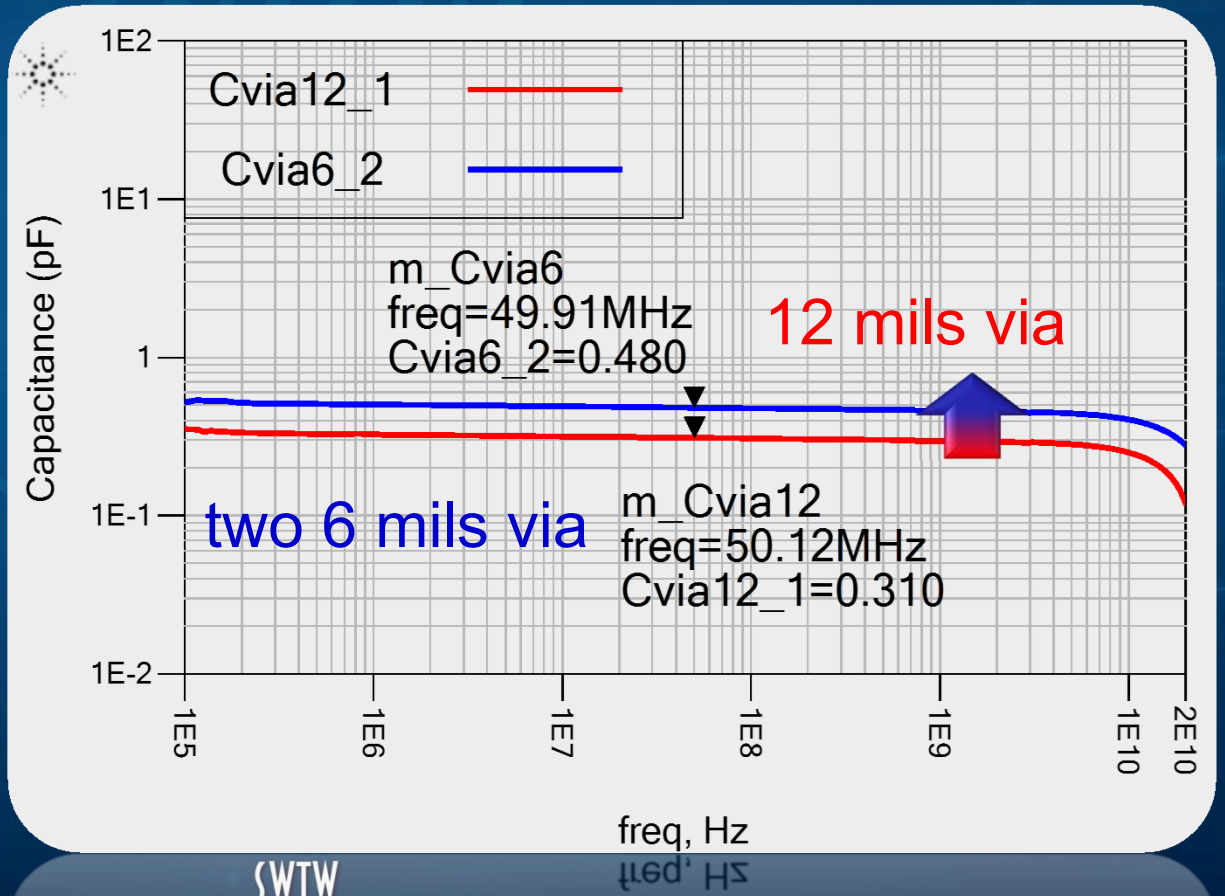


PDN Simulation Results

Via Simulation

Case2

Capacitance increased by 55%

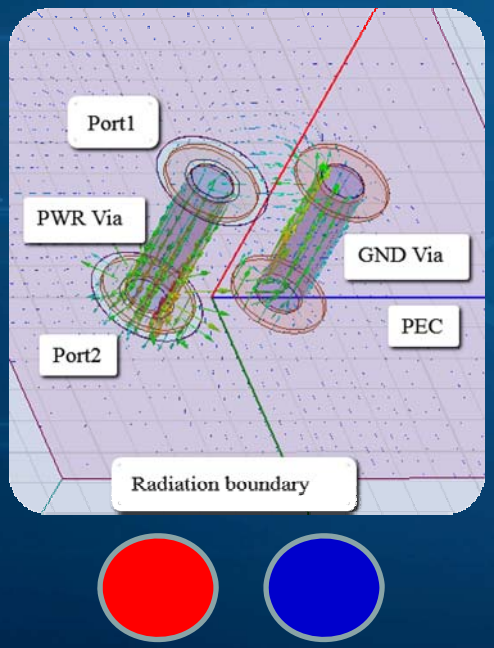


PDN Simulation Results

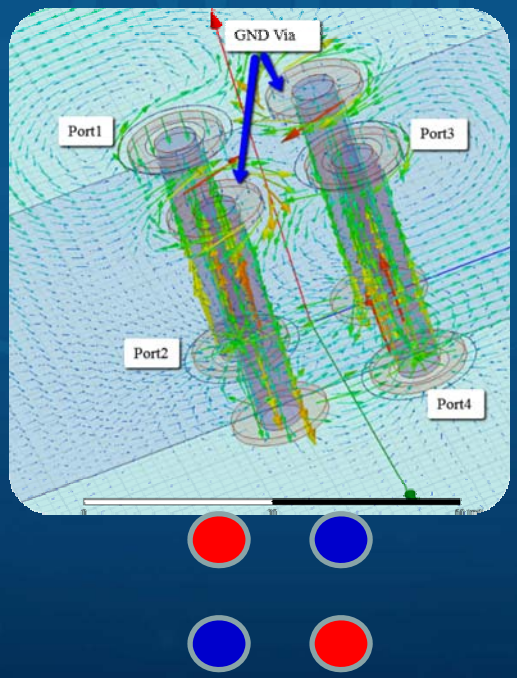
Via Simulation

- **Case3**
  - Comparison between two 6mil via vs single 12mil via using ANSYS HFSS

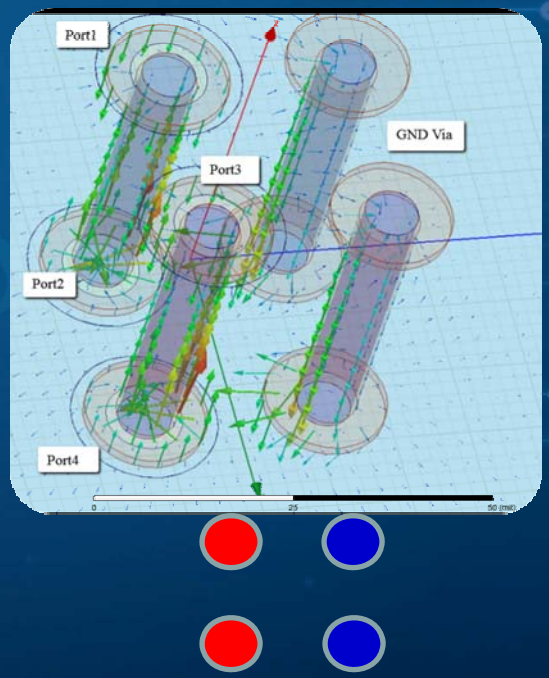
12 mil via



6 mil via Cross Configuration



6 mil via Inline Configuration



PDN Simulation Results

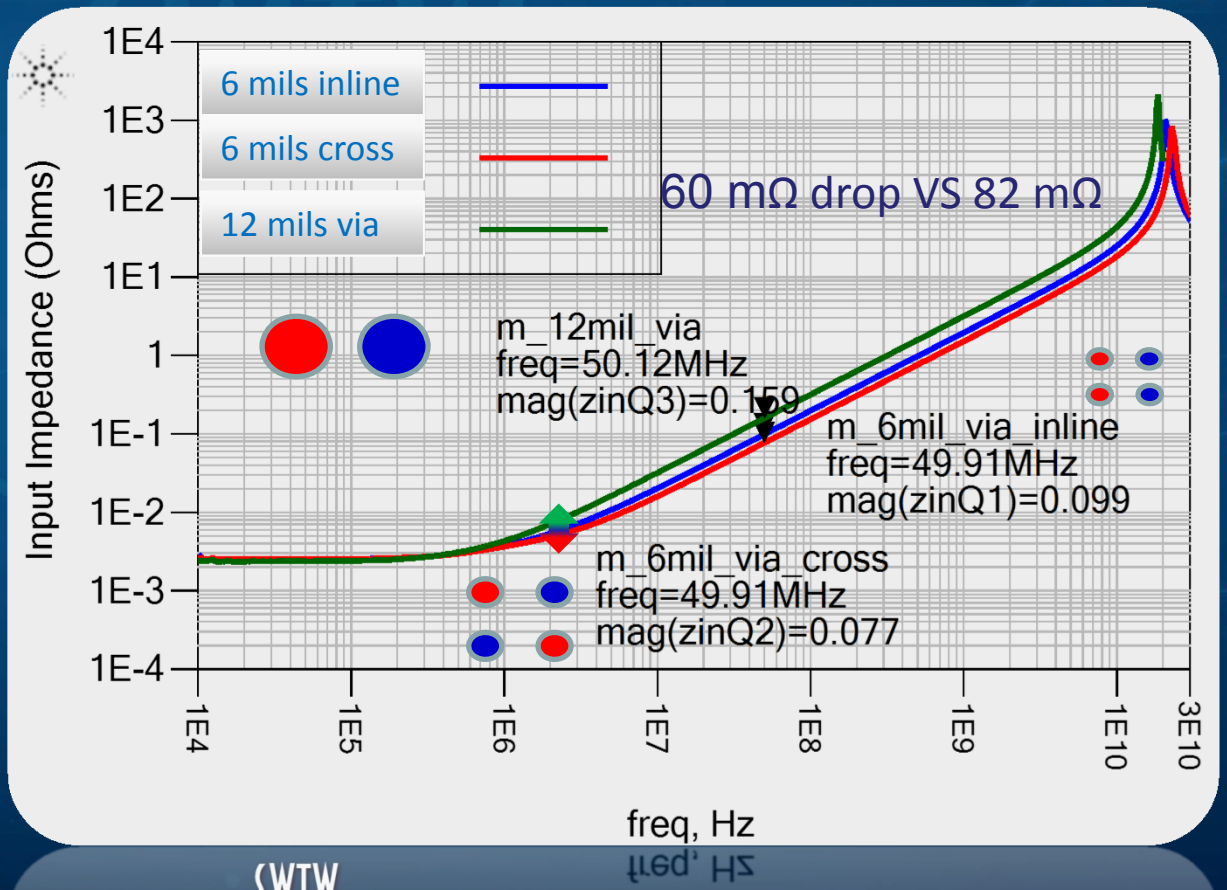
Via Simulation

Input Impedance for

1- two 6 mils via inline

2- two 6 mils via cross

3- single 12 mils via



PDN Simulation Results

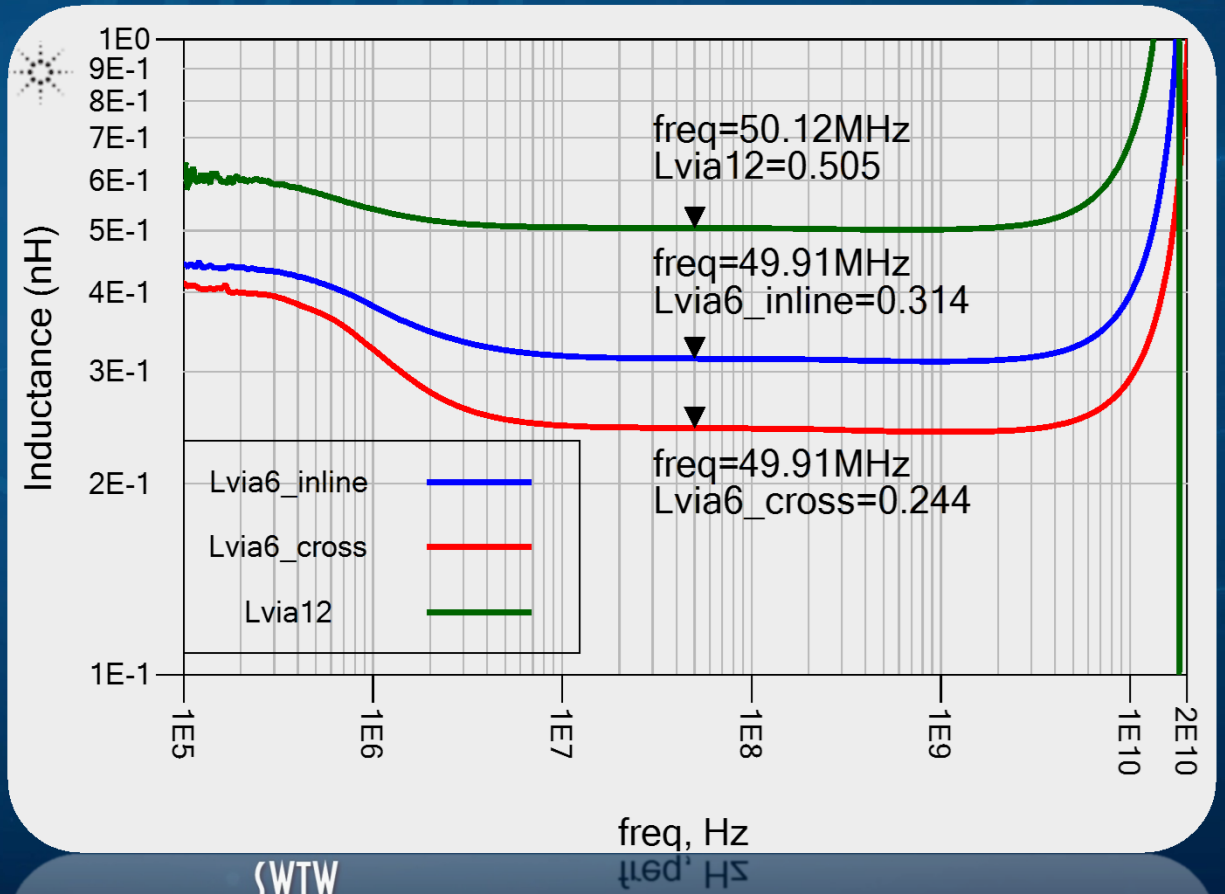
Via Simulation

Inductance for

1- two 6 mils via inline

2- two 6 mils via cross

3- single 12 mils via



PDN Simulation Results

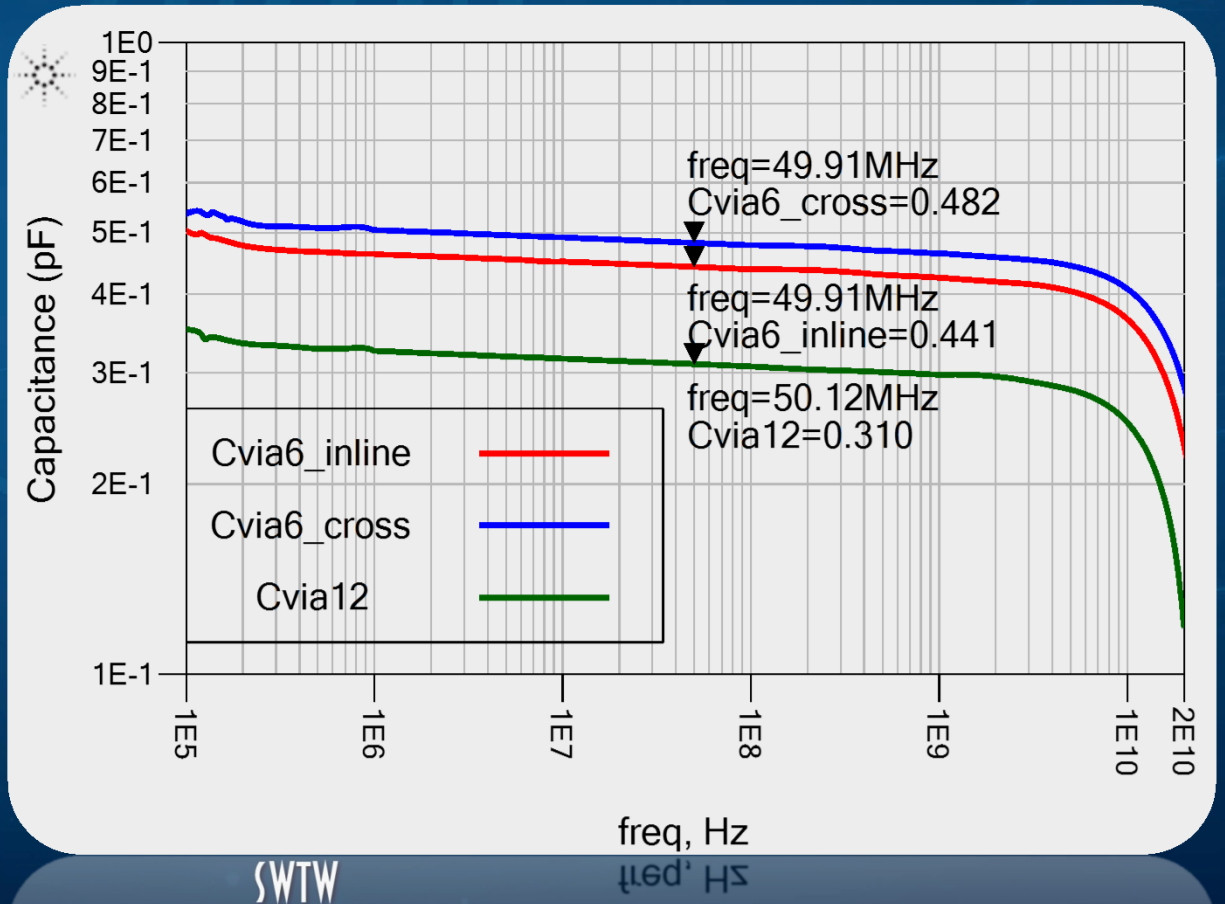
Via Simulation

Capacitance for

1- two 6 mils via inline

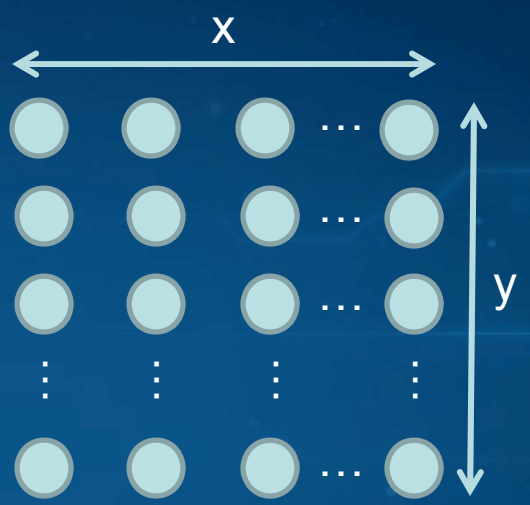
2- two 6 mils via cross

3- single 12 mils via



PDN Simulation Results

Real Estate Calculation



- **Area calculation**
  - Area required for N x N via array

$$A = (NS + 2r)^2$$

$$\left(\frac{r_2}{r_1}\right) = \frac{N_1 C + 1}{N_2 C + 1}$$

Where $C = S/2r$

- **Example**
  - Area required for 10 x 10 12mil via array with $c = 3$

$$A = 0.1384\ in$$

Number of 6 mil via for the same area is

$$N = 20$$

PDN Simulation Results

PWR Plane Simulation

- PWR Plane location investigation
- Via size impact on PWR Plane impedance
- Duplicating PWR plane impact on input impedance

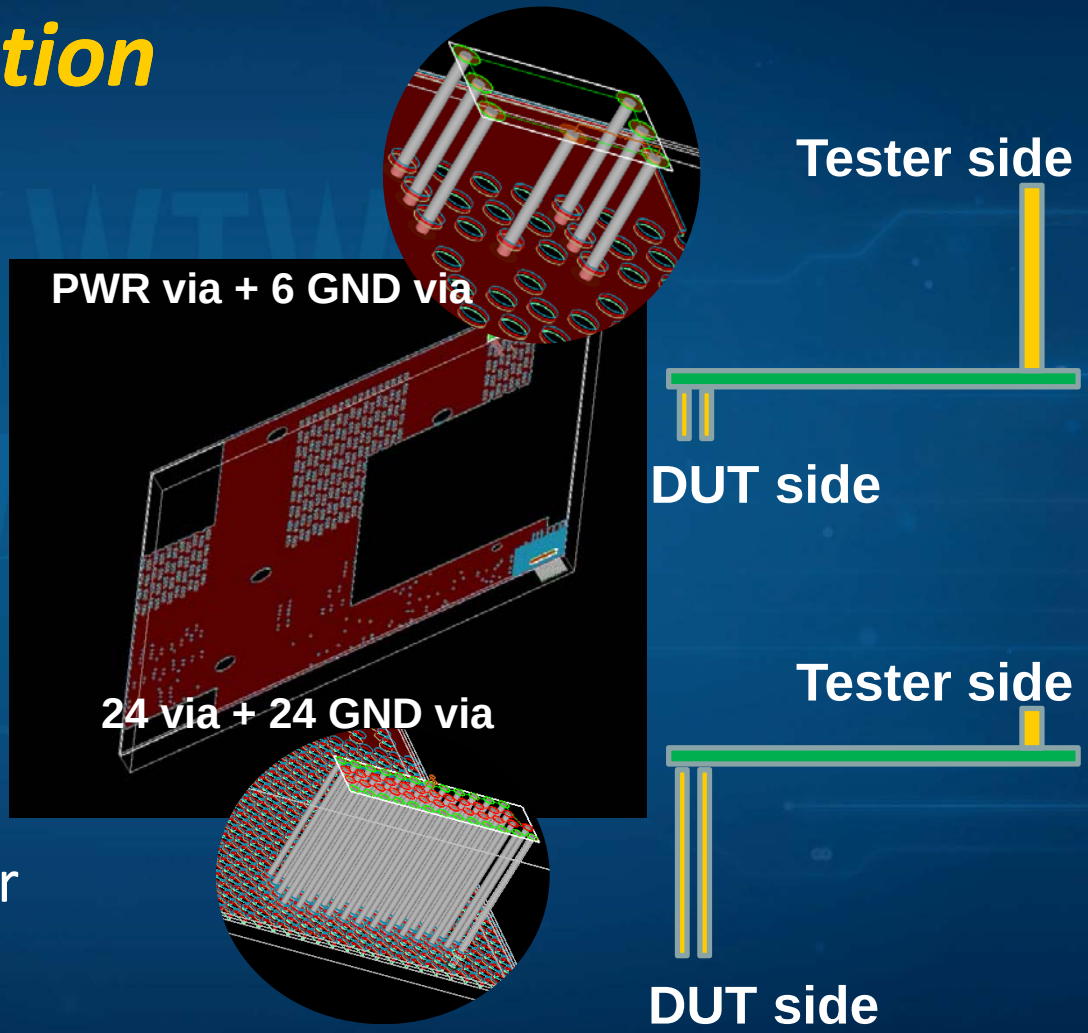
PDN Simulation Results

PWR Plane Simulation

PWR Plane Location

- 24 via connection from DUT to PWR Plane
- 1 via connection from Tester to PWR Plane

- **Case I**
  - PWR Plane close to DUT
- **Case II**
  - PWR Plane close to tester

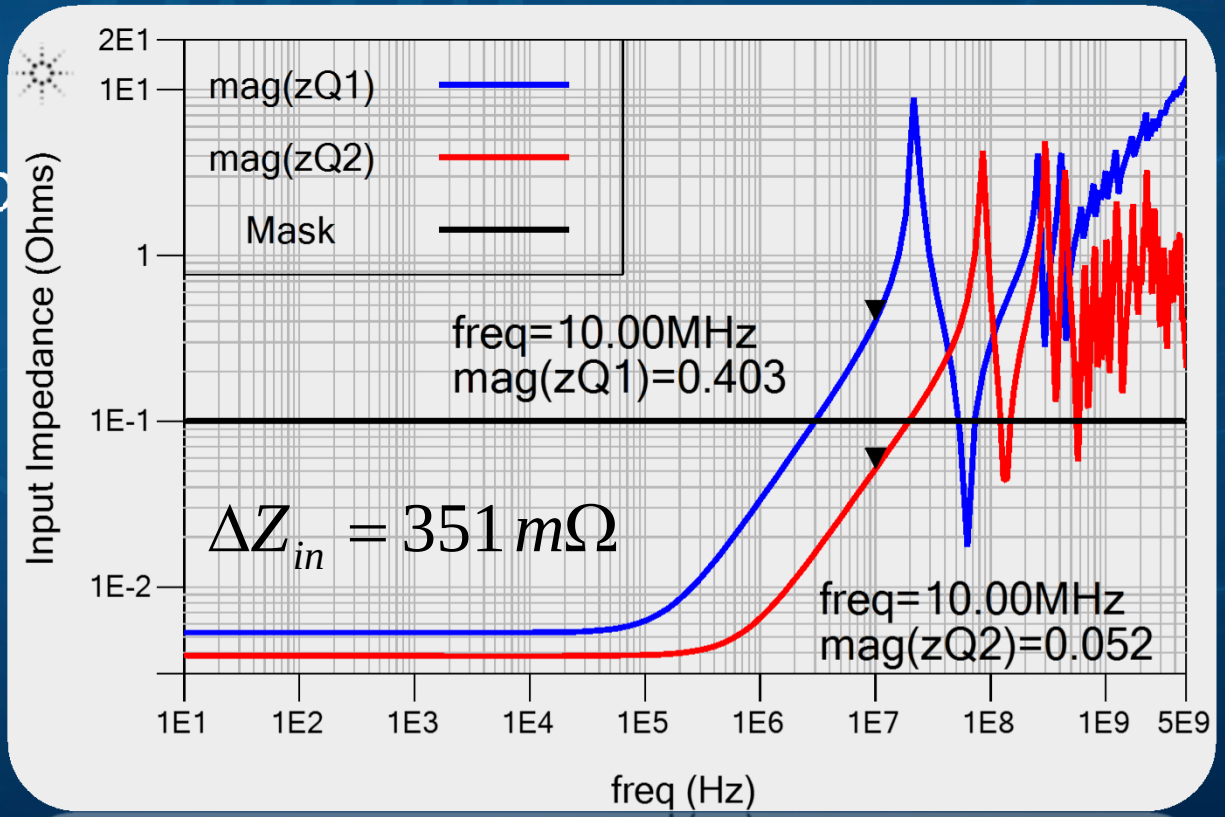


PDN Elements & Simulation Results

PWR Plane Simulation

PWR Plane Location

- **Case I**
  - PWR Plane close to D
- **Case II**
  - PWR Plane close to tester

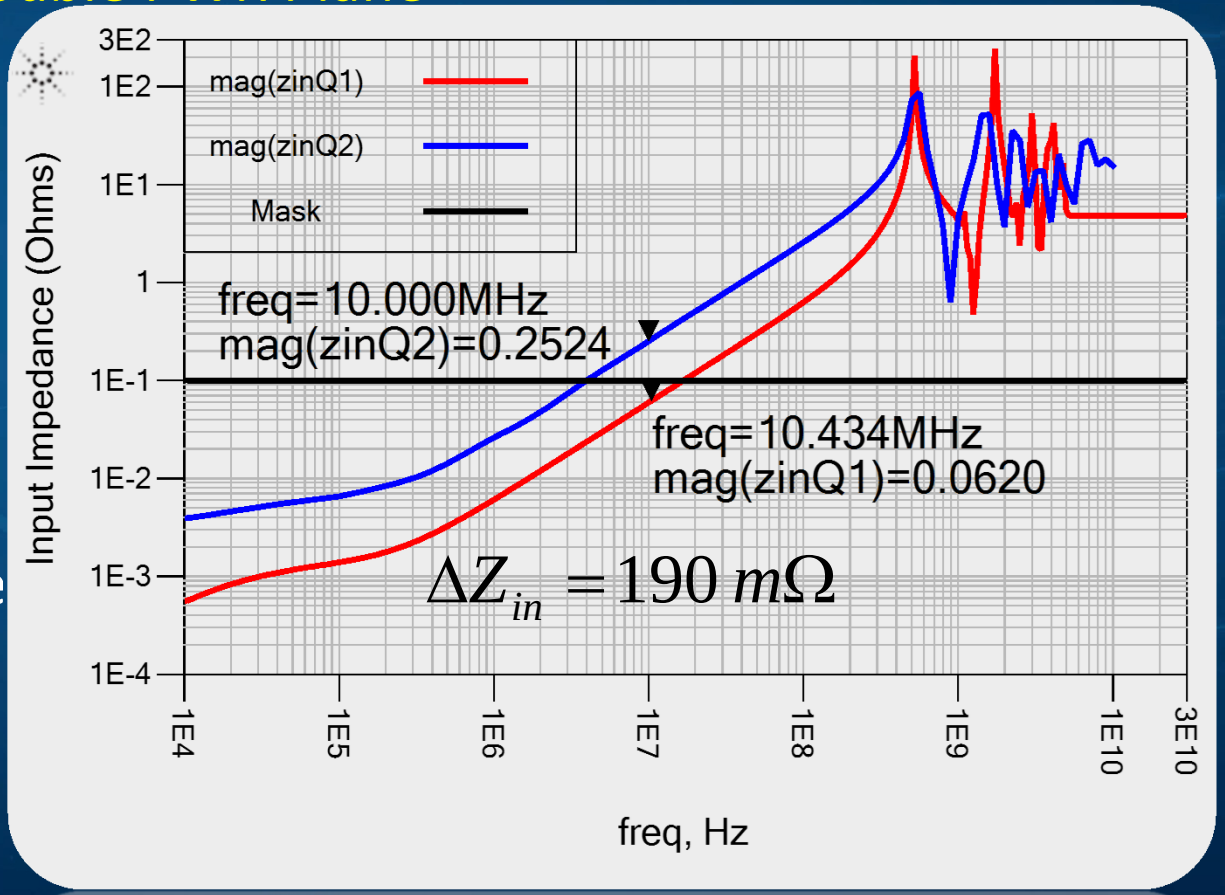


PDN Elements & Simulation Results

PWR Plane Simulation

Single PWR Plane Vs Double PWR Plane

- **Case I**
  - Single PWR plane
- **Case II**
  - Double PWR plane

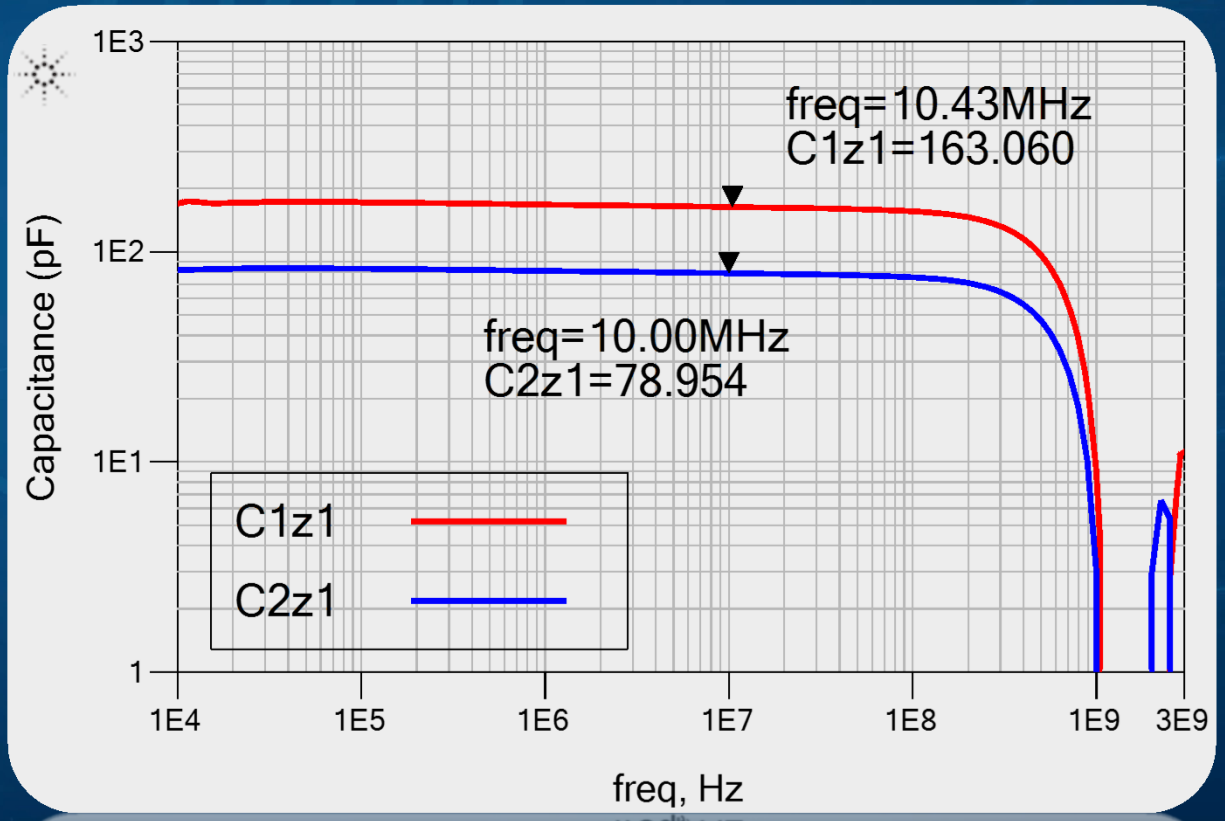


PDN Elements & simulation Results

PWR Plane Simulation

Single PWR Plane Vs Double PWR Plane

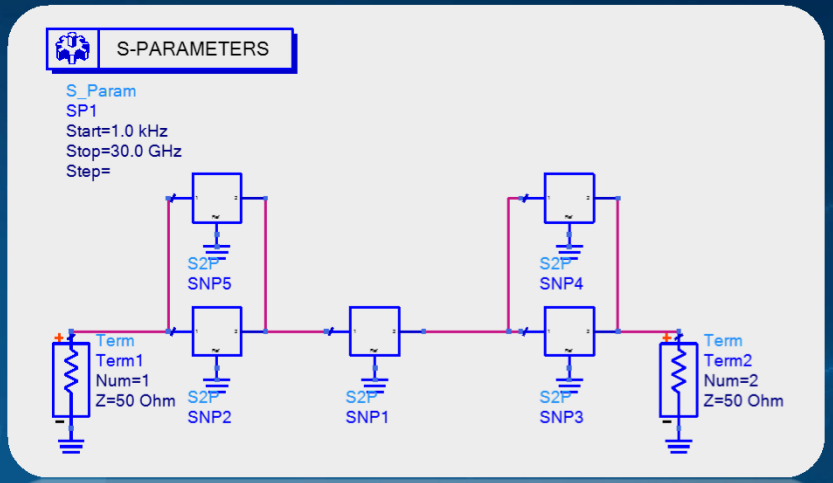
Inductance & Capacitance



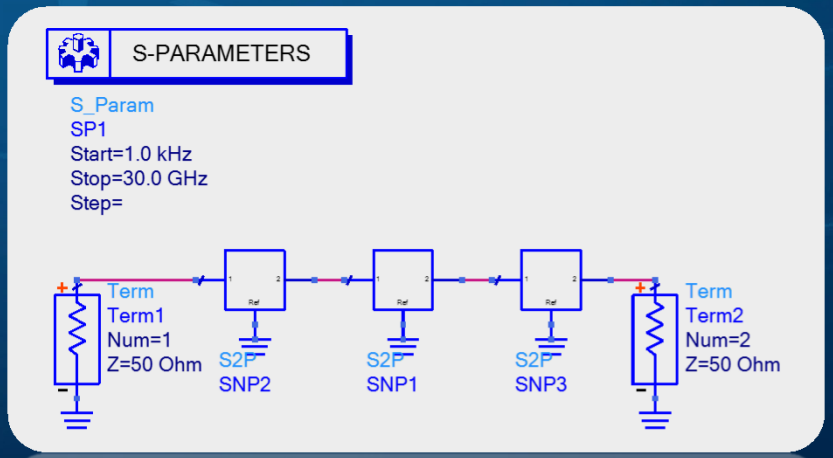
PDN Elements & Simulation Results

System Simulation

- **Case I**
  - Double 6 mil via with 6mil PWR plane



- **Case II**
  - 12 mil via with 12 mil PWR plane

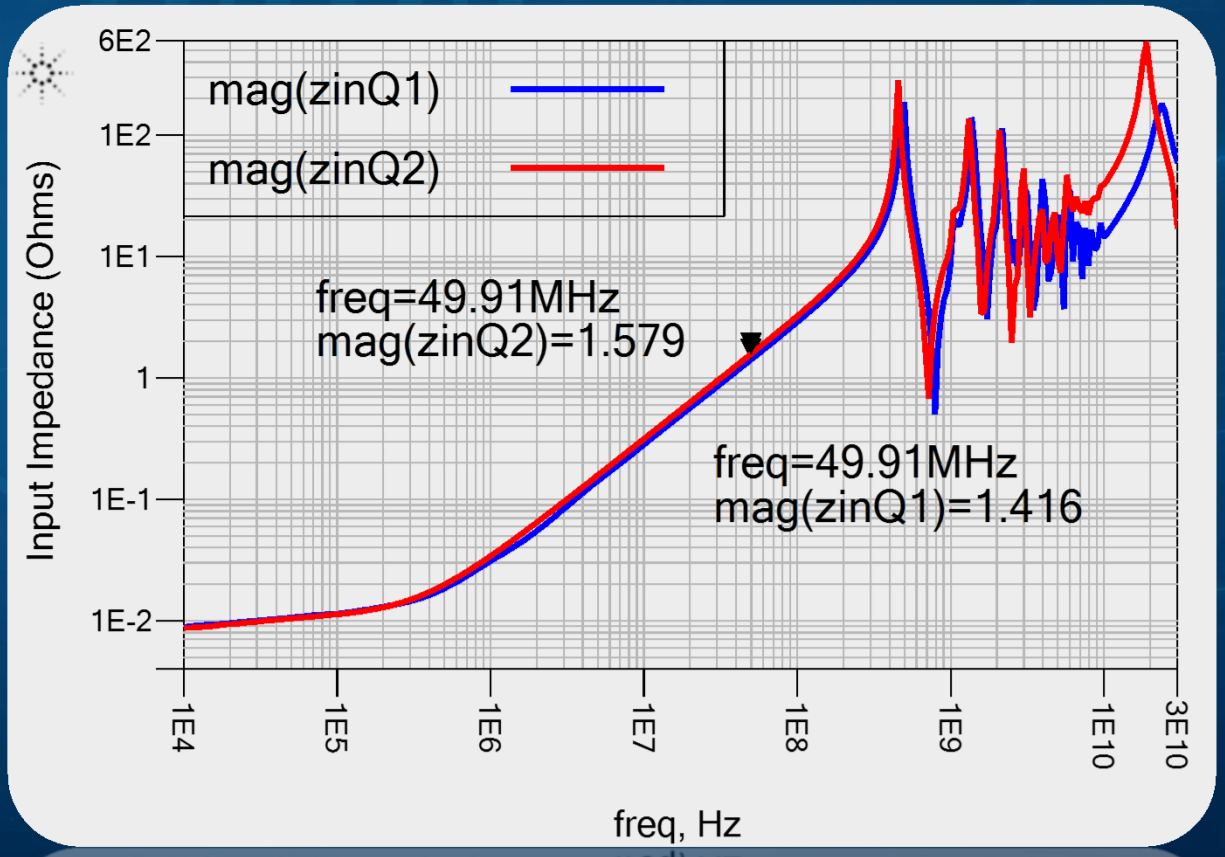


PDN Elements & Simulation Results

System Simulation

- **Case I**
  - Double 6 mil via with 6mil PWR plane
- **Case II**
  - 12 mil via with 12 mil PWR plane

ΔZ_{in}=163 mΩ

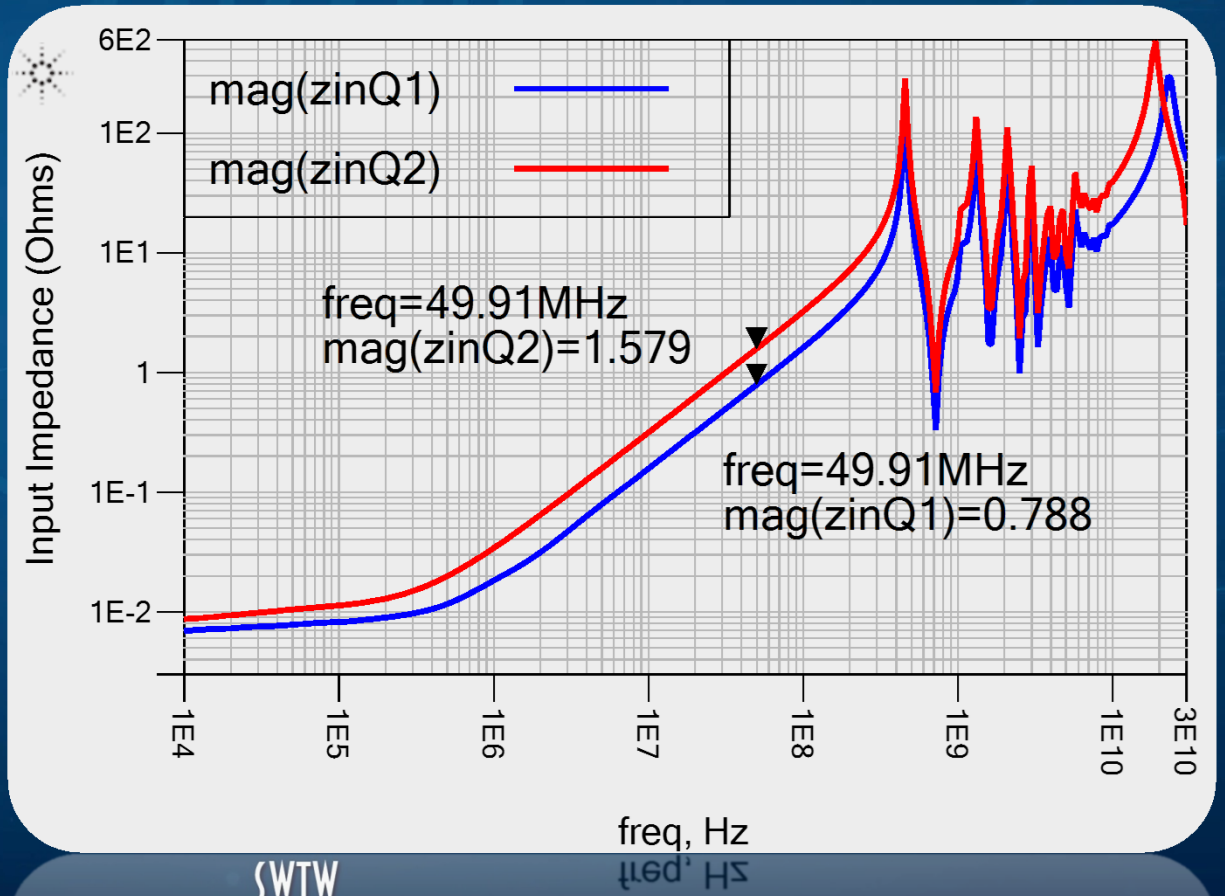


PDN Elements & Simulation Results

System Simulation

- **Case I**
  - Double 6 mil via with double 6mil PWR plane
- **Case II**
  - 12 mil via with 12 mil PWR plane

ΔZ_{in}=791 mΩ



Summary

- Two elements were investigated:
  - Via
  - PWR plane
- Different configurations were applied with different parameters:
  - Via diameter
  - Number of via connection
  - Via location & coupling effect
  - PWR plane location in the stack-up
  - Number of PWR plane

Conclusion

- **For optimum performance**
  - Keep S/r ratio of PCB via to keep loop inductance constant
  - Reduce PCB via diameter & increase number of via
  - Reduce the coupling between GND-GND & PWR-PWR
  - Reduce the input impedance by doubling PWR plane
  - Location of PWR plane should be based on minimizing the length of smaller number of via connections

Summary & Conclusion

- **Benefits**
  - Reducing Site-to-Site input impedance variation in multisite PC
  - Reducing Tester Program (TP) development time
  - Eliminating TP delay changes when ramping additional probe hardware
  - Produce High yield in multisite probing