SWTW

IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

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3D TSV Cu Pillar Probing Challenges & Experience

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SPIL

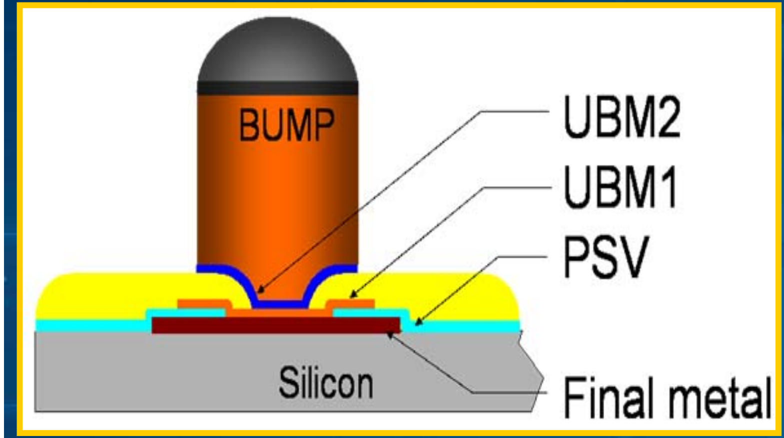
The Challenges

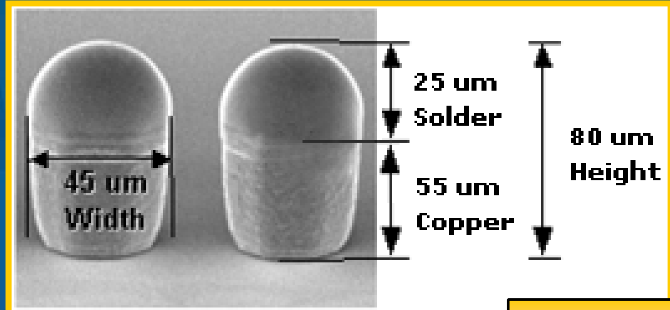
Cu Pillar Bump Reliability Shear Test

Each Assembly/Packaging house has done many DOEs & optimized their bump geometry, UBM, PI thickness to optimize reliability.

Reliability Test…

Condition	Pre-cond (L3 260 oC)	TCT (-65 ~ 150 oC)	HAST (130 oC / 85% RH)	HTSL (150 oC)
Read Point	3X Reflow	1000 Cycles	168 hrs	1000 hrs
Judge Method	SAT : O/S test	SAT : O/S test	SAT : O/S test	O/S test
Results	Pass.	Pass.	Pass.	Pass.





80 um Pitch Bump

Bump Structure

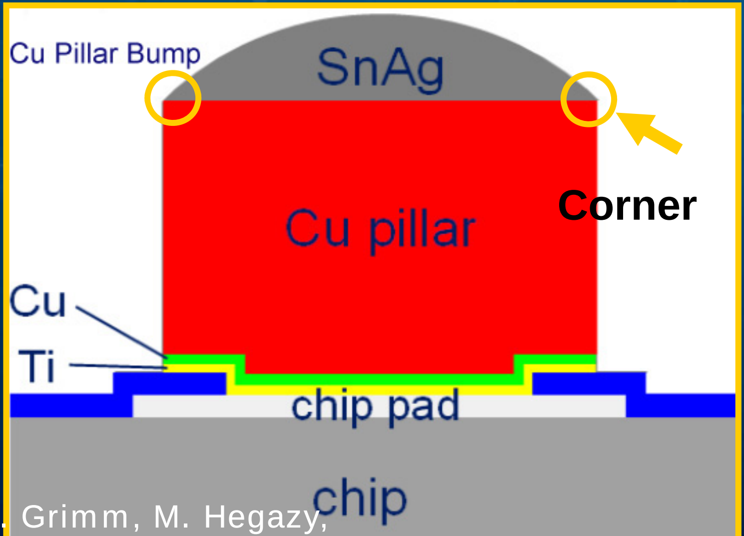


Fig 1. Stress Point after FC Attach Reflow

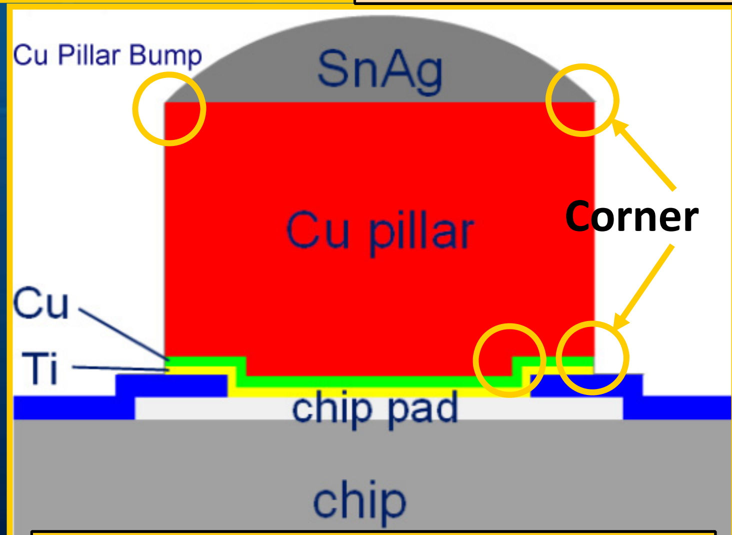


Fig 2. Stress Point After Assembly

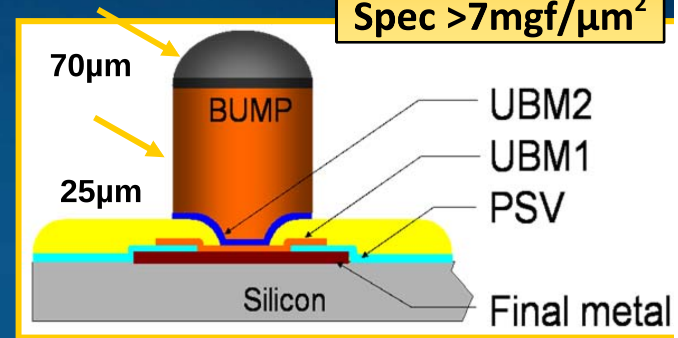
Cu-Pillar Bump Probing w/Staggered Probe

High Risk of Peeling & Fracture Failures

Bump shear tests were performed as per the JEDEC standards (JEDD22-B117).

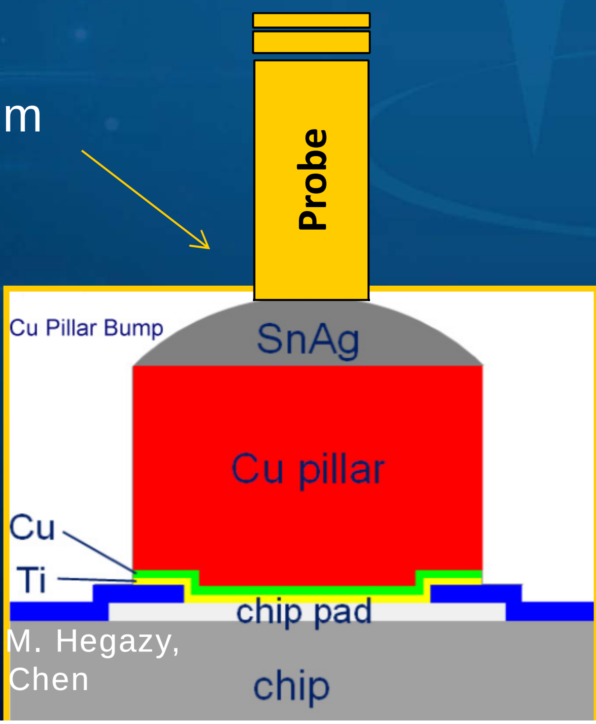
For Bump Shear Test, the wedge force at 20%~30% of Total Height of Pillar
Eg.TH= 80µm, shear test start at 25µm & the other to solder cap at 70µm.

Shear Force Test Spec >7mgf/µm^2

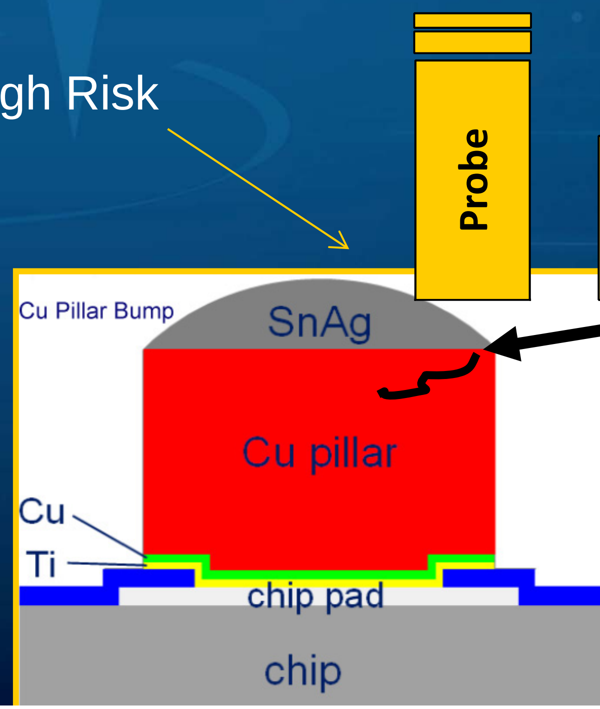


After the shear test was complete, the next step is for TCT Thermal Cycle for 1000 cycles, and results were observed to be passing. If the geometry is not optimized then fractures will show up on the stress points. Same concept was performed if probing on 2 different conditions…

Optimum



High Risk



shear force apply on stress point.

The SV-TCL Experience

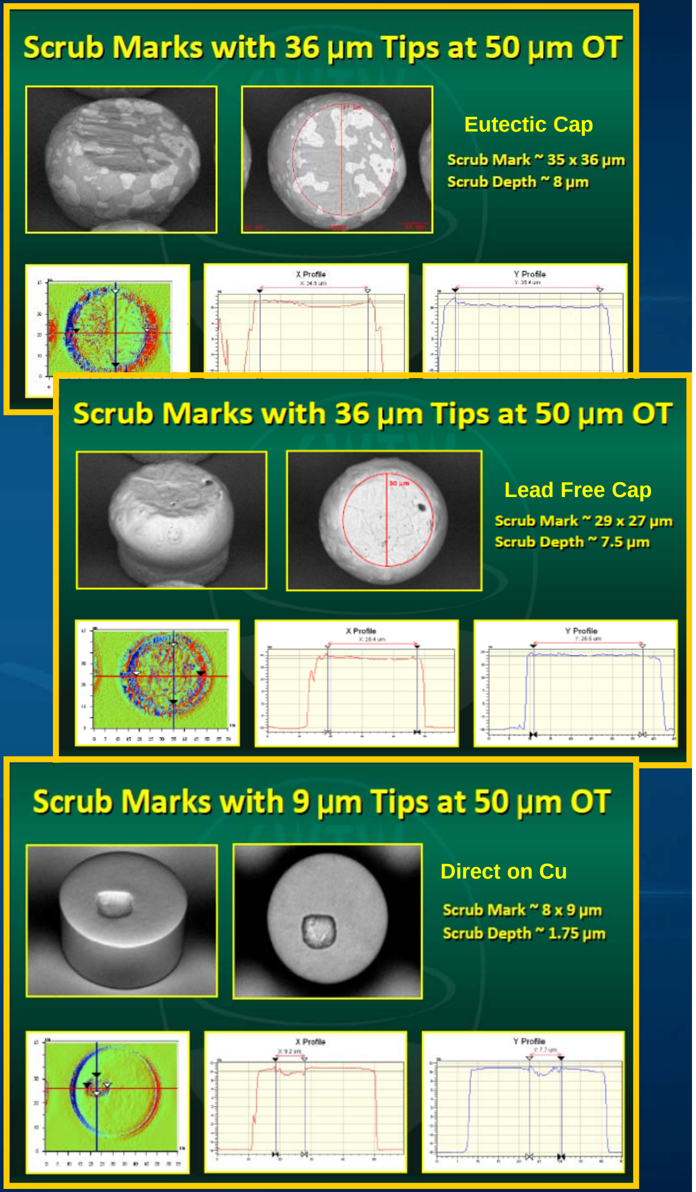
Recap of previous activities

- **Case #1 :2010 Copper Pillar & Bump Probing**
  - Engineering lab tests

- **Case #2: 2012 50µm Pitch Array w/LogicTouch™**
  - First trial on customer wafer

Case #1 - Copper Pillar & Bump Probing

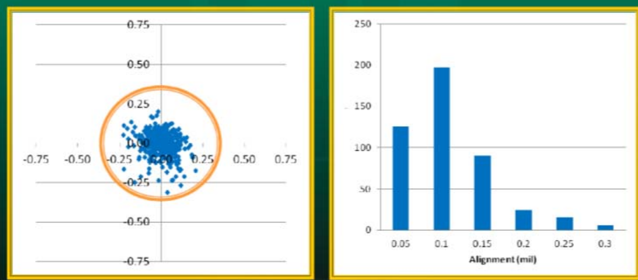
- **Internal Work to Study Contact Behavior of Cu-pillar Bumps at 60µm Pitch with Various Solder Cap Materials:**
  - Cu-pillar with Eutectic Solder Cap
  - Cu-pillar with Lead-free Solder Cap
  - Cu-pillars
- **Demonstrated**
  - Critical stress points and mechanical failure mechanisms of the probe card as well as the Cu Pillar
  - Critical parameters to achieve reliable and stable contact to different configurations
- **Presented at SWTW 2010**



Case #2 – 50µm Pitch Array w/LogicTouch™

Tip Alignment

- Probe Tip Alignment – 0.3 mil Radial



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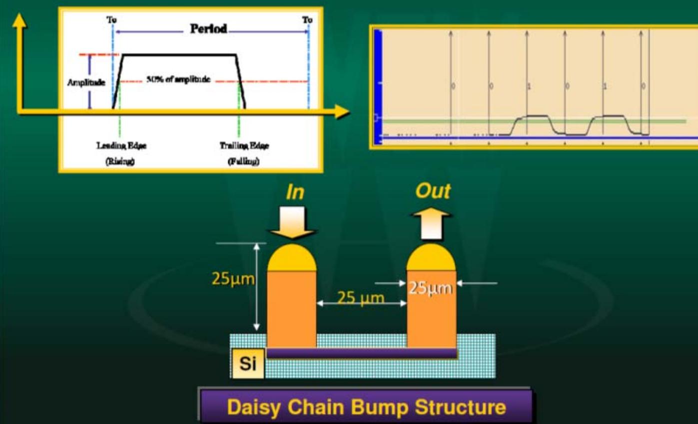
Test Method



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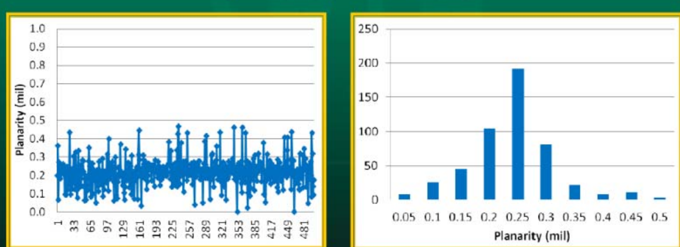
Planarity

- Probe Planarity < 0.5 mil (12µm)



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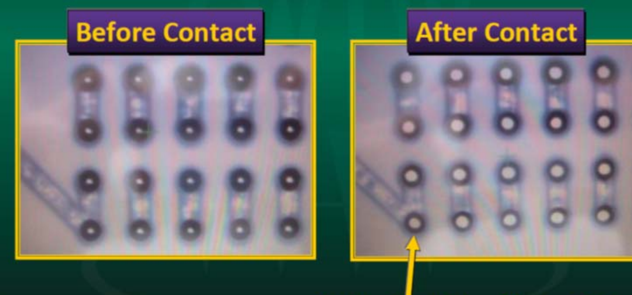
Co-presented with ASE at SWTW 2012

Probe Mark



**Over-Drive: 40µm*
 # probing: 2 TDs

Probe Mark Area Under 30%

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So where have we gone since SWTW 2010 and 2012 ?

Case#3 Production Reliability DOE

Huawei/Hi-Silicon/SPIL

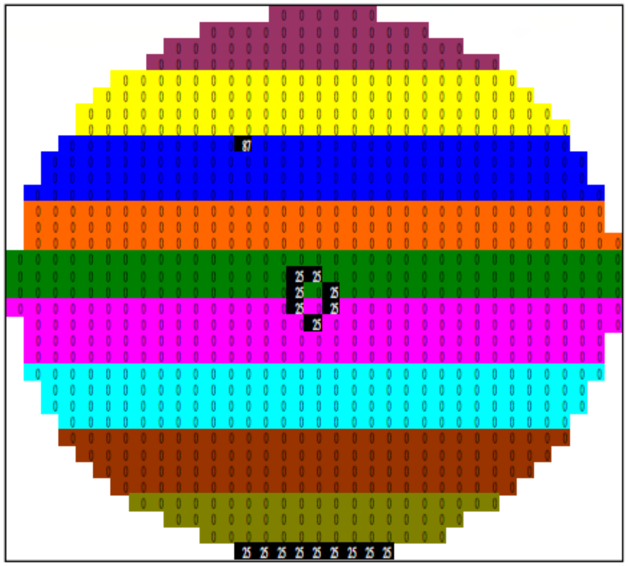
Cu Pillar + Solder Cap Probe Mark DOE

Mobile Chip Hi3620

DOE set up

Hi3620 Cu-Pillar Bump Probe Mark DOE Plan

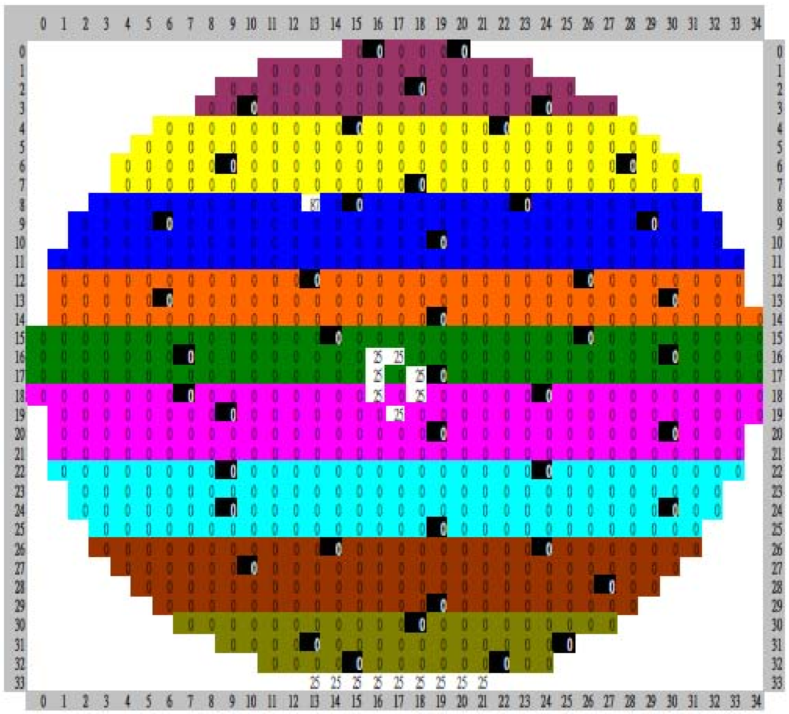
Area	Probe times	OD (um)	Test Time(sec)/Temp
A	4	50	6 sec/25℃
B		75	
C		100	
D	3	50	
E		75	
F		100	
G	2	50	
H		75	
I		100	



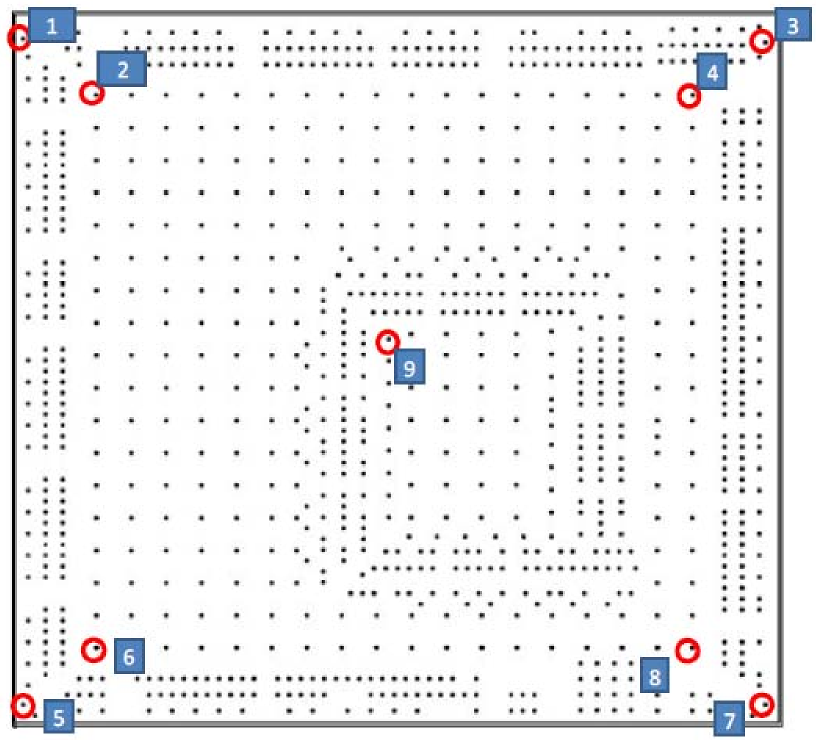
- MAX OD was suggested by vendor is 100um → Set OD 50,75,100
- Max TD of solid bump was 3 times. → Set 4 TD for the worst condition.
- Test conditions of Hi3620 was 5.17 sec/25℃. →Set to 6 sec./25℃

Probe Mark Size Sampling Plan

5 die per each area

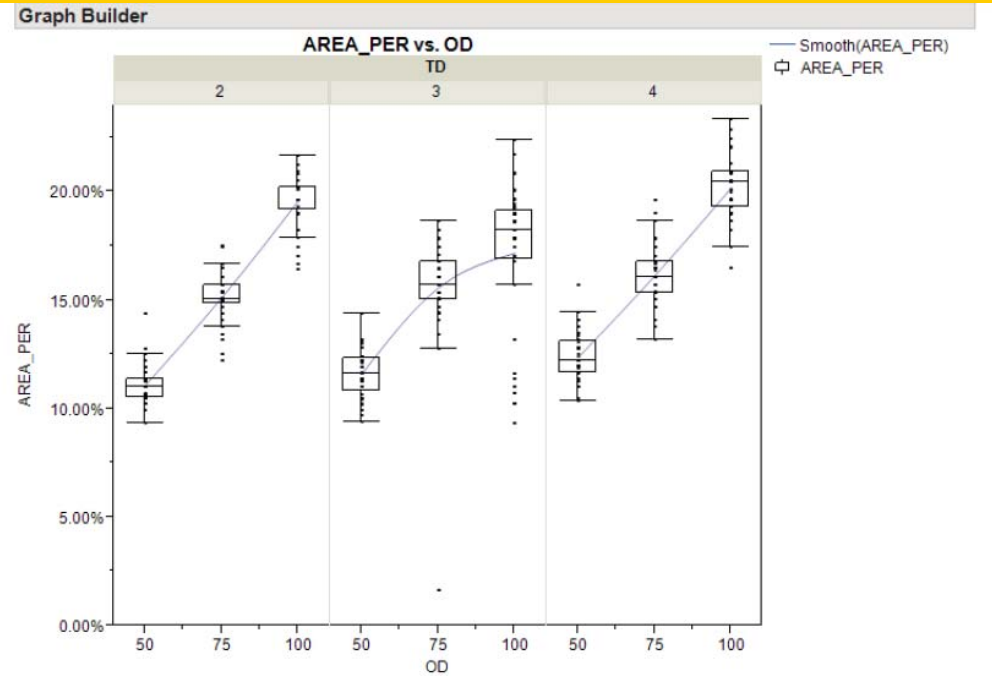


9 bump per each die



Probe Mark Size Analysis

Graph Builder

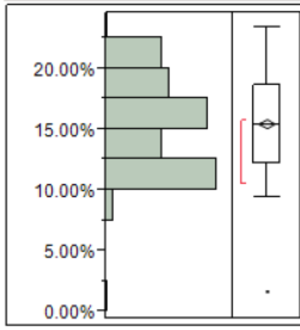


Probe mark related to OD strongly than TD

Probe mark range is 1.64%~23.32%

Distributions

AREA_PER

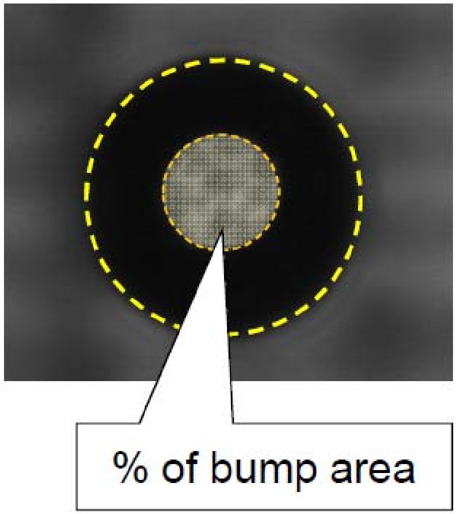


Quantiles

100.0%	maximum	23.32%
99.5%		22.85%
97.5%		21.20%
90.0%		20.24%
75.0%	quartile	18.62%
50.0%	median	15.36%
25.0%	quartile	12.21%
10.0%		10.98%
2.5%		10.21%
0.5%		9.34%
0.0%	minimum	1.64%

Summary Statistics

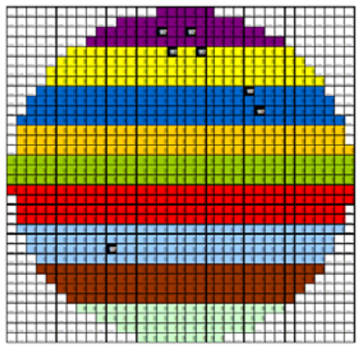
Mean	15.44%
Std Dev	3.56%
Std Err Mean	0.18%
Upper 95% Mean	15.79%
Lower 95% Mean	15.10%
N	40500.00%



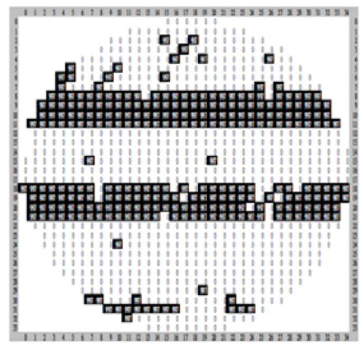
RVSI Inspection

Robotic vision bump inspection system

•No missing bump was found before DOE and after DOE



Before DOE



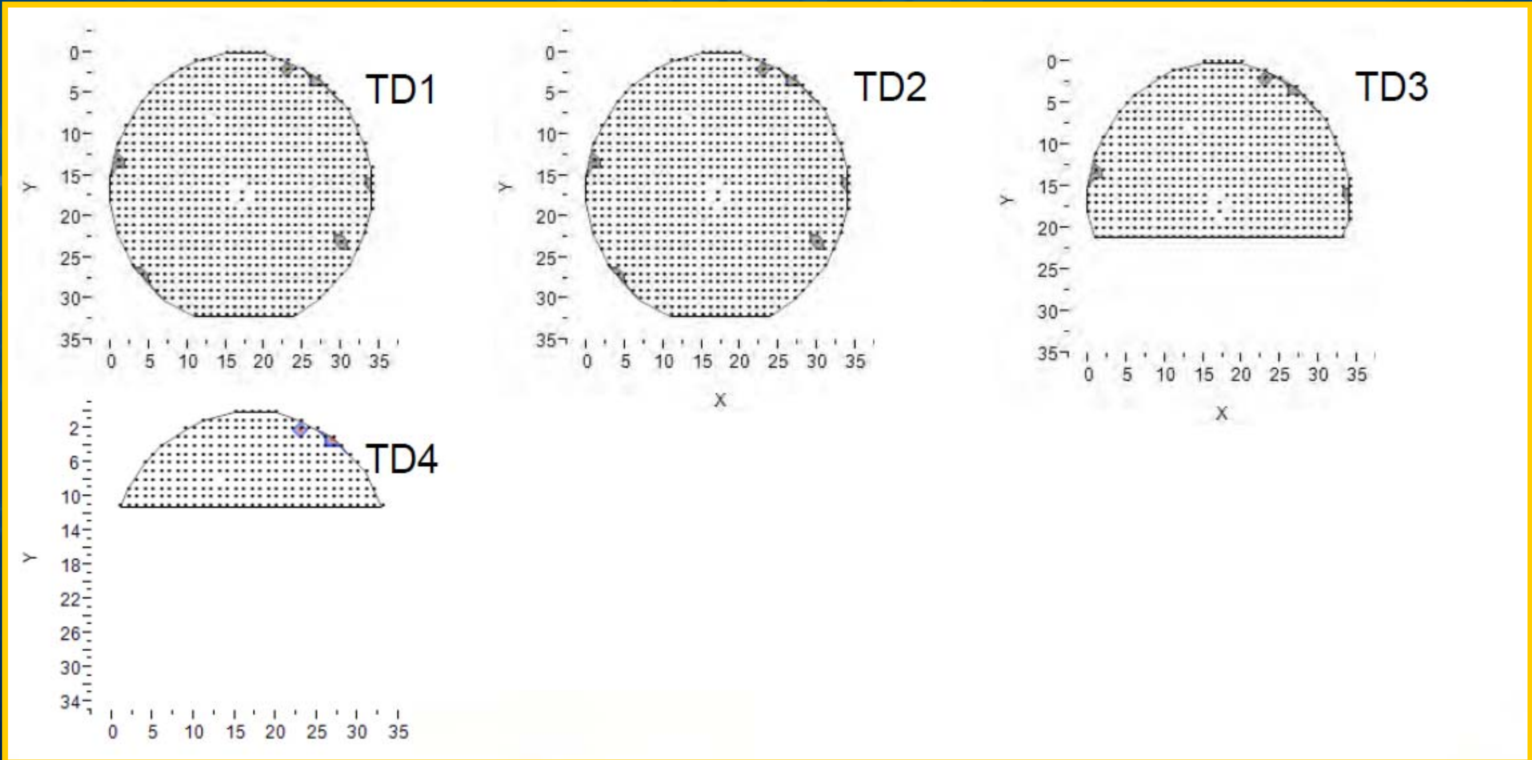
After DOE

Cu Pillar + Solder Cap Bump Wafer Spec		
VM	Operation instruction	RVSI 100 % Scan
	Critera	Probe Mark size can't exceed than bump area 25%
OQC	Operation instruction	1. Each lot, sample size: 12.5% 2. Each Wafer sampling inspection 5 areas, each area 3 dies
	Critera	Probe Mark size can't exceed than bump area 25%

Device	Bump damage rate of RVSI		Fail %
	Before Probing	After Probing	
HiXXXXV100WSS	99.60%	99.57%	0.03%
HiXXXXV100WSS	99.94%	99.89%	0.05%
HiXXXXV100WSS	99.79%	99.61%	0.18%
HiXXXXV100WSS	99.75%	99.70%	0.05%
HiXXXXV101WTS	99.78%	99.72%	0.06%
HiXXXXV121WTS	99.93%	99.74%	0.19%

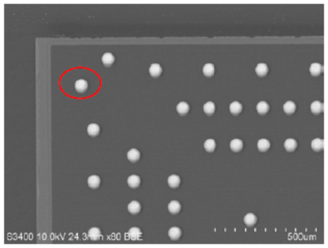
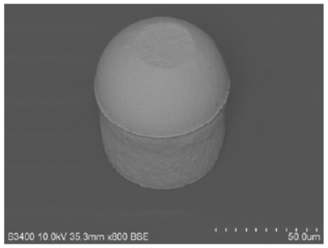
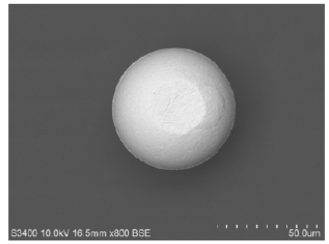
Die Test Results

- No Bin shifting observed
- Stability shown even with increasing TD and OD

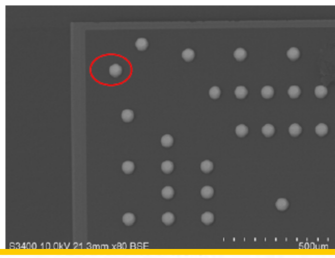
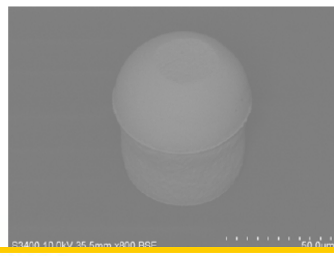
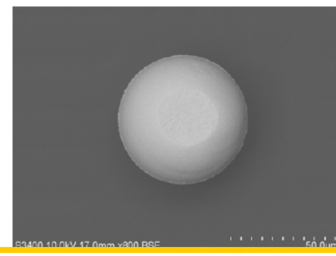


Probe Mark SEM Verification

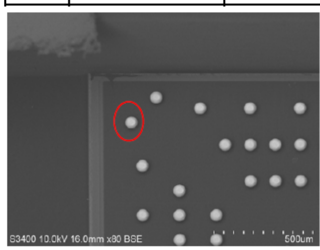
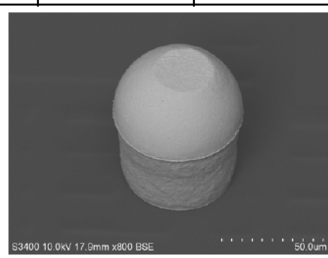
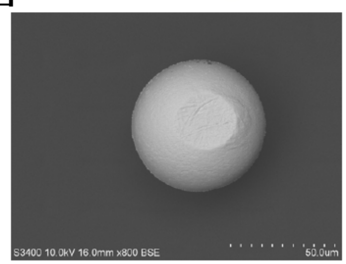
Leg	Unit location X	Unit location Y	Bump location	Probe mark area
C	6	9	1	20.86%

Leg	Unit location X	Unit location Y	Bump location	Probe mark area
F	7	18	1	13.19%

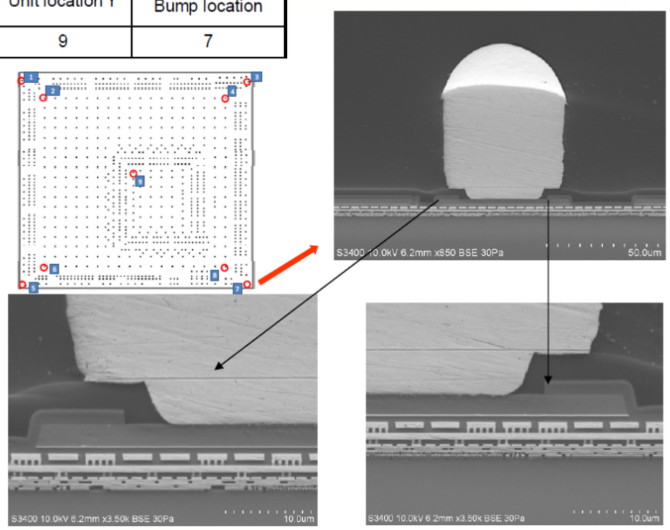
Leg	Unit location X	Unit location Y	Bump location	Probe mark area
I	13	31	1	20.11%

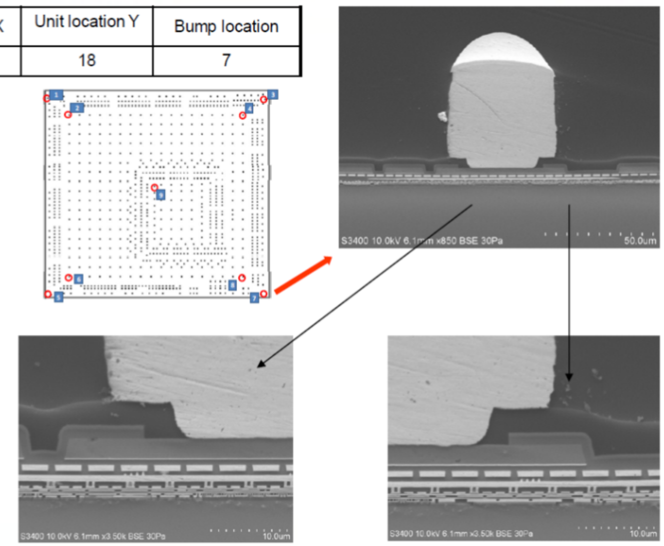
Ion Miller Verification of Low K Layer

- **No Low K cracking observed**

Leg	Unit location X	Unit location Y	Bump location
C	6	9	7

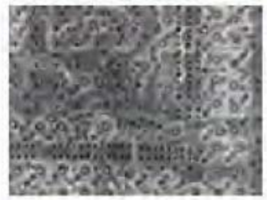


Leg	Unit location X	Unit location Y	Bump location
F	7	18	7



X-Ray Results

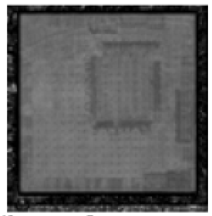
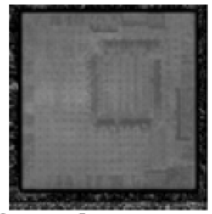
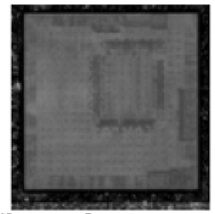
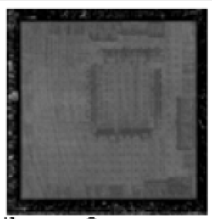
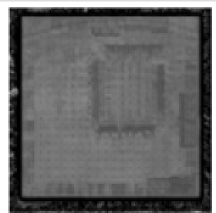
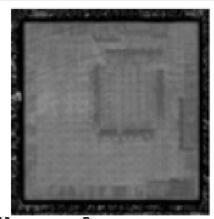
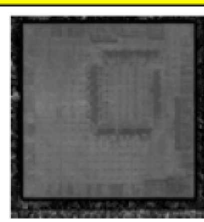
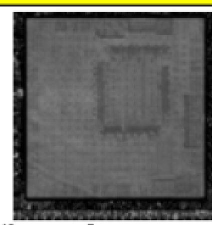
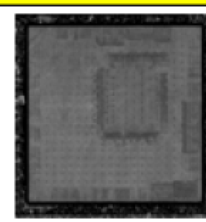
- **No Abnormality observed**

Leg	A	B	C
DB	 fail rate: 0	 fail rate: 0	 fail rate: 0
Leg	D	E	F
DB	 fail rate: 0	 fail rate: 0	 fail rate: 0
Leg	G	H	I
DB	 fail rate: 0	 fail rate: 0	 fail rate: 0

C-SAM Results

C-Mode Scanning Acoustic Microscope

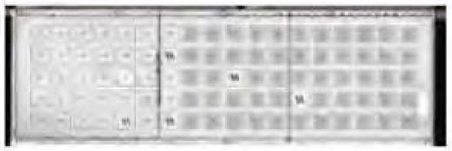
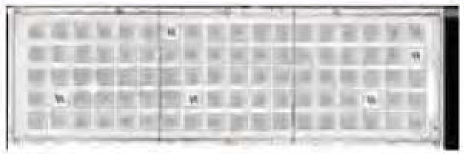
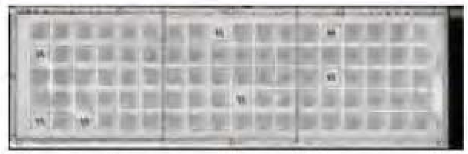
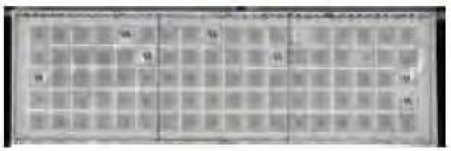
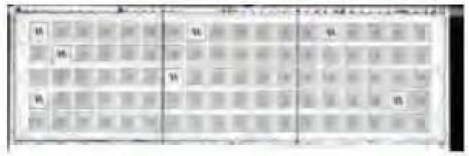
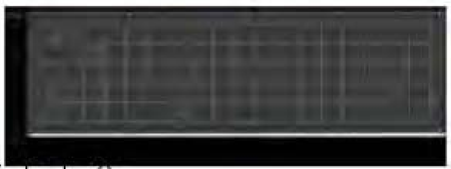
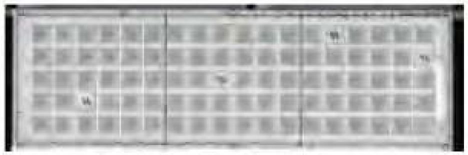
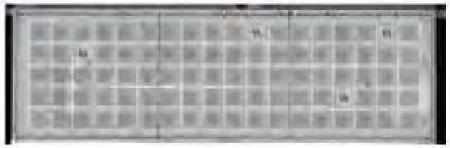
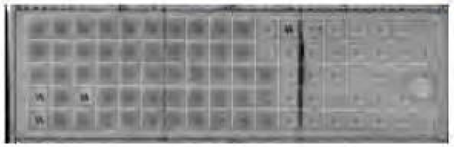
- **No Abnormality observed**

Leg	A	B	C
DB	 fail rate: 0	 fail rate: 0	 fail rate: 0
Leg	D	E	F
DB	 fail rate: 0	 fail rate: 0	 fail rate: 0
Leg	G	H	I
DB	 fail rate: 0	 fail rate: 0	 fail rate: 0

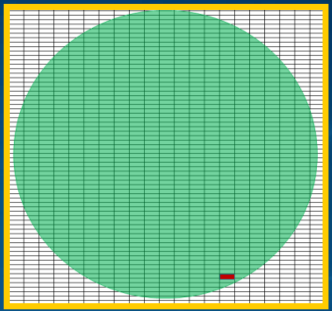
T-Ray Results

Terahertz Radiation

- **No Abnormality observed**

Leg	A	B	C
DB	 fail rate: 0	 fail rate: 0	 fail rate: 0
Leg	D	E	F
DB	 fail rate: 0	 fail rate: 0	 fail rate: 0
Leg	G	H	I
DB	 fail rate: 0	 fail rate: 0	 fail rate: 0

Current Status



- **High yield observed :**
  - 98% Die yield
  - 99% Mechanical bump damage yield
- **2 more Devices successfully completed reliability testing**
- **More than 10 devices are in full production**

Lifetime study versus actual

Probe mark and expected life time with aggressive clean Trio2milFlat pitch@80um

Customer	Patrs_ID	Device	#	Close die	Test Site	Initial tip extension	Current Tip extension	Current TDs	TDs per mil of tip extension loss	Life expectancy in TDs
HIS	HI0007	HI-3516	2	1317	2	18.26	16.67	135,736	85,369	875,881

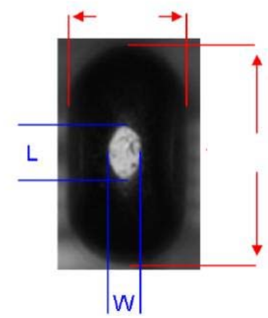
1-Obtain initial and current tip extension and TDs

2-Obtain TDs per mil of tip extension loss

3-Obtain life expectancy based on available tip extension and TDs per mil of tip extension loss

Set probe mark area = probe mark W x L

	OD	TD	Avg	Min	Max	Probe Mark Area %
A	50	2				3.21%
D	50	3				3.81%
G	50	4				3.87%
J	50	5				4.20%
B	75	2				4.07%
E	75	3				4.50%
H	75	4				4.71%
K	75	5				4.82%
C	100	2				5.09%
F	100	3				5.50%
I	100	4				5.65%
L	100	5				5.95%



The ratio of average probe mark area/bump area is pretty low.

Actual life time with optimized clean Trio2milFlat pitch@80um

1,921,787 TDs → 2 Million TDs !

Summary

- **Copper pillar probing requires not only electrical considerations, but also very precise mechanical probing techniques**
- **The positional accuracy of the probe contacts to the copper pillar is critical to prevent shearing and fractures during probing**
- **2 mil Trio probe contacts are an ideal solution for copper pillar applications**
  - Low cost
  - Tried and proven technology
  - Repairable
  - Short lead-time to market