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Low Temperature Test Implementation and Stabilization

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Outline

- Cold Probe – Why is it needed?
- Problem Statement
- Current Test Flows and how they are changing
- Measurement/Methodology
- Enabling Cold Probe
- Impact: Effectiveness & cost impact
- Acknowledgments

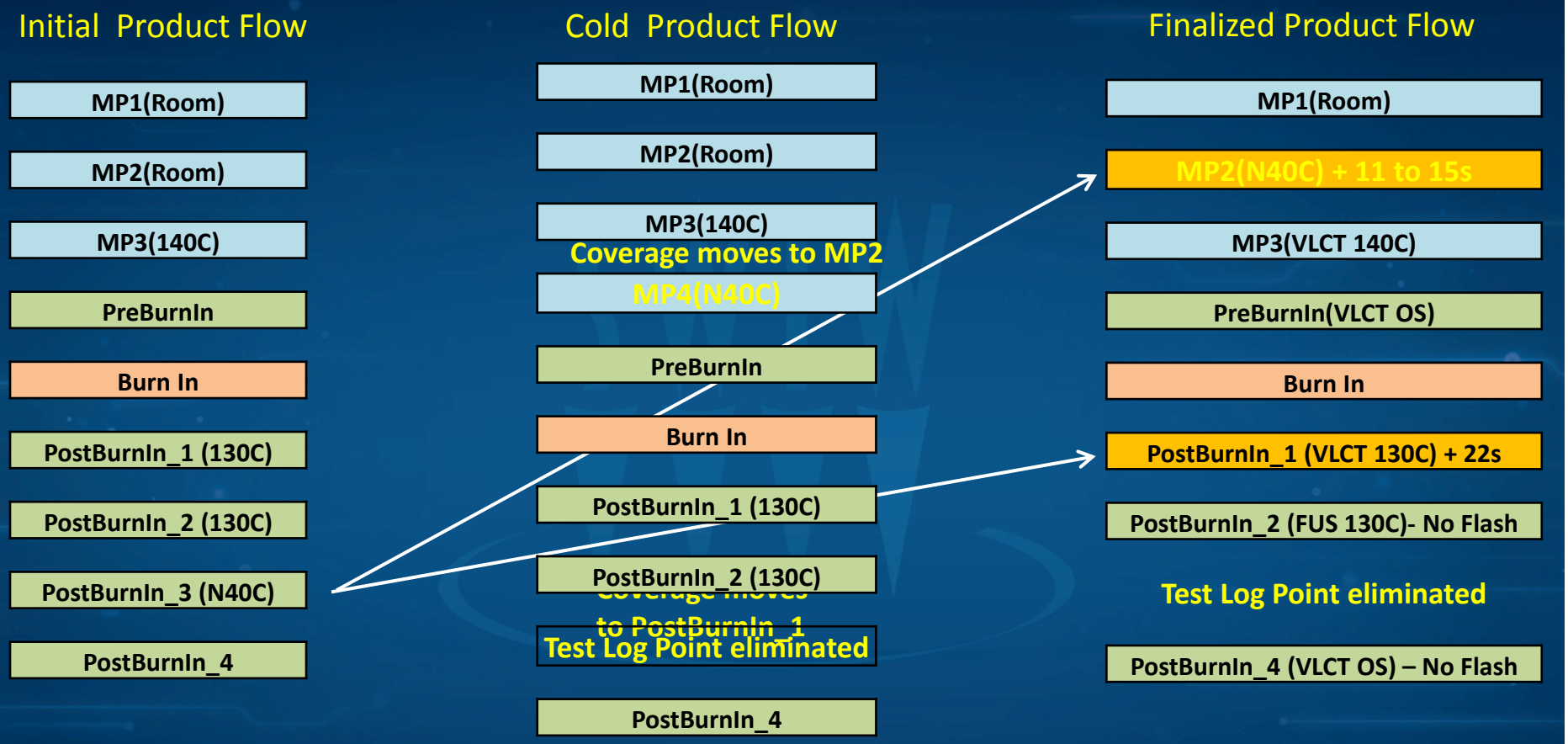
Cold Probe – Why is it needed?

- **Need to Reduce Test Cost**
  - Test cost is driven by multiple test insertions (up to 5X) and long test times specifically for flash memory flows.
- **Provide a stronger correlation to our packaged flows for direct wafer sales**
- **Improve quality for our customers**
  - Customers expect spec conditions duplicated at test.

Objective

- **Challenge: Provide a cost effective low temperature test solution for the TI product line.**
- **Show the effects of -40°C at test.**
- **Provide high quality/reliability standards for package flows and direct wafer sales.**
  - **Scrapping at the package level with multiple ICs for 1 faulty IC is expensive.**
- **Obstacles:**
  - **Protecting production material and high cost probe cards from thermal expansion and contraction.**
  - **Provide adequate moisture shielding to inhibit condensation as well as prevent current leakage during testing.**

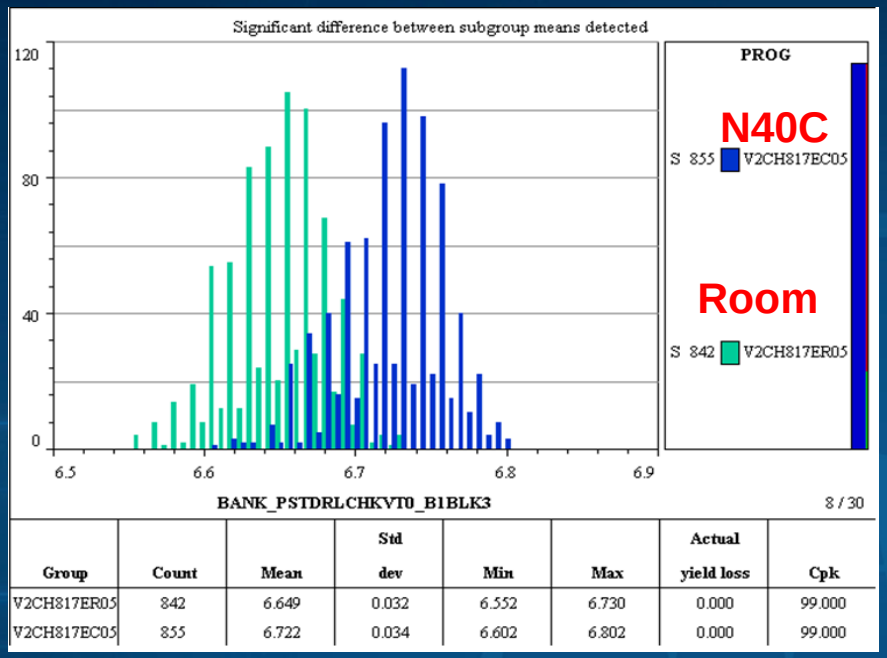
Cold Temp Probe: What's Changing?



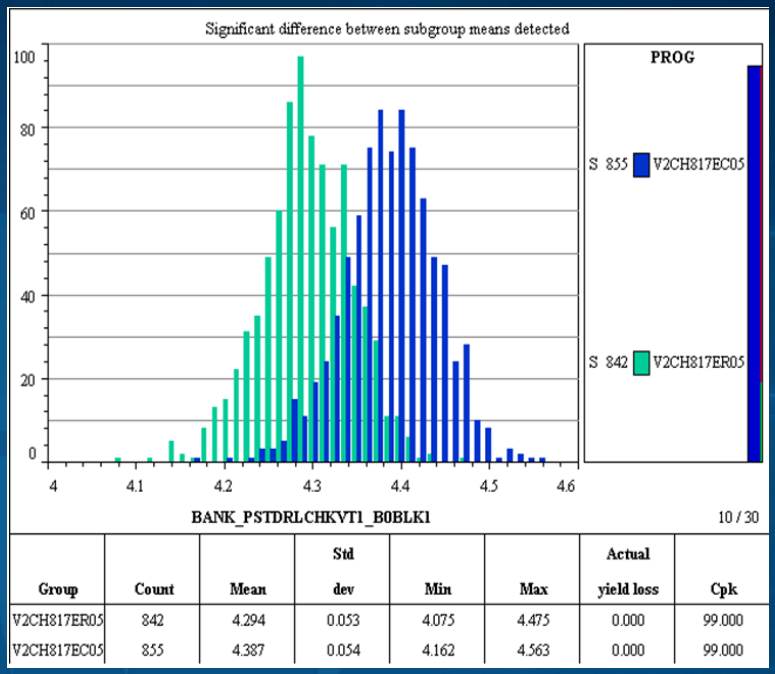
- **Post Burn in Coverage (Most Flash / All Digital & Mixed signal tests) are being moved to MP2.**
  - **The team was challenged with demonstrating room temperature to low temperature correlation, prove that parametrics moved predictably with temperature, and provide full test coverage.**

Cold Temp Probe Results

VT/DRL parameter correlation (Room vs. -40°C - Programmed at 30°C)



Group	Count	Mean	Std dev	Min	Max	Actual yield loss	Cpk
V2CH817ER05	842	6.649	0.032	6.552	6.730	0.000	99.000
V2CH817EC05	855	6.722	0.034	6.602	6.802	0.000	99.000



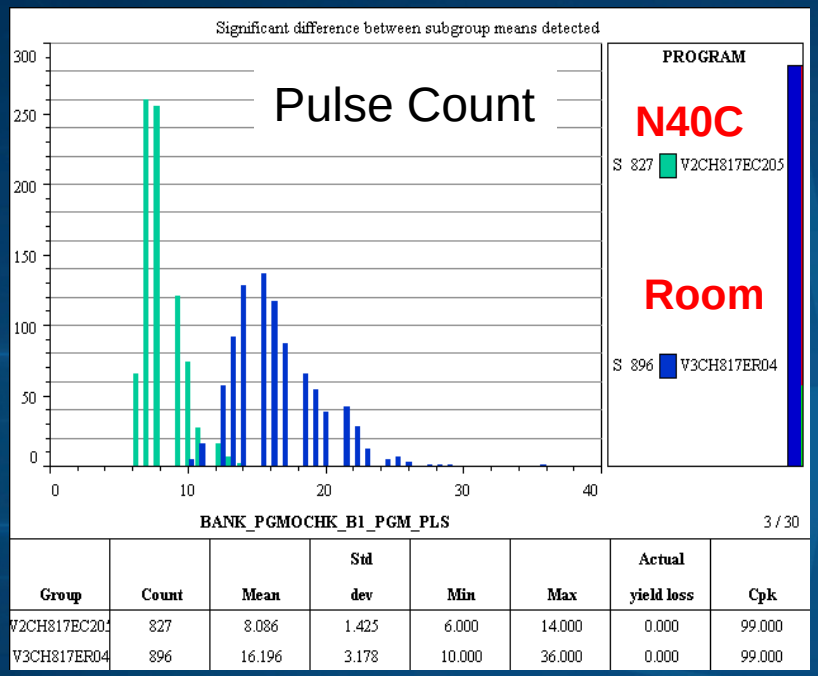
Group	Count	Mean	Std dev	Min	Max	Actual yield loss	Cpk
V2CH817ER05	842	4.294	0.053	4.075	4.475	0.000	99.000
V2CH817EC05	855	4.387	0.054	4.162	4.563	0.000	99.000

•VT0's, VT1's, DRL deltas & pump measurements remained stable at the -40°C insertion.

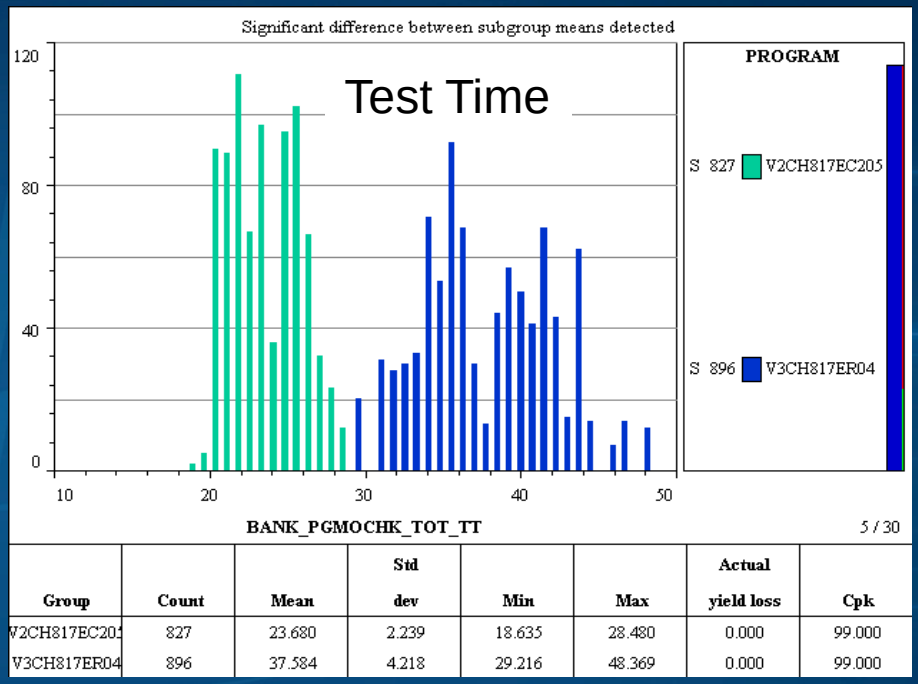
- Above are the post MP1 DRL VT's measured at 30°C & then at -40°C temp during the MP2 combined flow.
- VT0 moved up by ~70mV at -40°C (expected).
- VT1's moved up by about ~90mV at -40°C (expected).
- Data Retention Loss deltas moved by the same amount due to the VT moves.
- Per die analysis shows predictable results post MP1 and when tests were repeated post MP2.

Cold Temp Probe Results

Room Temperature vs. -40°C Slow Program Results



Group	Count	Mean	Std dev	Min	Max	Actual yield loss	Cpk
V2CH817EC201	827	8.086	1.425	6.000	14.000	0.000	99.000
V3CH817ER04	896	16.196	3.178	10.000	36.000	0.000	99.000



Group	Count	Mean	Std dev	Min	Max	Actual yield loss	Cpk
V2CH817EC201	827	23.680	2.239	18.635	28.480	0.000	99.000
V3CH817ER04	896	37.584	4.218	29.216	48.369	0.000	99.000

- Shown above are pulse count comparison & slow program test times for room vs. -40°C probe insertions.
- This data set is not for the same wafer but an engineering wafer at -40°C vs. production data from another wafer from the same lot.
  - Fewer pulses needed to perform the slow program & lesser time needed at -40°C .
  - This is resulted in a unexpected test time reduction.
  - The slow program at -40°C takes ~23 seconds as compared to 37 seconds at 30°C.

Cold Temp Probe Results

- **Engineering Evaluation**
  - Probe MP2 at Room with short flow material (Ireference, Pump & DRL only – No changes to the flash state).
  - Probe MP2 at -40C (Full Low Temperature Flow).
  - Probe MP3 at 30C (Ireference, Pump & DRL only – No changes to flash state).
    - These measurements were used as a reference for 30°C vs - 40°C correlations for post MP2 VT's.
- **Final Results**
  - During a 3X3 lot evaluation limits were pushed out by 35% at MP2 to be able to see the whole VT, pump measurement distributions and final test comparison.
  - Correlation at final test was one to one.
  - No changes were seen to Go-Nogo type tests (Flash/Digital).
  - The team was able to demonstrate 30°C to - 40°C characterization and prove that parametrics moved predictably.
  - Characterization shmoos where utilized to assess the margins at -40°C and then compared to 30°C shmoos.
  - All the shmoos looked clean with some shmoos having shmoo holes. Similar holes were observed in the 30°C plots.

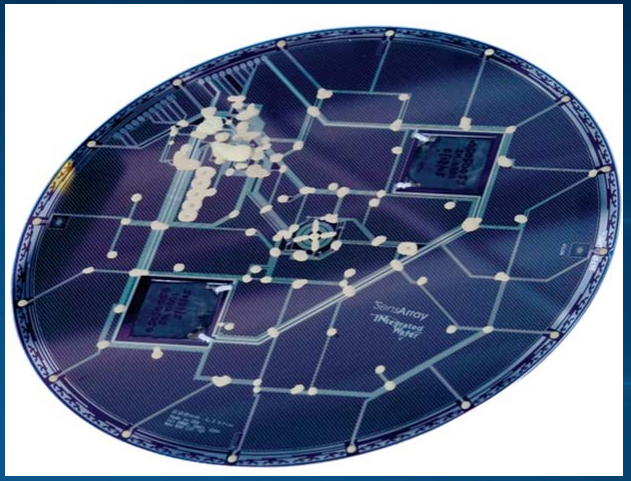
Test Cell Measurement Methodology

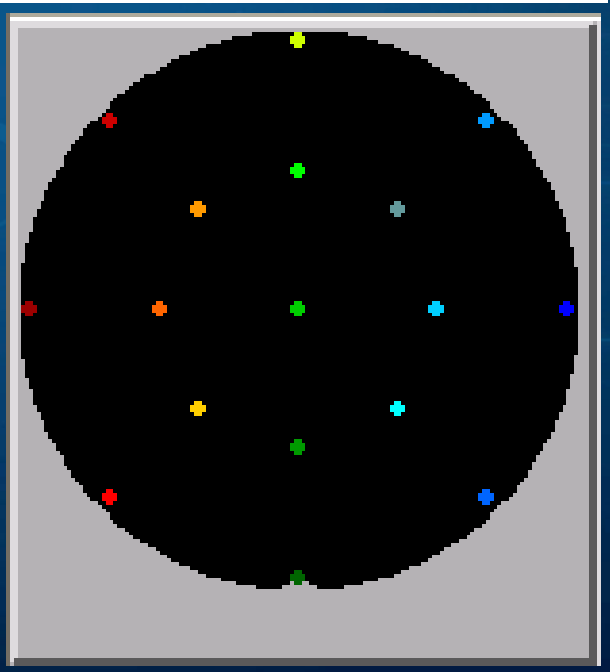
Measurement Methods

- Profile chuck temperature during setup and probing
- Profile probe card temperature during setup and probing
  - Modify the probe card to allow insertion of temperature probes at three positions adjacent to probe needles and probe needle support
- Profile the probe chamber environment.
  - Humidity (Dew Point temperature)
  - Air flow (Compressed Dry Air (CDA) purge requirements)
- Correlate measurement data to probe position effects
- Develop methods to counter effects

SenseArray Integrated Wafer

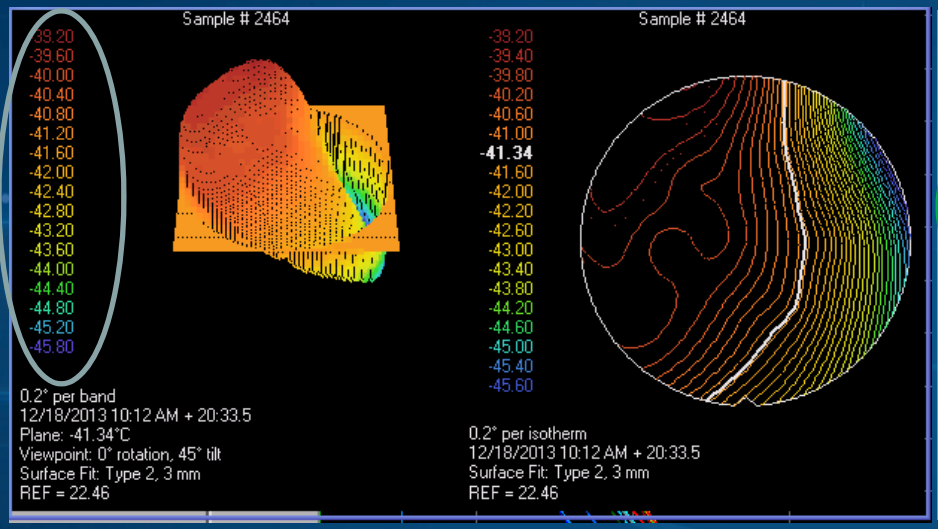
- 17 imbedded thermocouples
- Sampling rate set at 1 second intervals during 30°C to -40°C and 30°C to -55°C cool down.
- Loaded the wafer on the chuck for approximately 60 minutes.

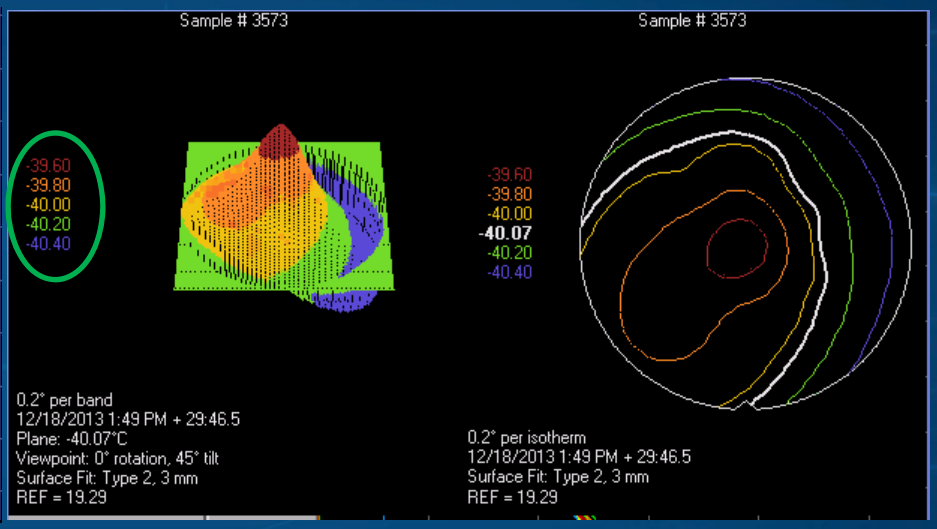




Chuck Temperature Profiles

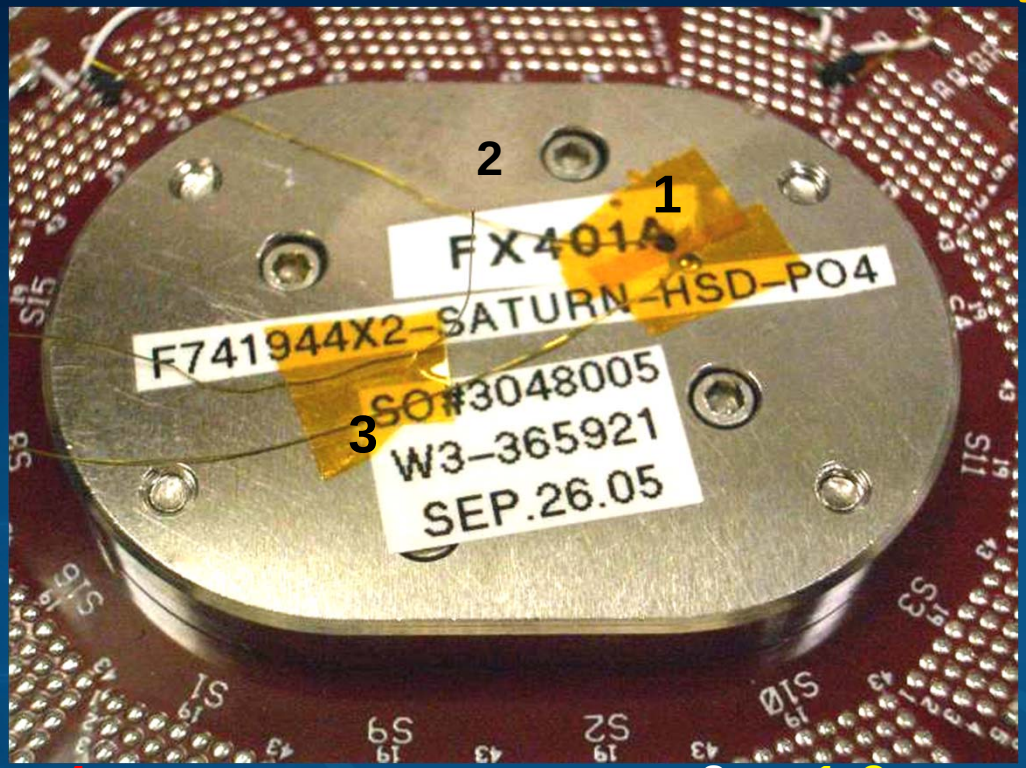
- Vendor A chuck temperature gradient at -40ºC: 6.6°C
- Vendor B chuck temperature gradient at -40ºC : 0.8°C





- After an elapsed time of 35 minutes the vendor A chuck temperature gradient remained at a delta of 6°C
- The vendor B chuck had stabilized to <1°C in 27 minutes
- Both vendors had equivalent CDA consumption rates and maintained <-70°C dew point temperatures

Probe Card FX401 with TC(K) Installed

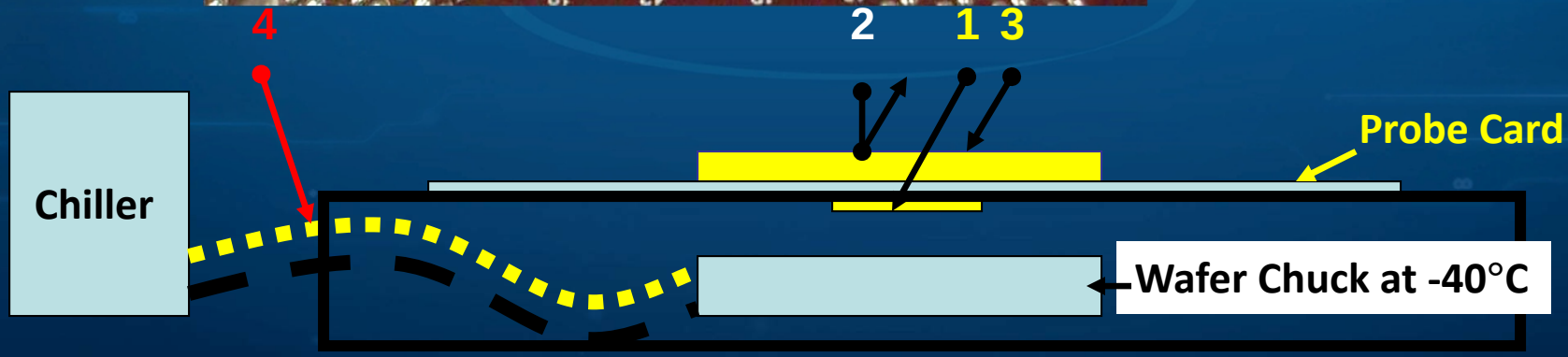


1 - Probe depth

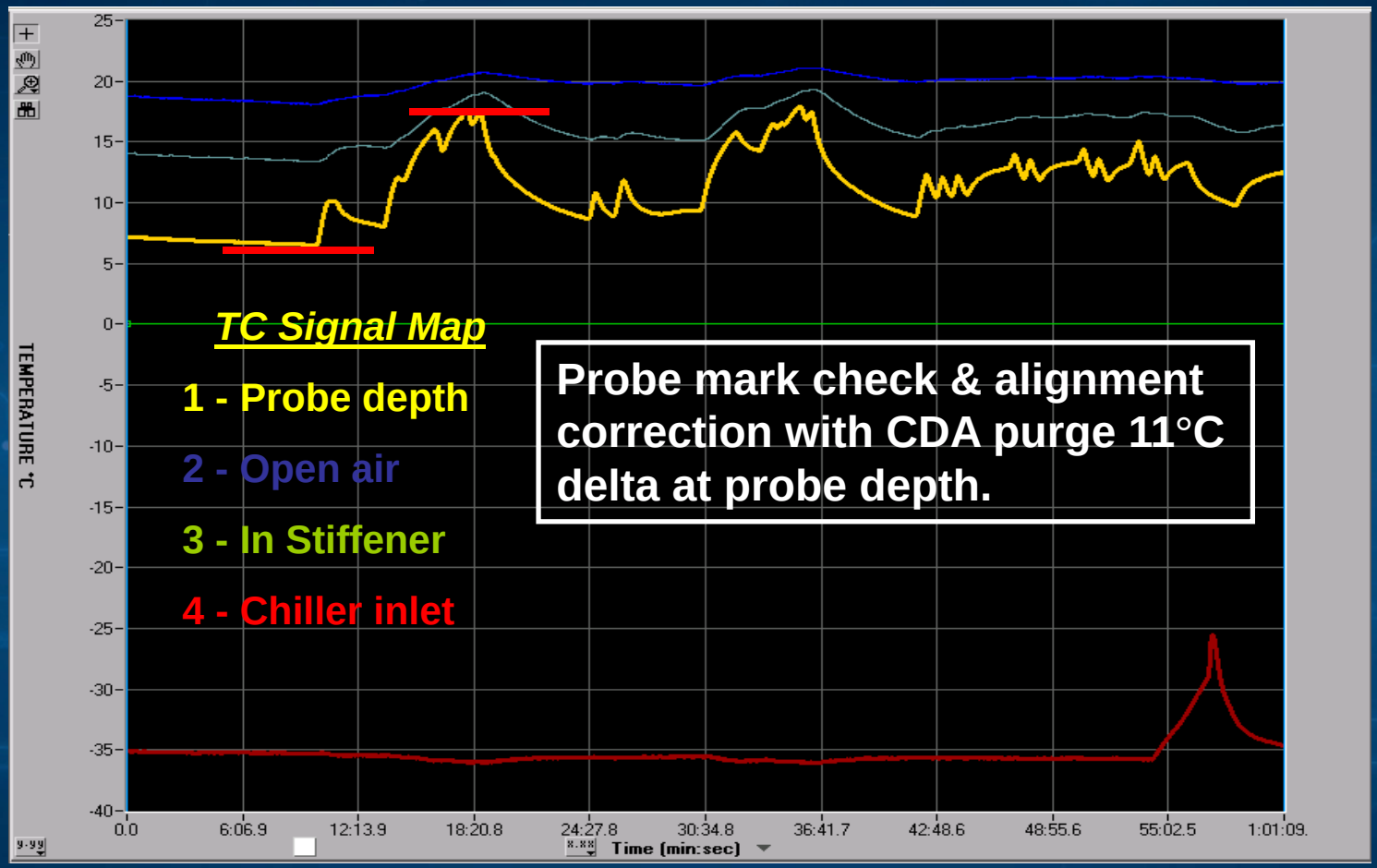
2 - Open air

3 - In Stiffener

4 - Chiller inlet

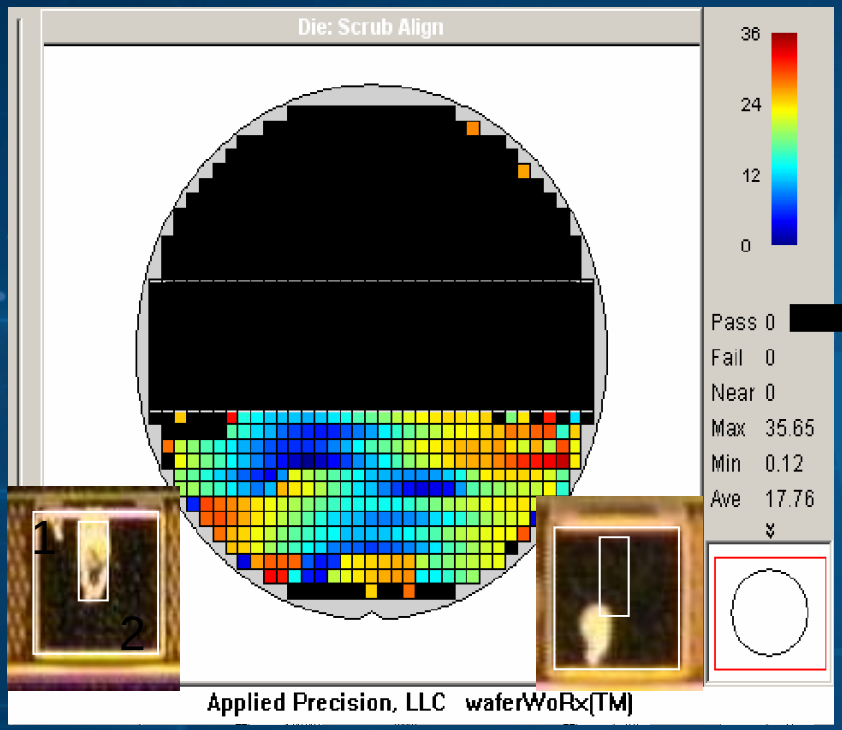


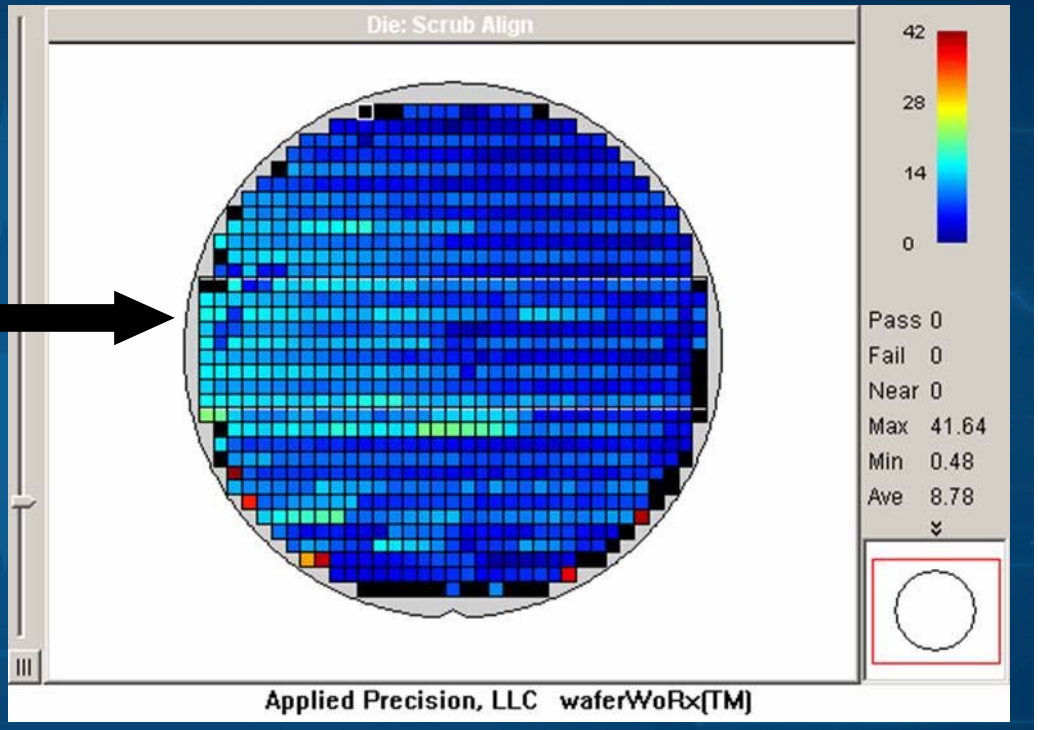
Probe Card FX401 Temperature Profiles



Scrub Alignment at -40°C

- No shielding, no re-alignment
- Ceramic cap utilized, 10 min. re-alignment

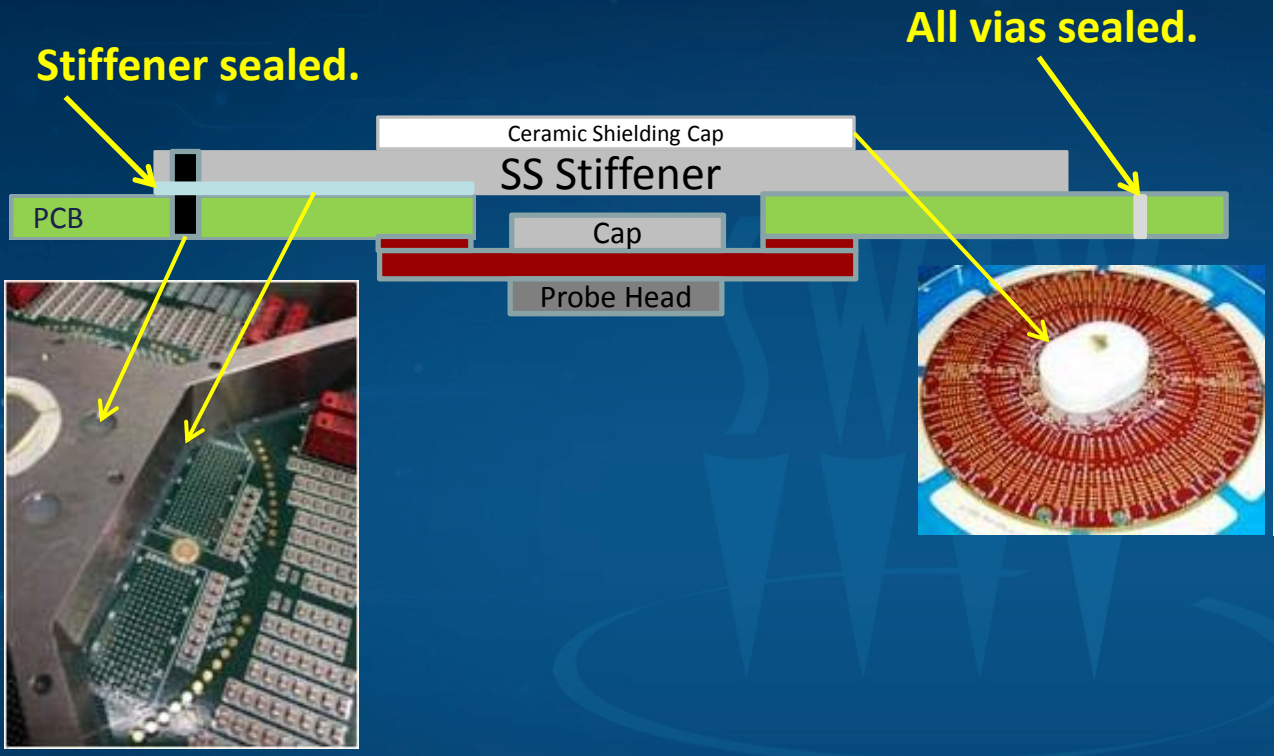


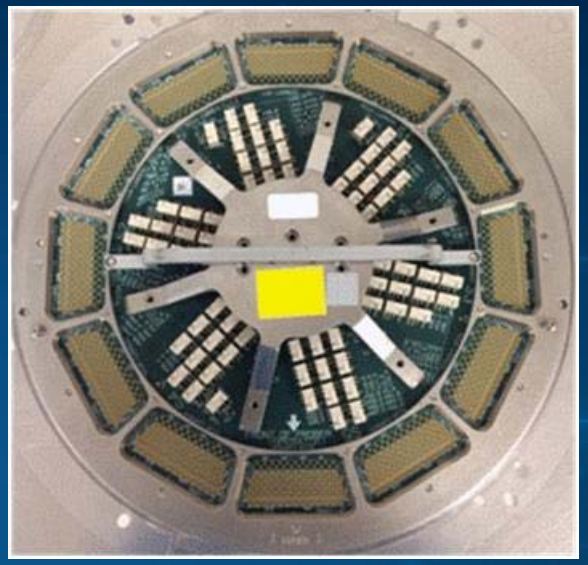


- Thermal affects were causing needle movement.
- Greater than 30 um lateral drift seen between center and edge of wafer
- Re-alignment routines required to maintain probe to pad alignment (PTPA)

Enabling Cold Probe: Test Cell Hardware

Probe Card Modifications



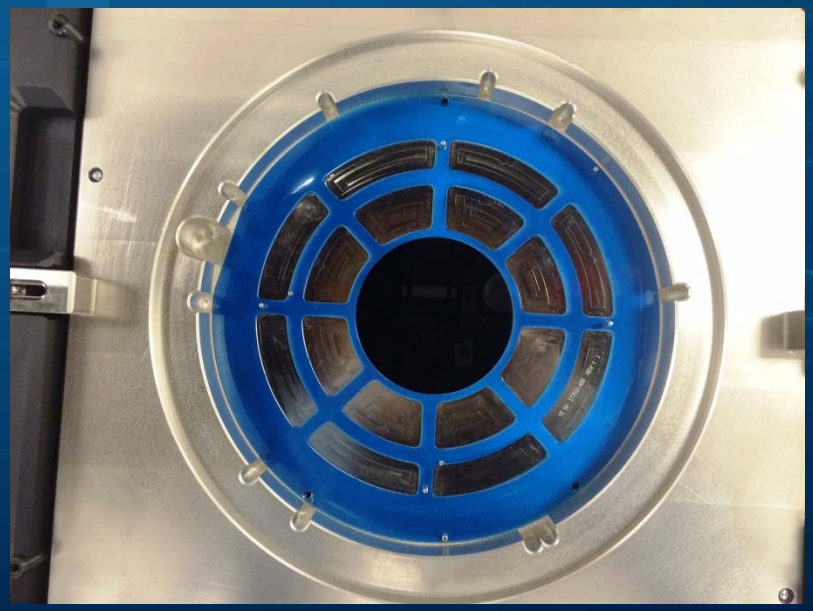


Sealed PC with wagon wheel stiffener.

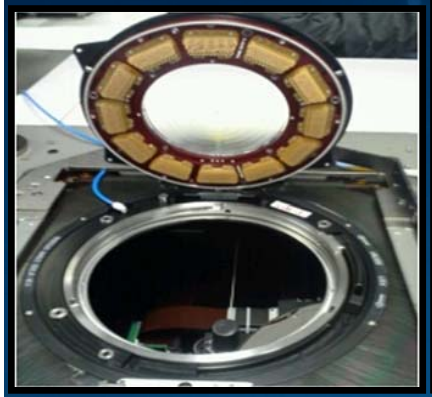
- Stainless Steel stiffener plate is utilized to limit thermal movement
- Ceramic shielding cap is utilized to maintain card temperature
- No through hole vias - all vias must be sealed (silver coat epoxy) to maintain probe chamber environment

VLCT Test Cell Hardware

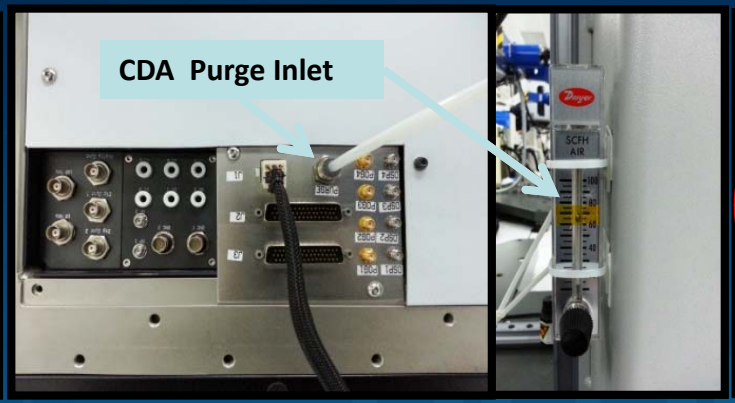
- Coolant / Air Cooled System
- Sealed Native Ring / RASP Interface
  - Invar pan utilized to prevent drift
- Sealed UF300/3000 with:
  - Purge air distribution system
  - Hygrometer to monitor dew point



IFlex Test Cell Hardware

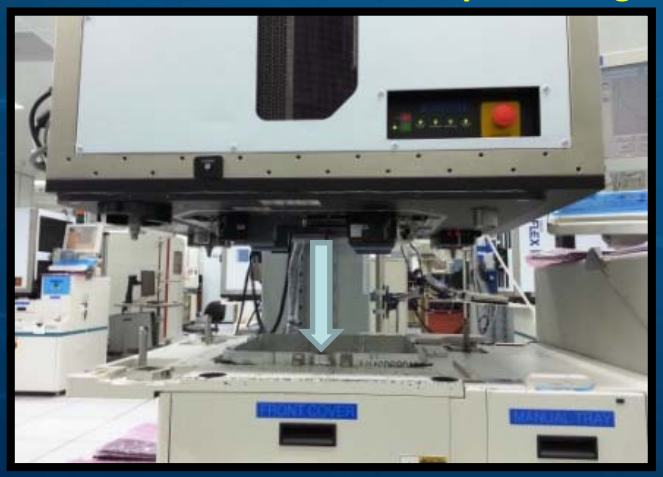


Sealed towers



SC designed I/O panel with Tester Purge inlet & Backside Purge with Flow Meter and pressure gauge

Backside Purge with Flow Meter and pressure gauge

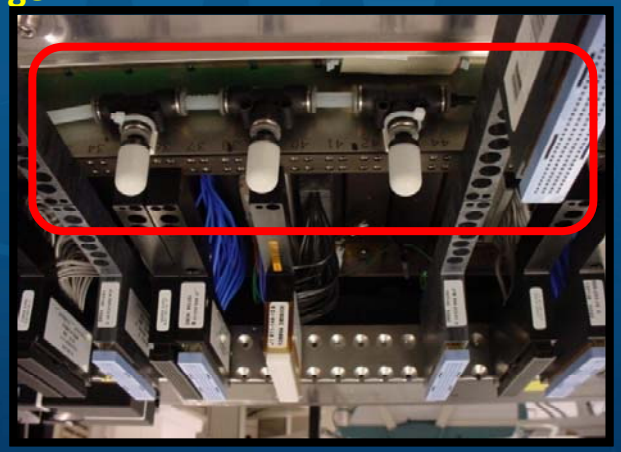


Advantages:

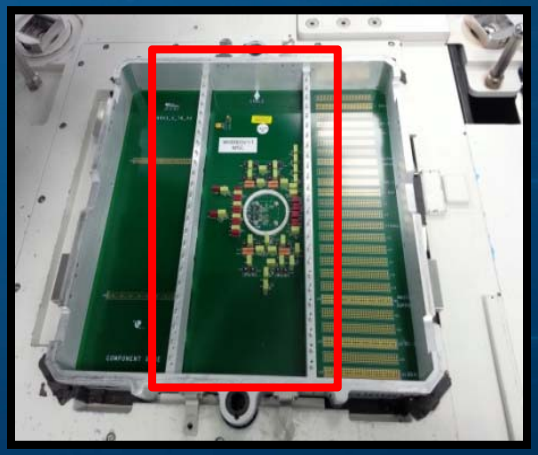
-Reduce moisture issues

-Reduce setup/conversion failures

-Increase MTBA and Output

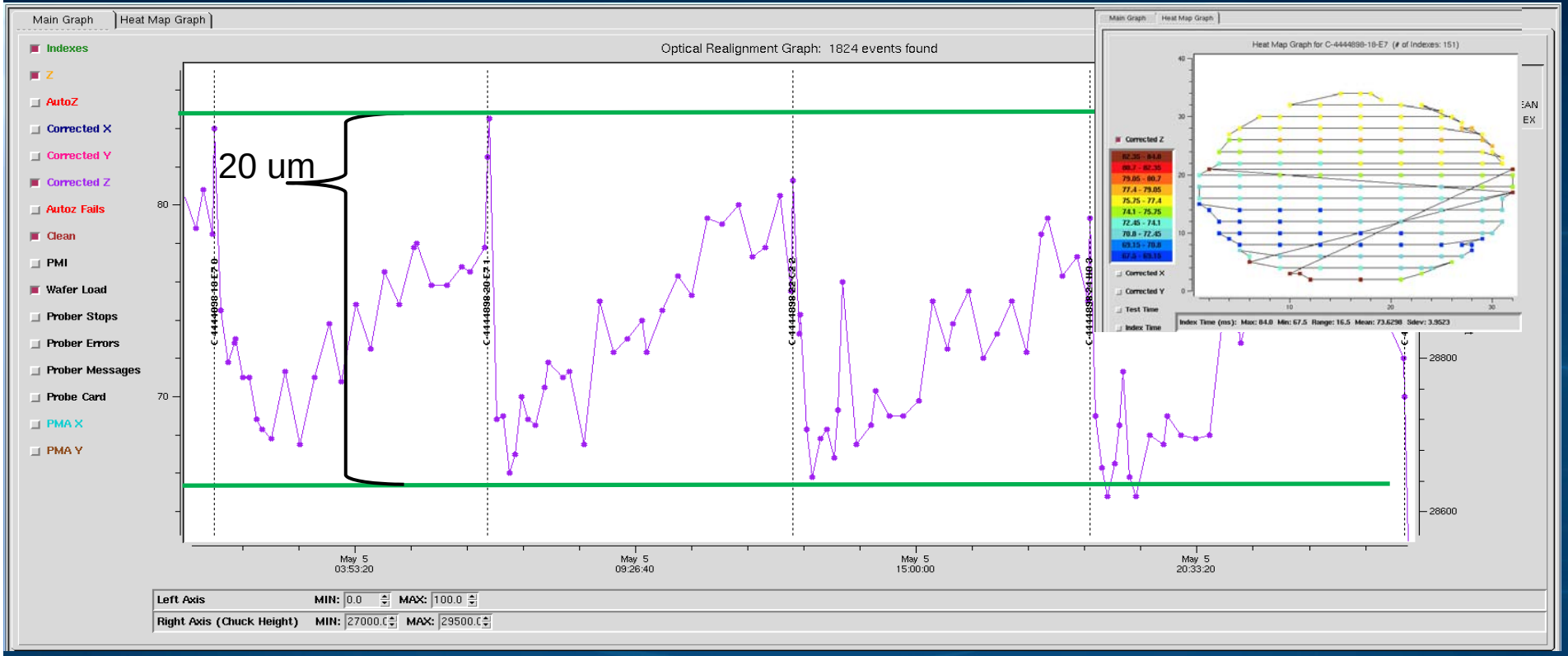


Back side purge diffusers attached inside IFLEX Test Head



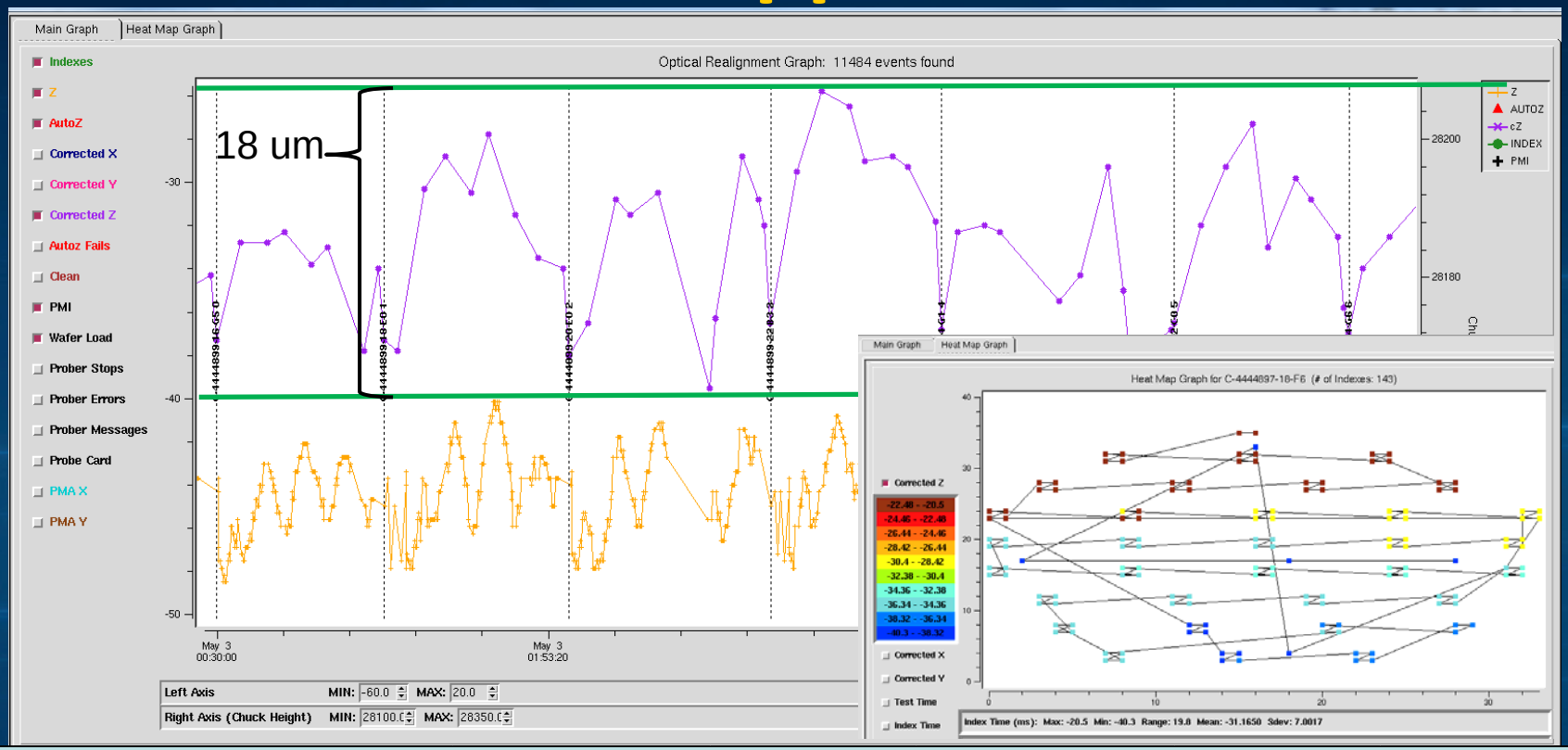
Probe Insert

Implementation of the Invar Head Stage



- **High Temperature Stabilization (140°C Trials):**
  - Invar head stages were utilized on all test cells testing above 75°C
  - Ceramic head stages were phased out due to maintenance issues
  - Probe card needle movement was reduced to ~20 um in the Z axis

Lessons Learned Applied to Cold Probe



Testing Temp: -40°C					
Measurement	**ST4xx Ceramic**	**ST4xx Invar**	**ST8xx Ceramic**	**ST8xx Invar**	**ST9xx Invar**
Within Wafer Delta Z (um)	**82.5**	**65.8**	**32.6**	**26**	**20.5**

- **Low Temperature Stabilization (-40°C Results):**
  - **Lessons learned improved leakage failures as well as X, Y, and Z thermal drift**
  - **With 4 to 5 pass probe flows AVI loss is controlled to < 0.25%**

Improved Temperature Capability

Project: Standardize to air cooled chiller systems for cold probe capability in EBT.

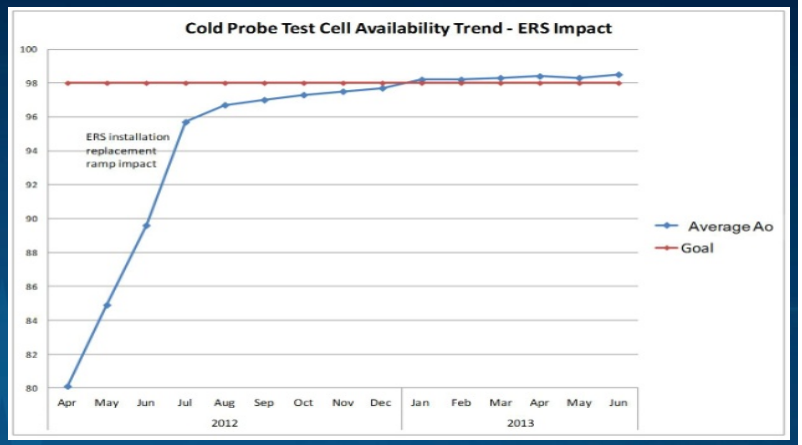
- 19 Air Cool Plus units installed and qualified

Impact

- Achieved 11% Ao improvement from baseline systems.
  - In house sealing of UF3000 probers allowed for cost avoidance of 5 additional cold probers
- MTBF ≥ 42 K hrs: **Article 1 has exceeded 40 K hrs of operation without fail**
- Enabled -40°C to 200°C probe capability
- Reduced coolant costs by $40K per year.
- 86% reduction in heat transfer fluids used to cool the probing chuck during low temperature product testing

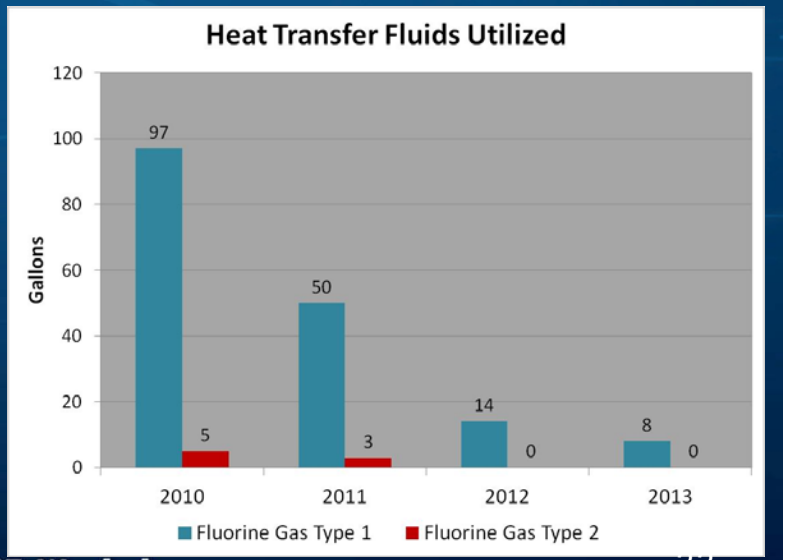
Current Status :

- First article for UF3000 Air Cool option installed on Fusion platform
  - Enables 20°C to 200°C probe capability
  - Reduced chuck cooling times (4 hour wait time reduced to < 30 min.)
- 9 UF200 air cool units implemented on VLCT and IFLEX platforms
  - Reduction in chuck cooling times (3 hour wait time reduced to < 12 min.)



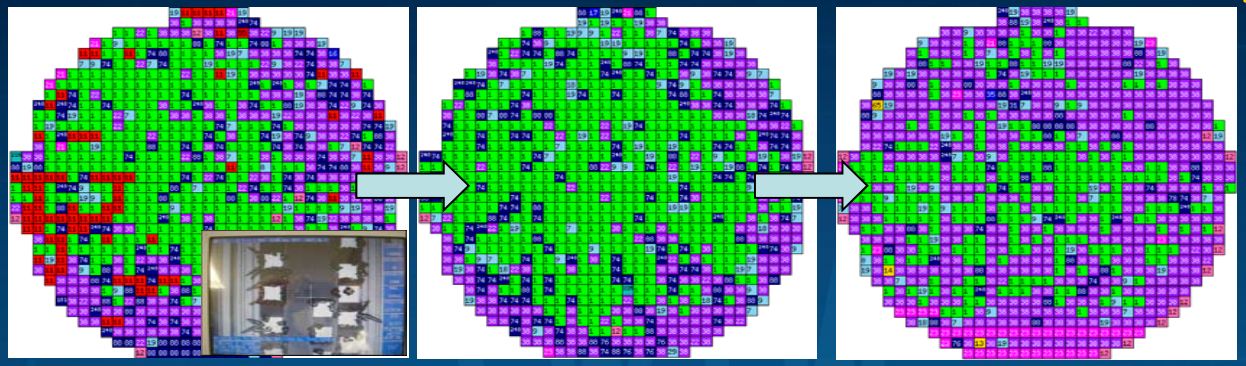
Cold Probe Test Cell Availabiltiy Across 19 Systems									
	Apr	May	Jun	Jul	Aug	Sep	Oct	Nov	Dec
Average Ao	80.1	84.9	89.6	96.7	97.7	95.1	97.0	94.3	97.5
Goal	98	98	98	98	98	98	98	98	98

Greenhouse Gas Reduction



Effects of -40°C at Test

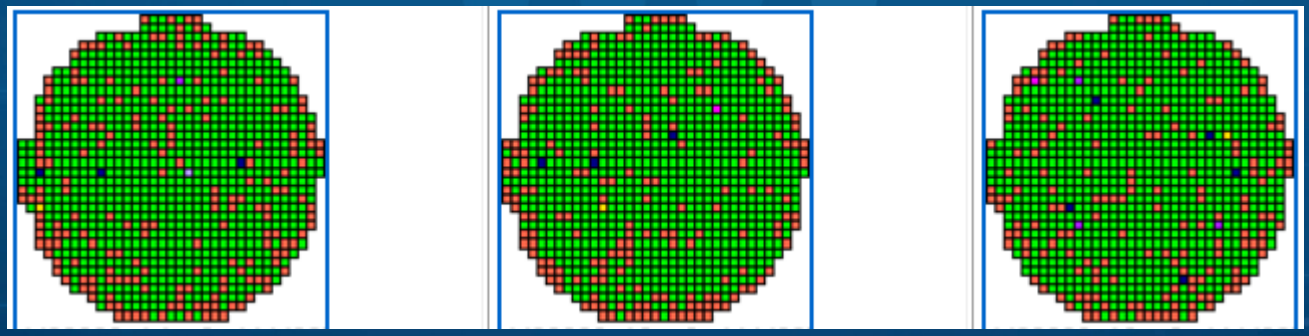
-40°C Probe: Native to RASP Comparison



•Leakage at docking interface results in icing/opens.

•Seals improve opens failures but current leakage failures remain.

•RASP hardware highlights current leakage failures.



- **Current Leakage Resolution:**
  - **The most recent -40°C probe passes have showed stable yield (> 80%) with no leakage failures**
  - **Prober hardware modified to allow a top down CDA purge as well as minimize pin to pad drift**

Summary of Findings

- **Low temperature probe has provided a stronger correlation to our packaged flows for direct wafer sales and reduced overall test cost.**
- **The test team was able to demonstrate 30°C to - 40°C characterization and prove that parametrics moved predictably.**
  - Implementation of cold probe at MP2 was proven to eliminate final test insertions without adding additional wafer level probe passes.
- **The implementation of air cooled technology improved tool availability, reduced cost of ownership, and allowed for a reduction in Greenhouse gasses utilized.**
- **Modifications of test cell hardware included:**
  - Sealed Probe Cards / Head Stages / Probe Chambers
  - Top down CDA purge
  - Implementation of specific head stage alloys to avoid AVI loss

Acknowledgements

- Alan Wegleitner
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