IEEE SW Test Workshop

Semiconductor Wafer Test Workshop

June 8 - 11, 2014 | San Diego, California

ILD Study: Contact/Deprocessing Methodology Comparison

Jory Twitchell FSL-CHD

Jeff Reeves FSL-OHT

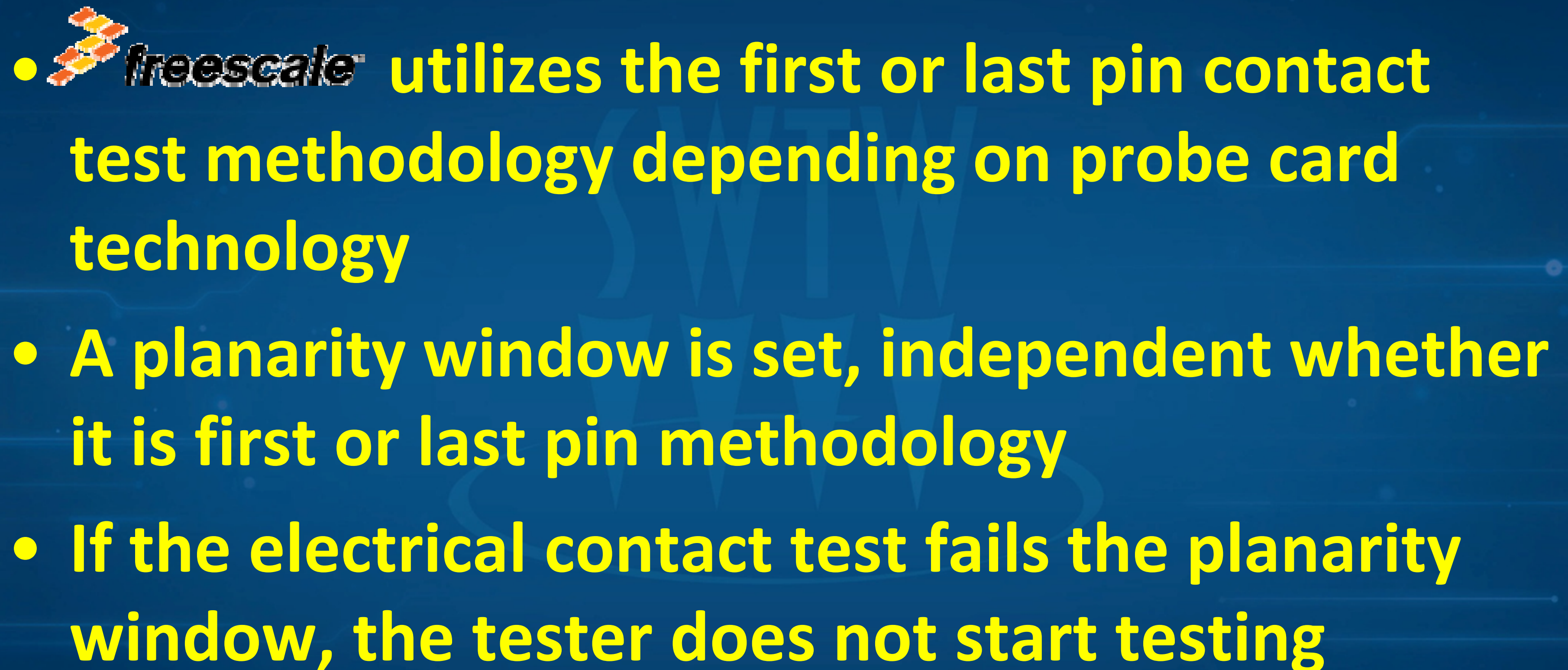
Overview

- **Background**
  - ILD study comparison (Probe induced pad damage)
- **Contact method**
  - Electrical
  - Visual
- **Deprocessing method**
  - HCL
  - AL etch
- **Conclusion**

Background

- **ILD studies done at all Freescale sites, internal and external**
  - Different methods used between sites
- **Develop method how to set the initial prober Z contact position which can be easily copied**
- **Accurately detect ILD cracking without causing additional damage**
- **Roll out one method for all sites to follow**

Electrical Contact Test Theory



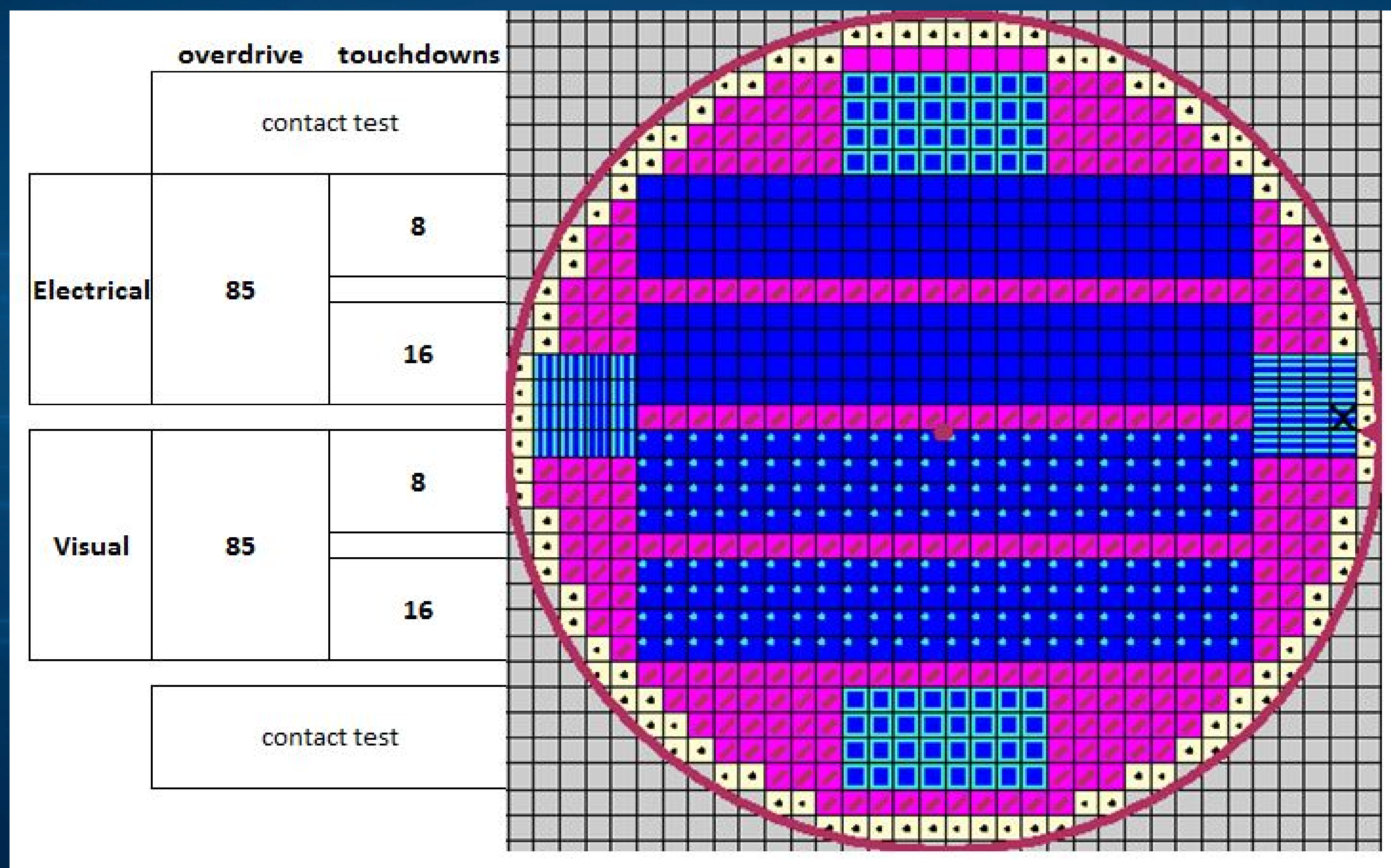
- freescale utilizes the first or last pin contact test methodology depending on probe card technology
- A planarity window is set, independent whether it is first or last pin methodology
- If the electrical contact test fails the planarity window, the tester does not start testing

Electrical Contact Test Applied

- **This study used electrical contact test from first pin**
  - The electrical contact test had a planarity window of 30 microns
  - The planarity window is measured from first pin to last pin and over travel applied to first pin

Wafer Setup

- Setup a single wafer with both Electrical and Visual setups



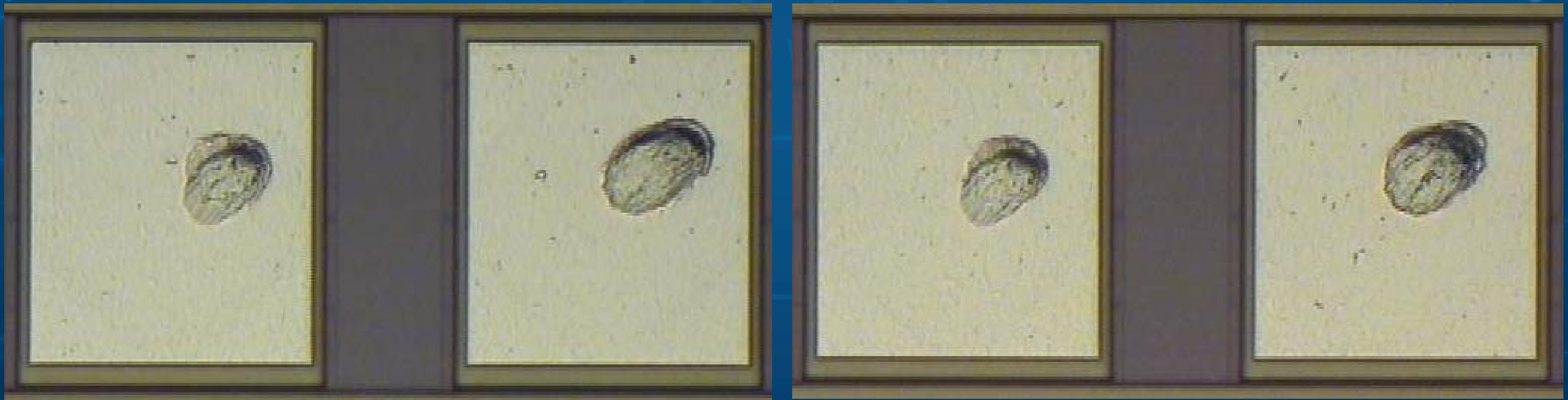
Note: The probe card is a 4x4 array

Probe Mark Examples

- Electrical setup probe mark examples
  - 8 touchdowns
  - 16 touchdowns

Probe Mark Examples

- Visual setup probe mark examples
  - 8 touchdowns
  - 16 touchdowns

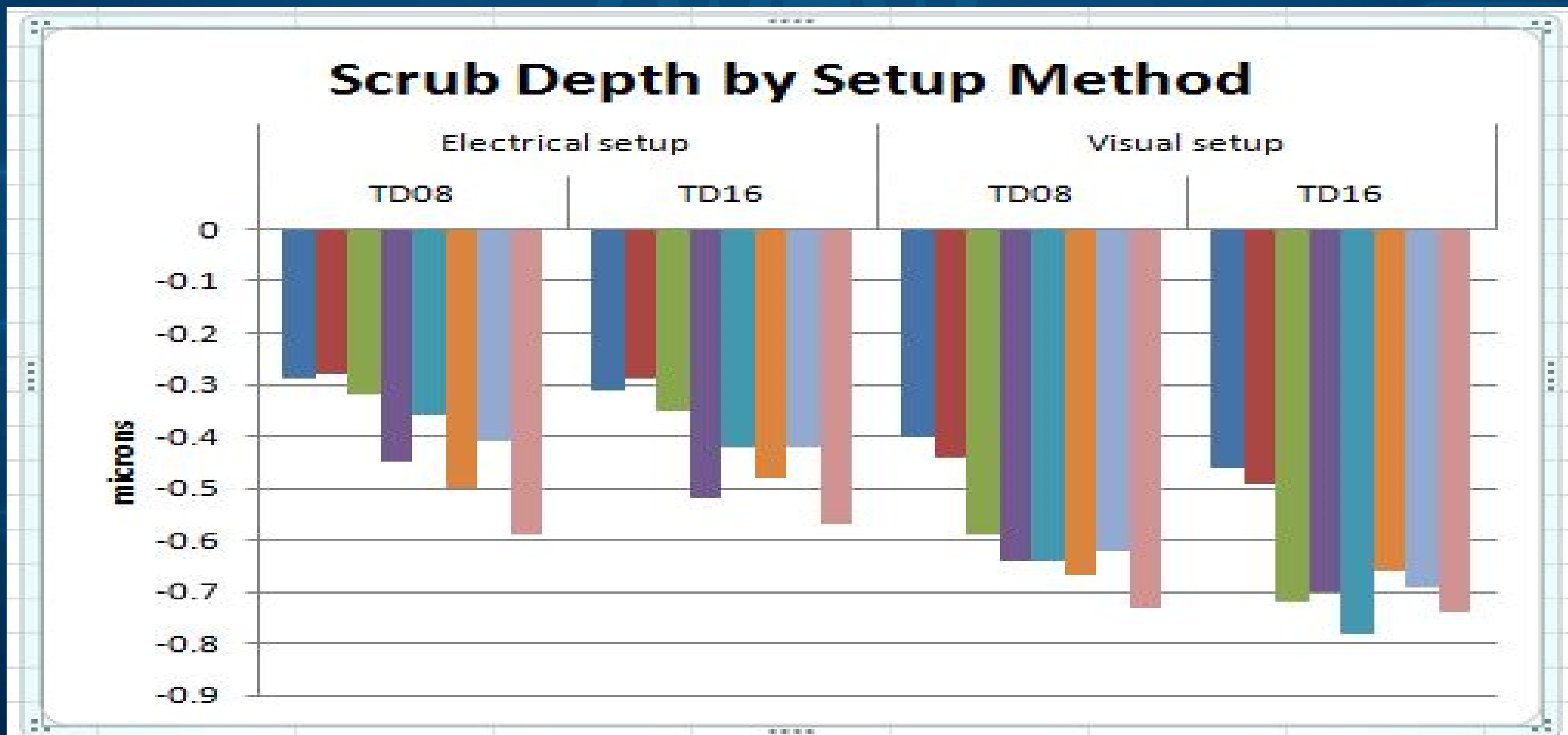


Probe Mark Depth - Measure

- **Measure scrub depth on 8 pads per cell – Same DUT, same pads used for each cell**

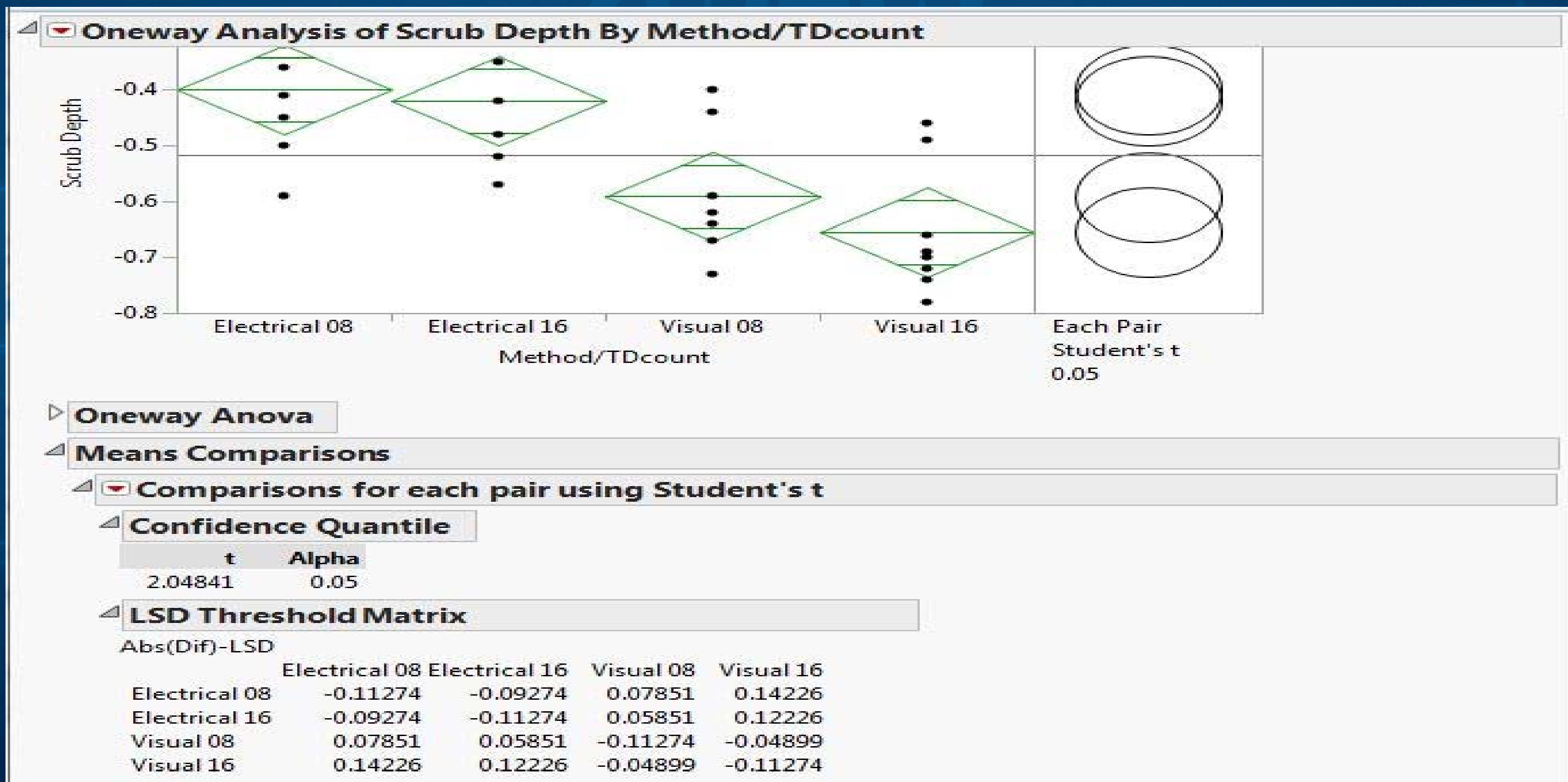
Probe Mark Depth -Plot

- Comparison of scrub depth by setup method and touchdown count



Probe Mark Depth – JMP Analysis

- **JMP scrub depth analysis**



t	Alpha
2.04841	0.05

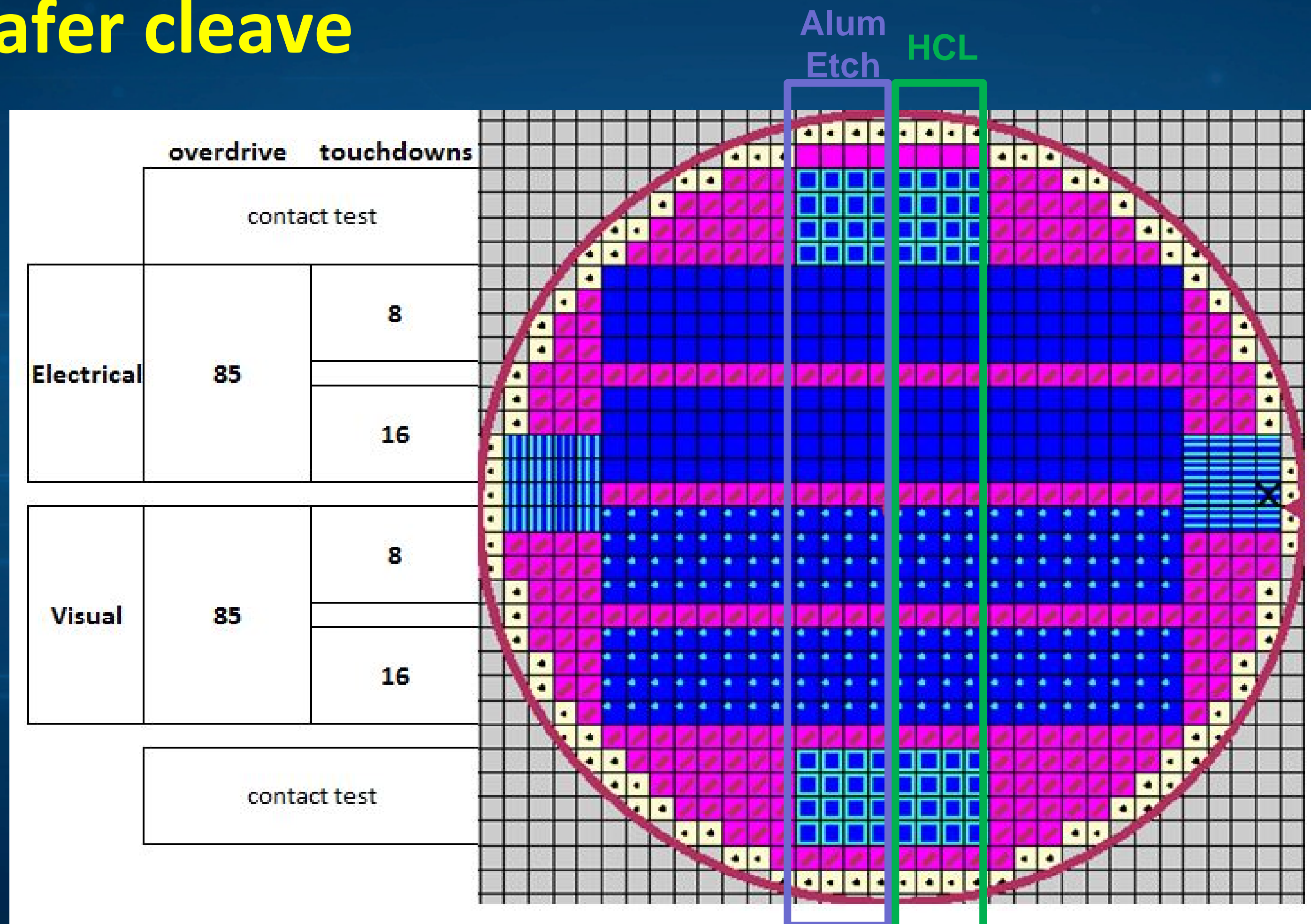
	Electrical 08	Electrical 16	Visual 08	Visual 16
Electrical 08	-0.11274	-0.09274	0.07851	0.14226
Electrical 16	-0.09274	-0.11274	0.05851	0.12226
Visual 08	0.07851	0.05851	-0.11274	-0.04899
Visual 16	0.14226	0.12226	-0.04899	-0.11274

Chemical Etch Detection

- **What is the best method to detect ILD cracking**
- **2 methods explored**
  - Aluminum etch solution
  - HCL solution
- **Setup of wafer for chemical etch:**
  - Cleave wafer in center (4 pieces total) to allow for 2 different chemical etch solutions to be reviewed on 4 full die array
  - Submit each center section for chemical etch
  - Document pictures of same pads between each etch solution

Chemical etch Setup

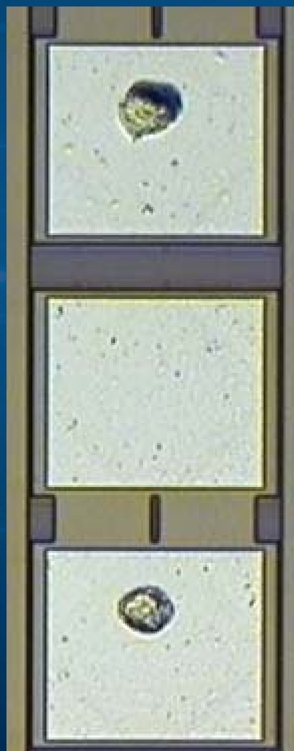
Wafer cleave



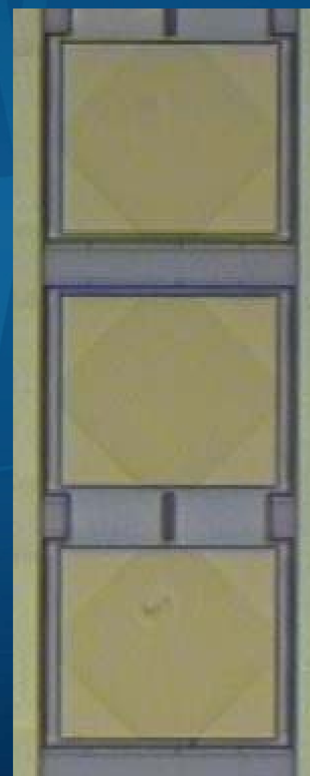
Note: Prober movement is Serpentine

Chemical Etch Examples

- Aluminum etch examples
  - Scrub Examples

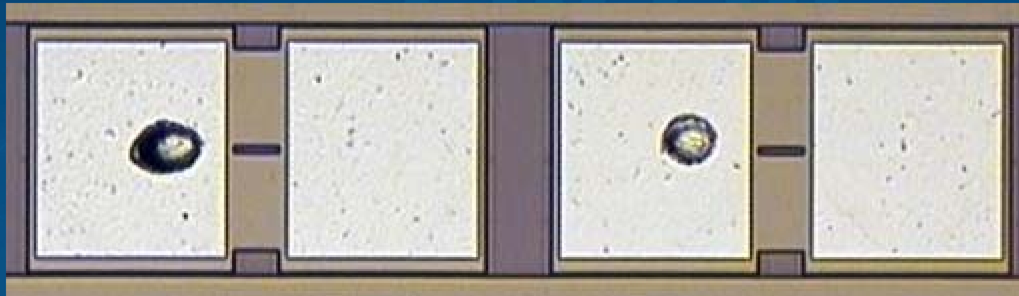


- Aluminum etch



Chemical Etch Examples

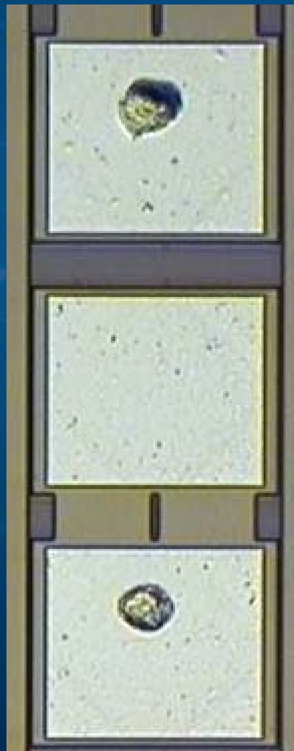
- Aluminum etch examples
  - Scrub Examples



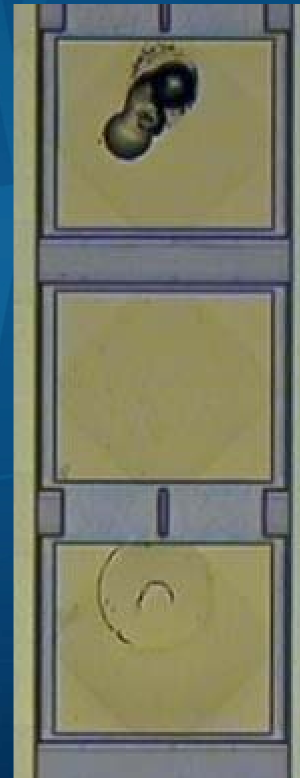
  - Aluminum etch

Chemical Etch Examples

- HCL examples
  - Scrub Examples

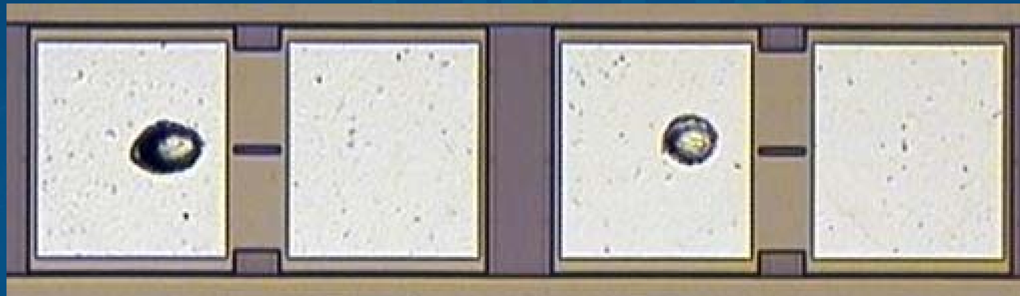


- HCL etch

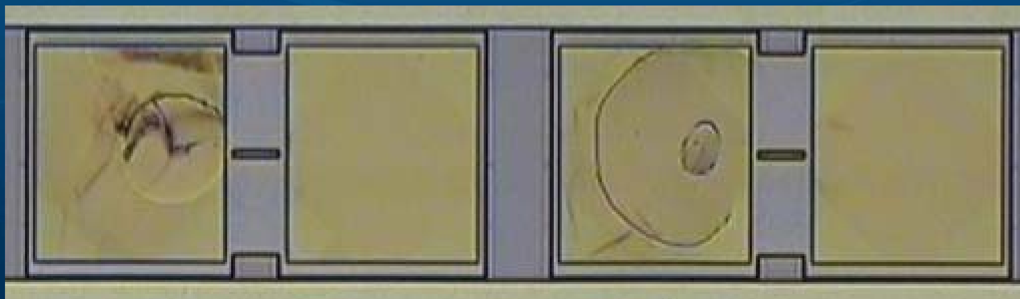


Chemical Etch Examples

- HCL examples
  - Scrub Examples



  - HCL etch



Chemical Etch Detection

- **Results from ILD inspection:**

Probe Temperature 25C
Inspected by Jeff Reeves and Jory Twitchell

Platform	Probe Technology	Probe Setup Method	Probe Stresses		ILD Results	
			Overdrive	Touchdowns	Die Inspected	Failed
J750	3.0mil cobra	Electrical	85	8	24	9
				16	24	25
		Visual		8	24	69
				16	24	113

Conclusion

- **The electrical contact methodology provides more accurate results for "real world" testing.**
  - The probe mark depth between electrical and visual setups can range as high as 0.2 microns in depth
  - Electrical takes out the variability which can occur between probe sites
- **HCL chemical etch is more effective for indentifying the ILD damage than aluminum etch**
  - Damage is visible when using the aluminum etch but requires a more careful inspection of pads
  - Damage is more easily indentified with the HCL solution.

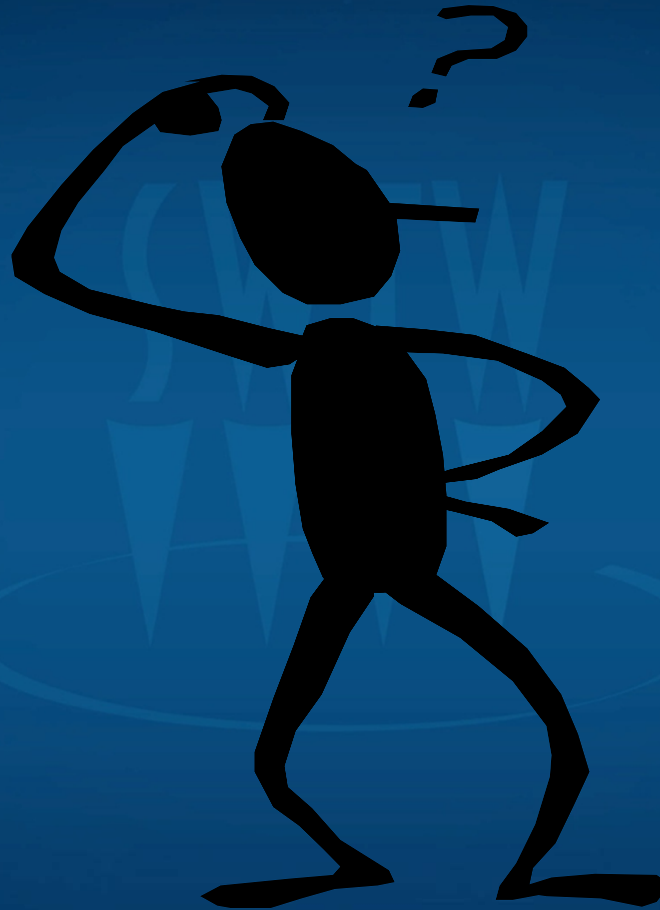
Follow - Up

- **Follow – up work to be completed**
  - Best probe card parameters (cantilever and vertical probe cards) for sensitive ILD layers at hot and cold temperature probing
  - Probe card tip diameters affect sensitive ILD layers more at hot and cold temperature probing than room temperature probing

Acknowledgments

- SW Test Workshop for opportunity to present
- Freescale colleagues at Oak Hill and Chandler for procedures and FA analysis

Q&A



Monday, June 9, 2014

10:30 AM to Noon – = † = u
= # u

Cost Effective 1,000V High Voltage Parametric Test Technique

Yoichi Funatoko and Nobuhiro Kawamata (FormFactor - Japan)
Takeki Andoh and Norio Ishibiki (Texas Instruments - Japan)

High pulsed current wafer probing in high temperature conditions: comprehensive framework for vertical and cantilever probe design

Daniele Acconcia, Dr. Emanuele Bertarelli,
Raffaele Vallauri, and Riccardo Vettori (Technoprobe SPA - Italy)

A Study on CCC of fine pitch vertical probe; Simplified CCC formula and its verification

Dr. Sanghun Shin, Jong-hyeon Park,
Kang Dae Lee, and Jae Hoon Park (Will Technology - Korea)