Are You Really Going to Package That?

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Outline

• Situation
• Cost of Test
• New Paradigm
• Probe Card Cost Drivers
• Computational Evolution
• New Approaches
• Conclusion
Increasing Wafer Probe Count

Probe Count, K

Number of Probe Points / Touchdown - SoC
Number of Probe Points / Touchdown - MPU/ASIC

30K @ 80 µm pitch
SWTW

80 K
Wafer Level Chip Scale Packaging

**WL-CSP (Wafer Level CSP) Process**

- RDL Forming/Encapsulation
- Dicing

**Bad die here**

**End up packaged**

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Fujitsu

June 7-10, 2015

SW Test Workshop
Semi Market Effects on ATE

- Cost Pressures on test continue

\[
\text{CoT} = \frac{\text{Yield} \times \text{Utilization} \times \text{Throughput}}{\text{Capital Costs}\text{\^{}}\text{\text{\textsubscript{Lifetime}}} + \text{Variable Costs} + \text{Overhead}}
\]

- ATE Impact on COT model

[References: Frazier13]
Capital Costs

CoT = \frac{\text{Yield} \times \text{Utilization} \times \text{Throughput}}{\text{Capital Costs} \over \text{Lifetime}} + \text{Variable Costs} + \text{Overhead}

# of sites = m

- Tester Pin Zero (Infrastructure)
- Tester Electronics \(x\)/site or pin
- Wafer Prober or Handler
# of sites = m

<table>
<thead>
<tr>
<th>Total</th>
<th>Per Site</th>
</tr>
</thead>
<tbody>
<tr>
<td>TPZ</td>
<td>TPZ/m</td>
</tr>
<tr>
<td>$x/site * m = x * m</td>
<td>x</td>
</tr>
<tr>
<td>WP</td>
<td>WP/m</td>
</tr>
</tbody>
</table>

[Rivoir03]
# Example Calculation

The table below shows the cost per site for different infrastructure and equipment options, given different numbers of sites. The cost decreases as the number of sites increases.

<table>
<thead>
<tr>
<th></th>
<th>$m = 1$</th>
<th>$m = 8$</th>
</tr>
</thead>
<tbody>
<tr>
<td>Tester Pin Zero (Infrastructure)</td>
<td>$250, \text{K}$</td>
<td>$31.25, \text{K}$</td>
</tr>
<tr>
<td>Tester Electronics $x$/site or pin</td>
<td>$50, \text{K}$</td>
<td>$50, \text{K}$</td>
</tr>
<tr>
<td>Wafer Prober or Handler</td>
<td>$300, \text{K}$</td>
<td>$37.5, \text{K}$</td>
</tr>
<tr>
<td>COST PER SITE</td>
<td>$600, \text{K}$</td>
<td>$118.75, \text{K}$</td>
</tr>
</tbody>
</table>
Performance vs. Cost

Test Cell cost/DUT

Number of DUTs in parallel

High Performance
High Pin-Count DUT

Low Performance
High Pin-Count DUT

Low Performance
Low Pin-Count DUT
Variable Costs

+ NRE + spares!

Probe Card or Socket + Load board

Power Consumption

Test Development

CoT =

Yield * Utilization * Throughput + Variable Costs + Overhead

Capital Costs

Lifetime

Cleaning Media

Probe Card or Socket Repair

Operator Labor

Handler Change Kit

e etc...
New Paradigm

Variable Costs >> Capital Costs
over life of test cell

Example: single Probe Card > Tester Cost
(often so expensive that they are being capitalized!)
Typical Probe Card Cost Drivers

• Linear
  – Number of probes (for singulated technology)

• Slightly more than linear
  – Number of holes to be drilled (for singulated technology)
  – Low force probe technology

[Feldman11]
Typical Probe Card Cost Drivers

- **Non-linear (some area & some exponential)**
  - Mechanical elements
    - Increased force
    - Larger area for co-efficient of thermal expansion (CTE) match
  - Active area
    - Larger space transformer (more layers?) & interposer
    - Larger PCB (plating variance across area, tight pitch issues)
    - Probe head (photolithographic processes w/defect density)
  - Printed Circuit Board (PCB)
    - Size & layer count
    - Advanced materials
  - High frequency / high bandwidth challenges
Operational Issues Too

• Supply related
  – Cycle time to build probe card
  – Higher cost of “spares”
  – Higher repair cost if head cannot be repaired

• Operational
  – Decreased step pattern efficiency
  – All die on touchdown are limited by longest test time
    • Adaptive test limitations
    • Costly for low yielding wafers
    • Retest is costly
  – Longer metrology times

[Leong14]
[Wegleitner13]
Other Issues...

- Site to site correlation – not copy exact
- Slower to reach “economies of scale”
  - fewer copies ordered on multisite
- Increased investment for slight increases in capacity
- Will probe cards scale to 450 mm? [Feldman12]
- Testing of 2.5/3D die stacks [Feldman13]
Computational Evolution

Time & Increasing Performance

IBM System/360 - computerhistory.org

IBM 5150 - Wikimedia / Zarek

Facebook.com/PhoneDesigner

datacenterknowledge.com
Simplified Die Handling?
‘PEZ’ Nano-Tester

“Contactor” / Probe Head

Load Board 6” (150 mm) sq. ?

INPUT  PASS  FAIL

Handling & Active Thermal

Electronics & Power Supplies
Introducing High Density Modular Test (HDMT)

- **Common Architecture**
  - Fast TTM Engineering Module
  - >30 sites with parallel, asynchronous operation in production module

- **Flexible Architecture**
  - Enables standard instrumentation integration (PXI)

- **Low Cost**
  - > 2X Cost improvement over conventional test platforms
Introducing High Density Modular Test (HDMT)
ONE SIZE DOES NOT FIT ALL
Conclusions

• Previous “answers” need to be re-evaluated as boundary conditions change
  – New product requirements and packaging technology will force changes

• Solutions need to be optimized at test cell, factory, and supply chain level
  – Increased ability to build test solutions that fit product mix vs. living with legacy solutions
  – Careful choices need to be made about “plug and play” alternatives

• Capital and Operating budgets need to be balanced and rationalized
Acknowledgements

- Dave Armstrong – Advantest
- Rey Rincon – Freescale
- Jochen Rivoir - Advantest
- Jeff Roehr – Texas Instruments

Plus “Anonymous” at IDM and Fabless...
Thank You!

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Please visit Ira’s blog
www.hightechbizdev.com
References


Fleeman12 - Gary Fleeman, Advantest, “Getting to Known Good Stack”, Silicon Valley Test Workshop, October 2012

Fraizer13 – Mike Frazier, LTX-Credence, “What will Drive the ATE Market beyond 2013?”, SEMICON Singapore 2013
References - continued


Leong14 – Alexander Witting (GLOBALFOUNDRIES), Amy Leong, et. al (FormFactor), “Key Considerations to Probe Cu Pillars in High Volume Production”, IEEE Semiconductor Wafer Test Workshop (SWTW) 2014


Wegleitner13 - Al Wegleitner (Texas Instruments), Tommie Berry (FormFactor), “When Brick Wall is not the best, PART II (A Touch Down Optimization Study)”, IEEE Semiconductor Wafer Test Workshop (SWTW) 2013