SW Test Workshop
Semiconductor Wafer Test Workshop
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Are You Really Going to Package That?

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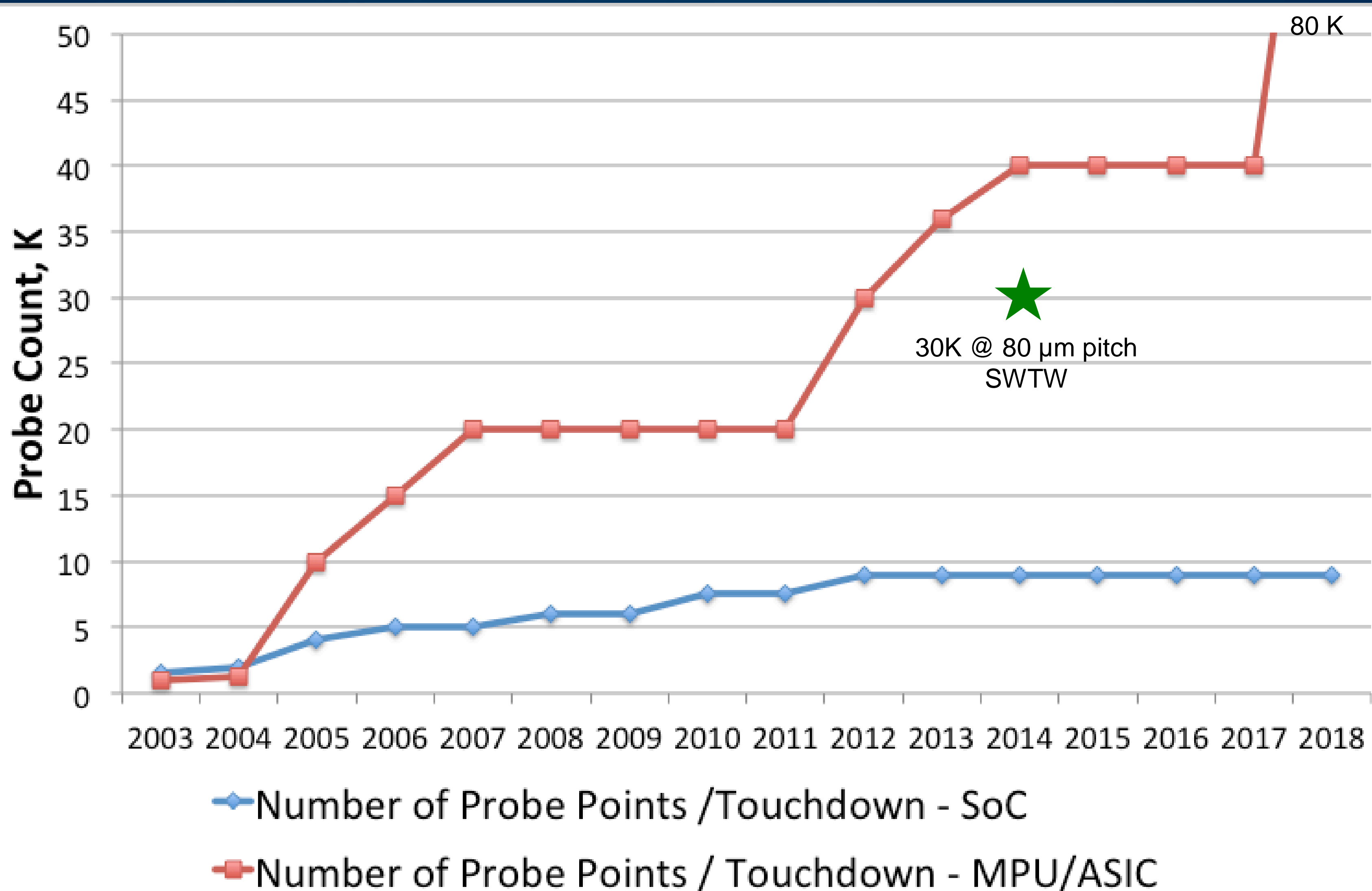
Outline

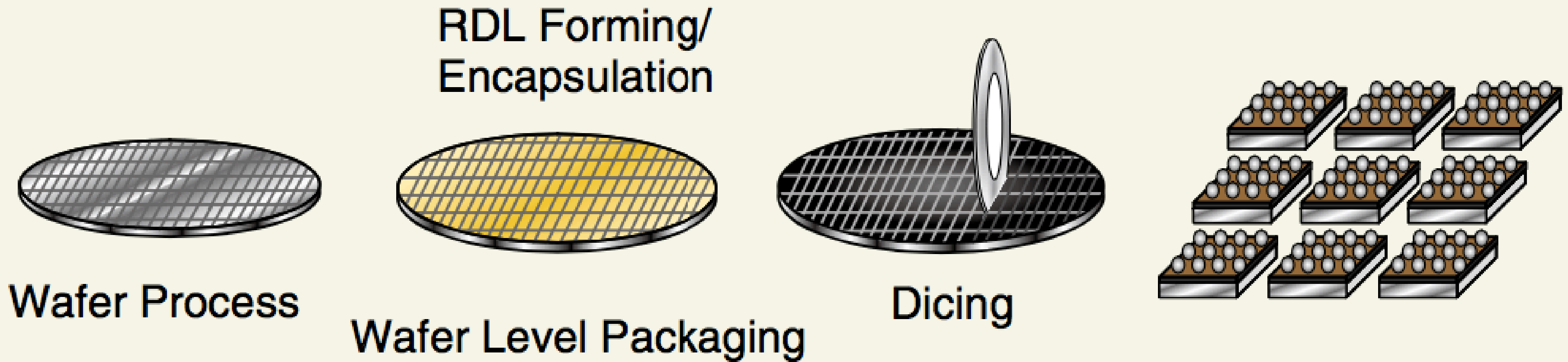
- Situation
- Cost of Test
- New Paradigm
- Probe Card Cost Drivers
- Computational Evolution
- New Approaches
- Conclusion

Increasing Wafer Probe Count



[ITRS]

Wafer Level Chip Scale Packaging



Fujitsu

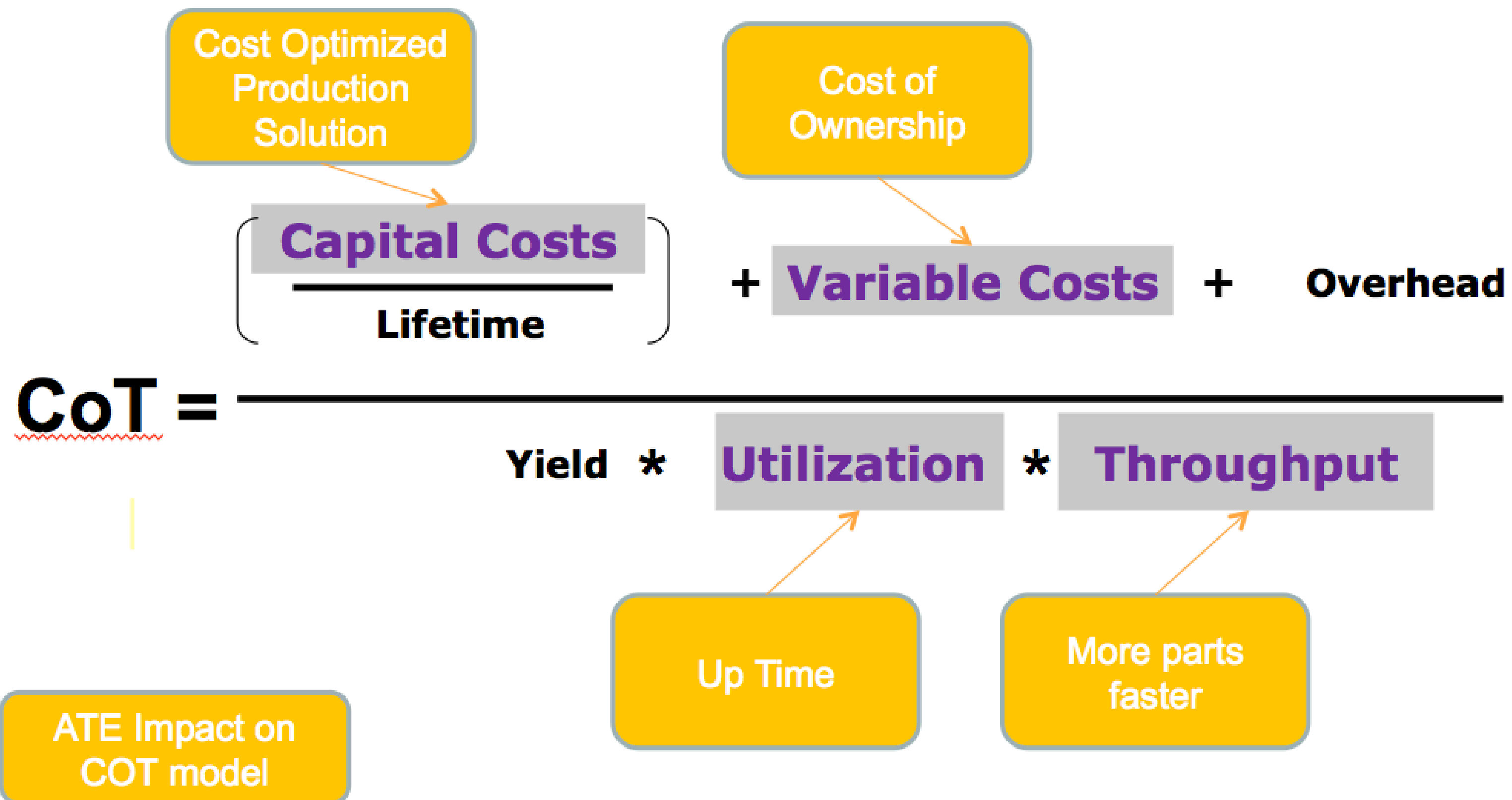
Bad die here

End up packaged

Semi Market Effects on ATE

semi

- Cost Pressures on test continue



[Frazier13]

Capital Costs

Tester Pin Zero (Infrastructure)

Tester Electronics $x/site or pin

Wafer Prober or Handler

$$CoT = \frac{\left(\frac{\text{Capital Costs}}{\text{Lifetime}}\right) + \text{Variable Costs} + \text{Overhead}}{\text{Yield} * \text{Utilization} * \text{Throughput}}$$

# of sites = m

Usual Math...

of sites = m

	Total	Per Site
Tester Pin Zero (Infrastructure)	TPZ	TPZ/m
Tester Electronics $x/site or pin	$x/site * m = x * m	x
Wafer Prober or Handler	WP	WP/m

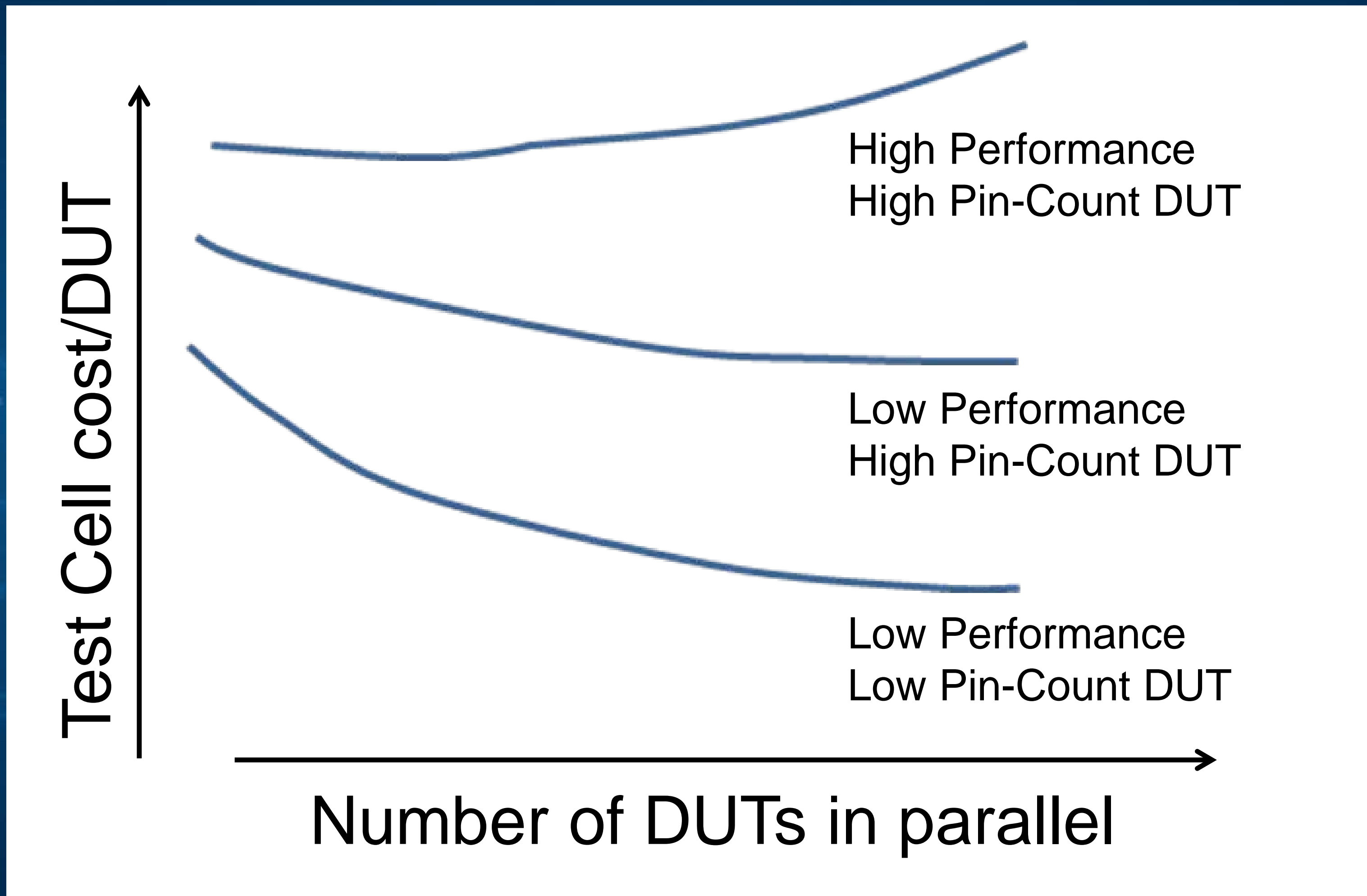
[Rivoir03]

Example Calculation

of sites = m

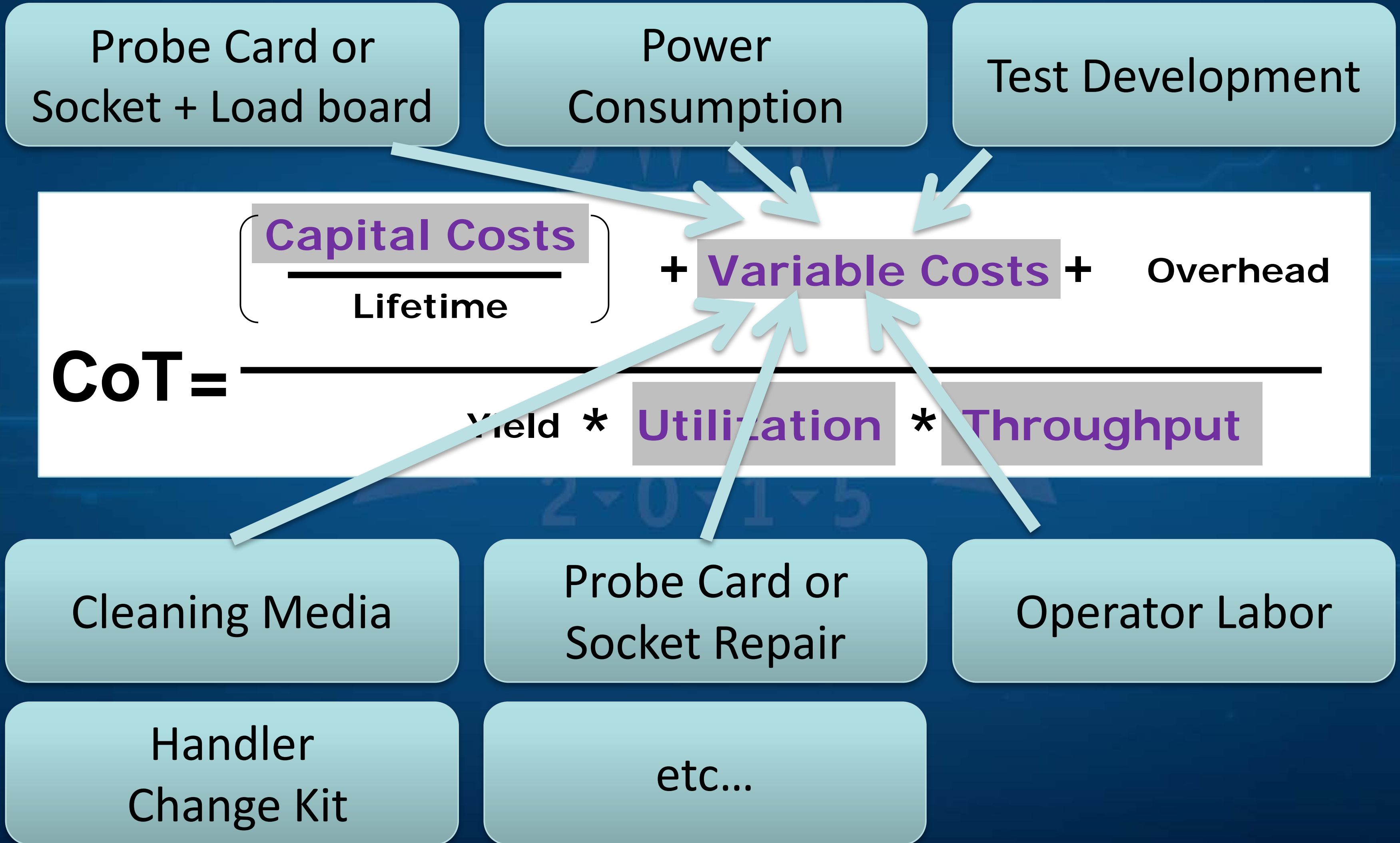
	m = 1	m = 8
Tester Pin Zero (Infrastructure)	$250 K	$31.25 K
Tester Electronics $x/site or pin	$50 K	$50 K
Wafer Prober or Handler	$300 K	$37.5 K
COST PER SITE	$600 K	$118.75 K

Performance vs. Cost



Variable Costs

+NRE + spares!



New Paradigm

Variable Costs >> Capital Costs

over life of test cell

Example: single Probe Card > Tester Cost

(often so expensive that they are being capitalized!)

Typical Probe Card Cost Drivers

- **Linear**
  - Number of probes (for singulated technology)
- **Slightly more than linear**
  - Number of holes to be drilled (for singulated technology)
  - Low force probe technology

[Feldman11]

Typical Probe Card Cost Drivers

- **Non-linear (some area & some exponential)**
  - Mechanical elements
    - Increased force
    - Larger area for co-efficient of thermal expansion (CTE) match
  - Active area
    - Larger space transformer (more layers?) & interposer
    - Larger PCB (plating variance across area, tight pitch issues)
    - Probe head (photolithographic processes w/defect density)
  - Printed Circuit Board (PCB)
    - Size & layer count
    - Advanced materials
  - High frequency / high bandwidth challenges

[Feldman11]

Operational Issues Too

- **Supply related**
  - Cycle time to build probe card [Leong14]
  - Higher cost of "spares"
  - Higher repair cost if head cannot be repaired
- **Operational**
  - Decreased step pattern efficiency [Wegleitner13]
  - All die on touchdown are limited by longest test time
    - Adaptive test limitations
    - Costly for low yielding wafers
    - Retest is costly
  - Longer metrology times

Other Issues…

- Site to site correlation – not copy exact
- Slower to reach "economies of scale"
  - fewer copies ordered on multisite
- Increased investment for slight increases in capacity
- Will probe cards scale to 450 mm? [Feldman12]
- Testing of 2.5/3D die stacks [Feldman13]

Computational Evolution

datacenterknowledge.com

Time &
Increasing Performance

IBM System/360 - computerhistory.org

IBM 5150- Wikimedia / Zarek

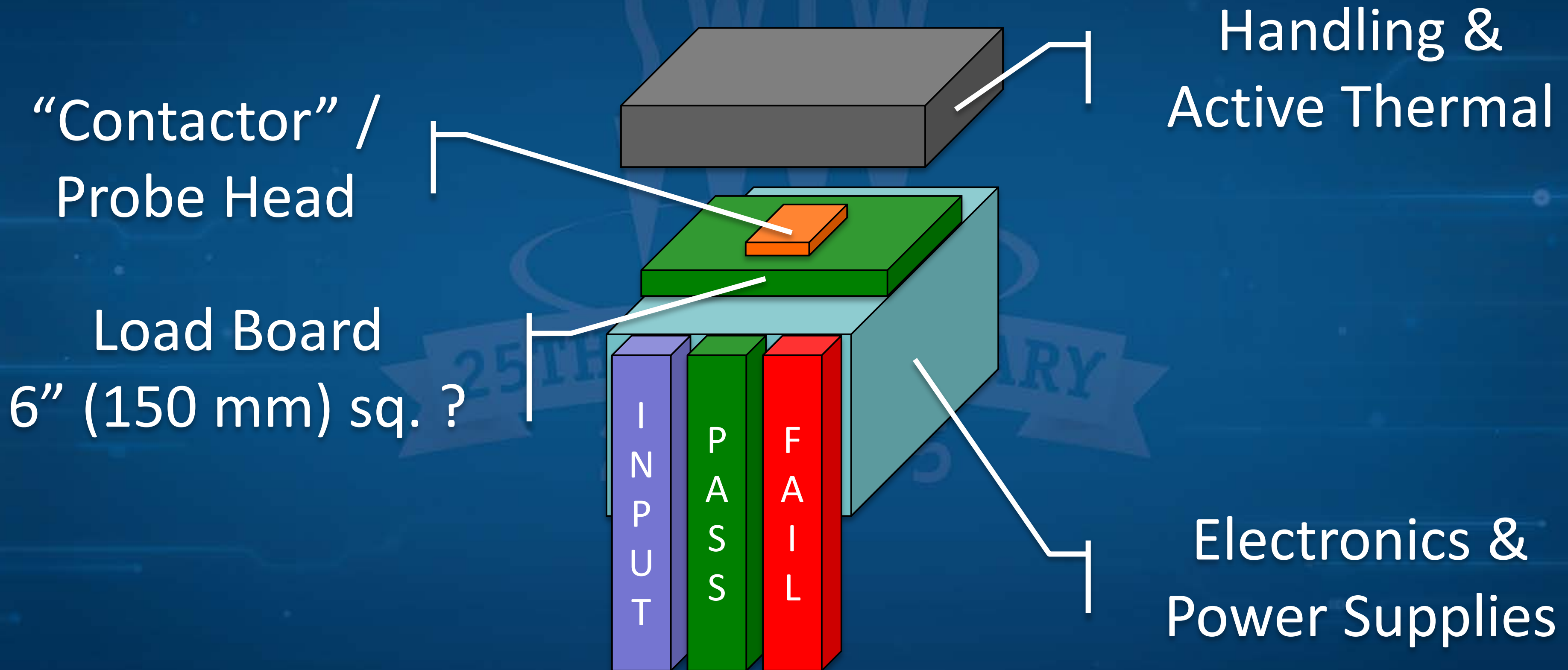
Facebook.com/PhoneDesigner

Simplified Die Handling?

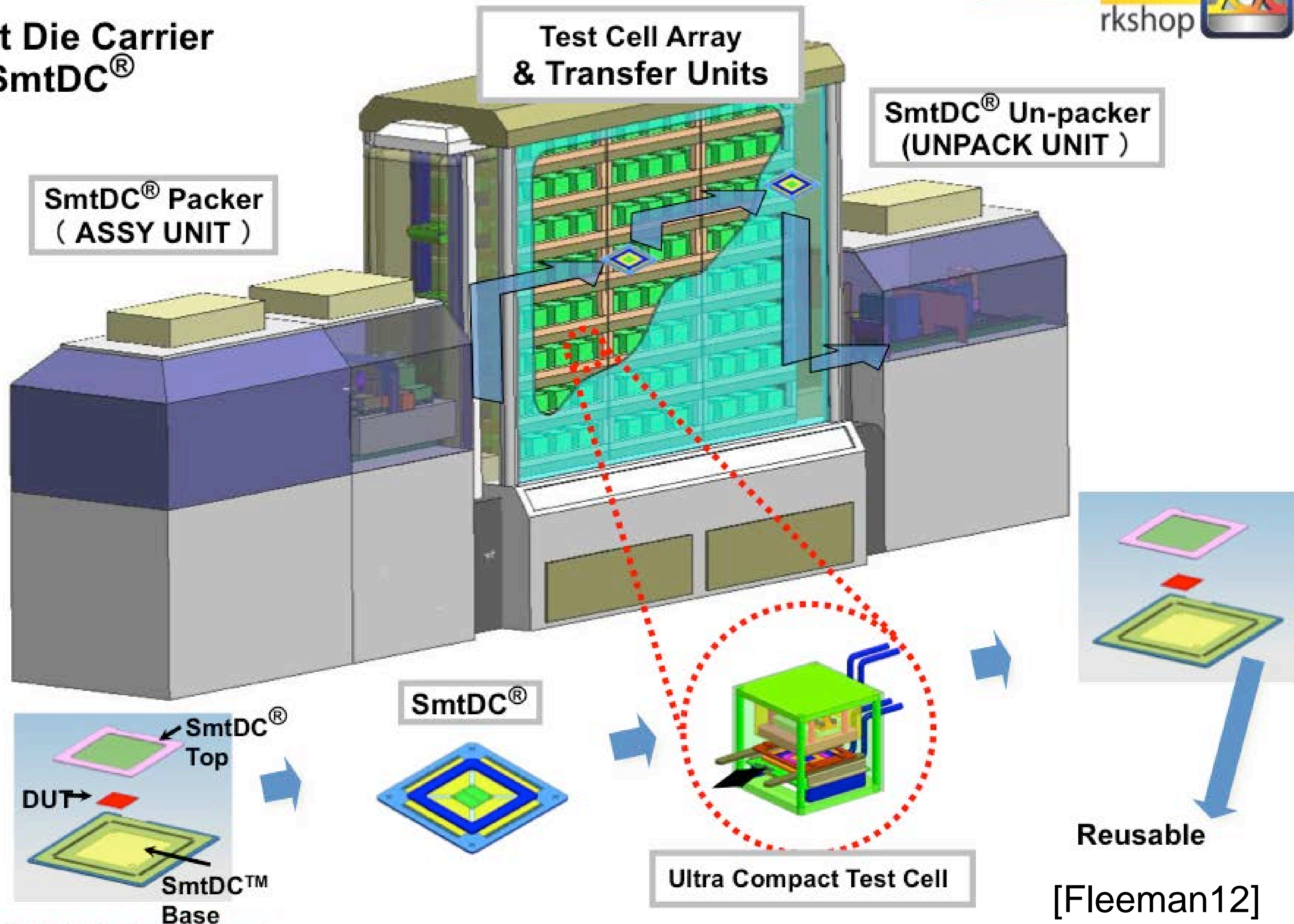
pazumpa.com

20thcenturytoycollector.com

'PEZ' Nano-Tester



HVM Stacked Devices



[Fleeman12]

Intel HDMT

Introducing High Density Modular Test (HDMT)

Engineering Module	Production Module

- **Common Architecture**
  - Fast TTM Engineering Module
  - >30 sites with parallel, asynchronous operation in production module
- **Flexible Architecture**
  - Enables standard instrumentation integration (PXI)
- **Low Cost**
  - > 2X Cost improvement over conventional test platforms

IDF14

Intel HDMT

Introducing High Density Modular Test (HDMT)

n Module

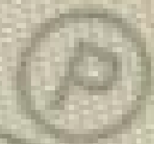
oduction module

orms

IDF14

GB USA MEX

ONE SIZE DOES NOT FIT ALL



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Conclusions

- **Previous "answers" need to be re-evaluated as boundary conditions change**
  - New product requirements and packaging technology will force changes
- **Solutions need to be optimized at test cell, factory, and supply chain level**
  - Increased ability to build test solutions that fit product mix vs. living with legacy solutions
  - Careful choices need to be made about "plug and play" alternatives
- **Capital and Operating budgets need to balanced and rationalized**

Acknowledgements

- Dave Armstrong – Advantest
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- Jeff Roehr – Texas Instruments

Plus “Anonymous” at IDM and Fabless…

Thank You!

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Please visit Ira's blog

www.hightechbizdev.com

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Rikhi14 – Sunit Rikhi, Intel, “Leading at the edge of Moore’s Law with Intel Custom Foundry”, Intel Developer Forum (IDF) 2014

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Wegleitner13 - Al Wegleitner (Texas Instruments), Tommie Berry (FormFactor), “When Brick Wall is not the best, PART II (A Touch Down Optimization Study)”, IEEE Semiconductor Wafer Test Workshop (SWTW) 2013