WLP Probing Technology
Opportunity and Challenge

Clark Liu
PTI Group Overview

- Founded: May/15/97'
- Capital: USD 246 Millions
- Total Assets: USD 2.2B
- Employees: 11,100 (Greatek included)
- Major Services: Chip Probing, Bumping, Packaging, Final Test & Module Assembly
- IPO: 4/3/03' in Taiwan

Group Overview - Business Model

- Vertical integration model to transform wafer to module system
- Well-proven design-in capability & flexible production capacity
Group Overview - Global Network

**China**
- Suzhou Plant
- Xi’an Plant
- Payton in China
- Hsinpu Plant
- HSIP Plant
- HuKou Industrial Park Headquarter
- Chung-Li Plant
- Greatek Electronic

**Southeast Asia**
- Singapore Plant

**Customer Success!!**
Put more resource for next technology!
Probing at 2G Wide I/O Bump Pad

Source: 2011 IEEE _ Samsung
Wafer-level-packages have emerged in many different varieties that can be categorized into different advanced packaging technology platforms.

Source: 2013 SEMI _ Yole
Map of WLP manufacturing companies

Source: 2015 Yole

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WLP Key Connection Technology

Wafer Level Package

Bump
RDL
TSV
CPB
From Kid View!

Wafer Level Package

- Bump like
- RDL like
- TSV like
- CPB like
Electrical Tests for WLP Connectivity

Fault Model

Source: 2010 IEEE 3D IC Workshop _TSMC
# Fault Model for different test items

## Fault Detection of Test Items

<table>
<thead>
<tr>
<th>Test Item</th>
<th>Misalignment</th>
<th>Abnormal Cu pillar</th>
<th>Impurity</th>
<th>Substrate</th>
<th>micro-bump</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
<td>Type 1</td>
<td>Type 2</td>
<td>Type 3</td>
<td>Type 4</td>
<td>Type 5</td>
</tr>
<tr>
<td>Continuity test</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td></td>
<td></td>
</tr>
<tr>
<td>Resistance test</td>
<td>*V</td>
<td>V</td>
<td>*V</td>
<td>V</td>
<td>*V</td>
</tr>
<tr>
<td>Capacitance test</td>
<td>*V</td>
<td>V</td>
<td>*V</td>
<td>V</td>
<td>*V</td>
</tr>
<tr>
<td>Leakage test</td>
<td>*V</td>
<td>V</td>
<td>*V</td>
<td>V</td>
<td>*V</td>
</tr>
<tr>
<td>AC test</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
<td>V</td>
</tr>
</tbody>
</table>

* means need high resolution measurement tool/method

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**Source:** 2010 IEEE 3D IC Workshop _TSMC

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**2015**  
**SW Test Workshop**

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WoW!

Source: Taipei 101
Challenge?
Cost?
Technology?
Opportunity?
New Model?
Cooperation?
Case1: Tools Short Delivery Cycle Time?

- Design Type Out
- Wafer Process
- Wafer Test

4~10 Weeks

MP card

Design Type Out
WLP Process
WLP Test

Gap

Early Plan??
Eng Card??

2~3 Weeks

MP card??
• Bump Type: WLCSP
  – a. Diameter: 300um
  – b. Height: 170um ± 10%
  – c. Pitch: 500um
  – d. TD : 10
  – f. Total Pin Count 2560 Pins

Delivery Time 8 Weeks
Case 2: Process Change for more Chip Probing?

**Exist Process**
- **Wafer Process**
- **Wafer Test**
- **Assembly**
- **Final Test**

**Process X**
- **Wafer Process**
- **Wafer Test (KGD)**
- **WLP**
- **WLP Test**
- **Assembly**

**Process Y**
- **Wafer Process**
- **WLP**
- **WLP Test (KGD)**
- **Assembly**
More WLP Test or More Finial Test?

- WLP Test
  - Fine Pitch
  - Contact Force
  - Silicon Base

- Finial Test
  - Pitch Limit
  - Clean/10K Cleanness
  - Package Base

Pictures Source: Mitsubishi
Wafer Test or Final Test Vendor @ WLP Testing?

- Wafer Test Vendor
- Finial Test Vendor

- Cycle Time Challenge
- Cost Challenge
- New Process Challenge

- Cooperation Model Challenge
- Wafer Level Requirement and Quality

Gap
Ideal Probe Force v.s Over Drive
@ WLP Probing

Probe Force Depend on Material

Electrical All Pass Point

Low Force Keep No Damage

Over Drive Slope Depend on Material

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Case 3: Probe mark analysis Technology

AOI Probe Mark Analysis Challenge

- Probing Position / Depth / Sharp
- Different Layer
- OD / Force / Probe area / Bump Height

- Bump
- RDL
- CPB

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SW Test Workshop
What Expect data from those Probe mark?

Cu Pillar Probe Mark Photo Gallery

Pass
Good Probe Mark on 30um Cu Pillar

No Pass
Misaligned Probe Tip

No Pass
Cu Pillars with Sheared Solder Cap

No Pass
Probe force too high

Data Mining:
(1) Prober Performance
(2)Probe card Performance

[Keep Under Development]

User Expect Data

AOI
Probe mark Analysis

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Case 4: Business or Process Change?

- Chip Design
- Wafer Process
- WL Test
- A.P
- Final Test

- Customer
- Foundry
- OSAT

- WLP Design
- WLP Process
- WLP Test

- Tech
- Cost
- Yield
Same Issue but different site?

Customer

Foundry A

Foundry B

Foundry C

ATE Vendor

Prober Vendor A

Prober Vendor B

Probe card Vendor A

Probe card Vendor B

OSAT A

OSAT B

OSAT C

Gap

Cooperation

Contact

Alignment

Recipe

AOI Vendor

Clean Vendor

Vender

Vender A

Probe card

Vender B
Conclusion

- Cooperation from Customer to Supplier (Design House /Foundry/OSAT/Vender).
- New opportunity for Wafer/Finial Test I/F vender.
- The Evolution Business Model will start change something.