SW Test Workshop
Semiconductor Wafer Test Workshop
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Probe Route Optimization and its effects on the efficiency of test

(Fitting a square peg in a round hole)

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Outline

- Probe Optimization – Why is it needed?
- Objective and obstacles
- Implementing an automated solution
- Enabling Efficiency the tools
- Manufacturing issues and solutions
- Thermal Challenges Identified
- Acknowledgments

Step Optimization – Why is it needed?

- **Need to Reduce Test Cost**
  - Test cost is driven by multiple test insertions (up to 5X) and long test times specifically for flash memory flows.
- **Provide a means for PC design**
  - Complex probe card designs (matrix, skip row / skip column, diagonal) call for more upfront design work to insure optimal efficiency.
- **Improve quality for our customers**
  - Extreme temperatures, multiple insertions, and automotive quality requirements make card technology selection critical for the end product.

Objective

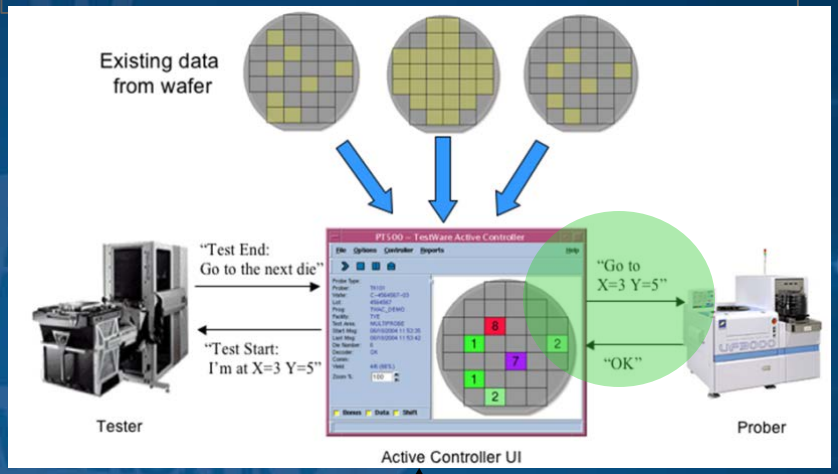
- Challenge: Provide a cost effective means of optimizing the existing probe card library as well as new card designs.
- Show the effects of test time reduction, yield improvement, and probe card life across all technologies.
- Obstacles:
  - Providing an automated route optimizer that could be used across all TI factories.
  - Ensuring all quality checks were met with the introduction of new optimization procedures.
  - Protecting production material and high cost probe cards from thermal expansion and contraction.

Preliminary Architecture - Hardware

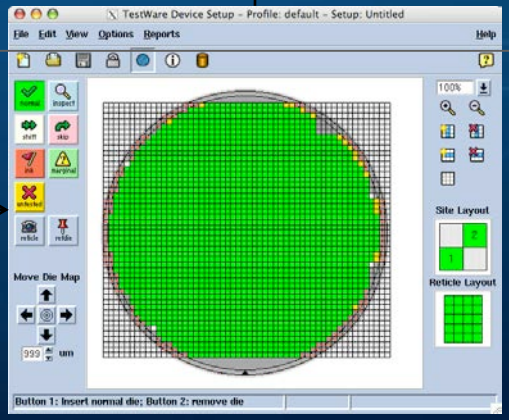
•Centrally supported Windows client that will be used WW by FAB PDE for device setup and tracking process.

Internal Users

Optimized step pattern utilized by TWAC for Test Time Reduction.



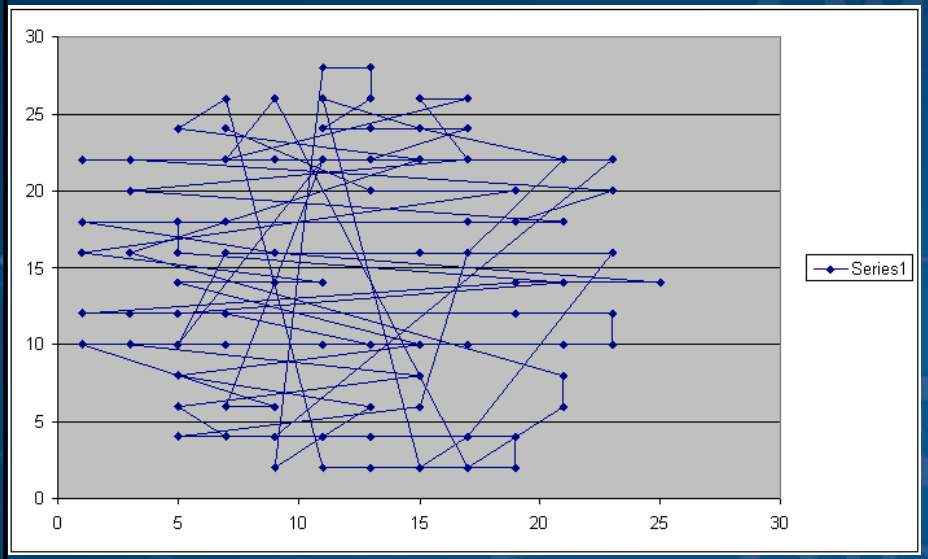
FTP .step file output from optimizer to TWsetup.



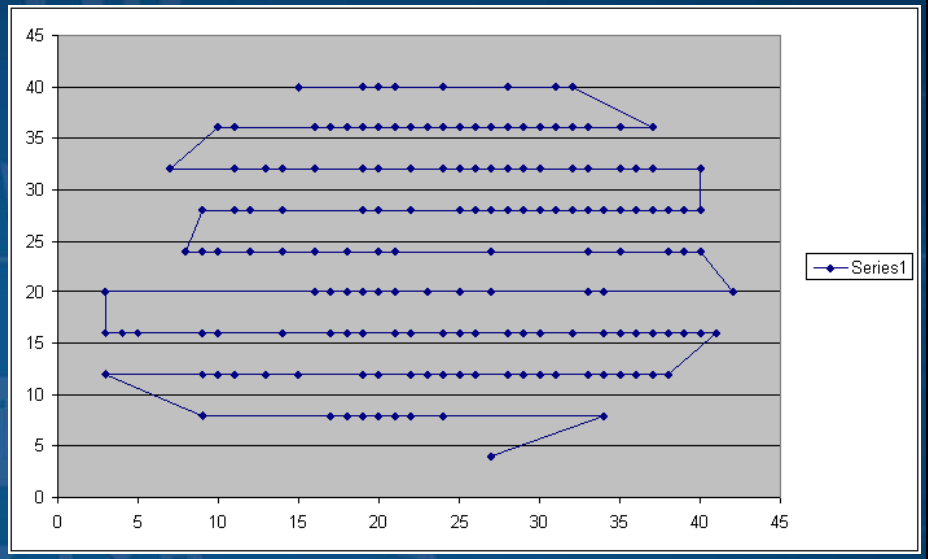
The Beginning: Reduced Reprobe Losses

Immediate Reprobe - Active Control Stepping Improvements

Current IR step method example

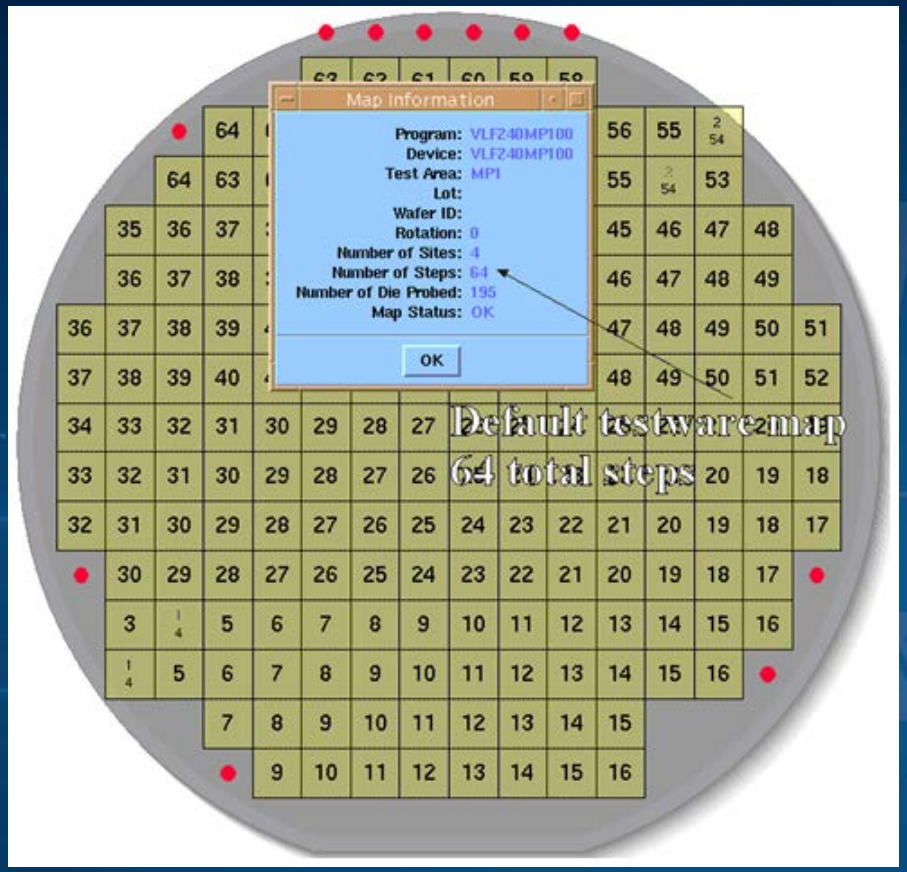


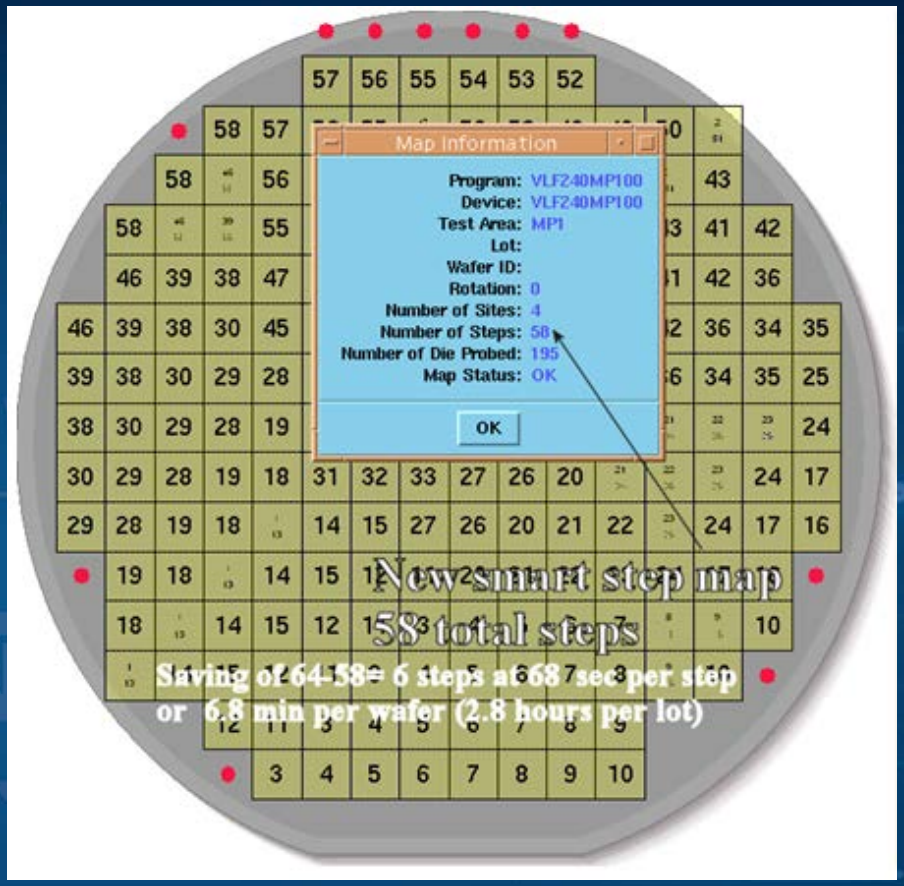
New IR step method example



- **Stepping / Indexing Efficiency greatly improved**
- **Reprobe Test Time reduction ~ 1% (shorter test time devices greater impact)**
- **Eliminated potential for miss-aligned probe due to large prober indexing**

Phase Two: The Smart Step Map





- Test time savings that are simple to implement or back-out
- Enable the user to prevent probe card overhang and the could potentially cause probe card damage
- Best to use on high volume, high test time devices
- Currently does not work with array type probe cards

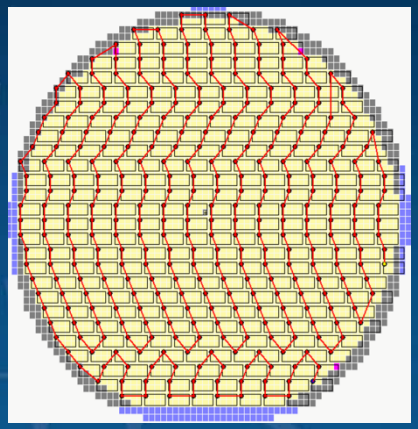
Implementation of Efficiency Tools

Project Description

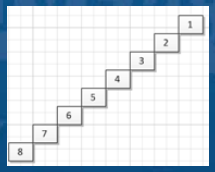
Create, Test, and Release Step Map Optimization for all multi-site devices.

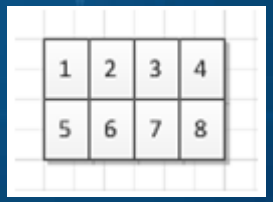
Close & Review

- **2013:**
  - The current TI scripts are not capable of optimizing all potential probe card configurations.
  - Stepping optimization is implemented post PC layout
- **2014:** New Optimizer Capability
  - Allows engineer to optimize card layout
  - Increased UPH
  - Maximize TD efficiency
  - Reduce the cost of test



- Default Pattern
  - 8 site diagonal
- Optimal Pattern
  - 2x4 block
- TD reduction
  - 350 vs. 376 touchdowns
  - 6.9% savings

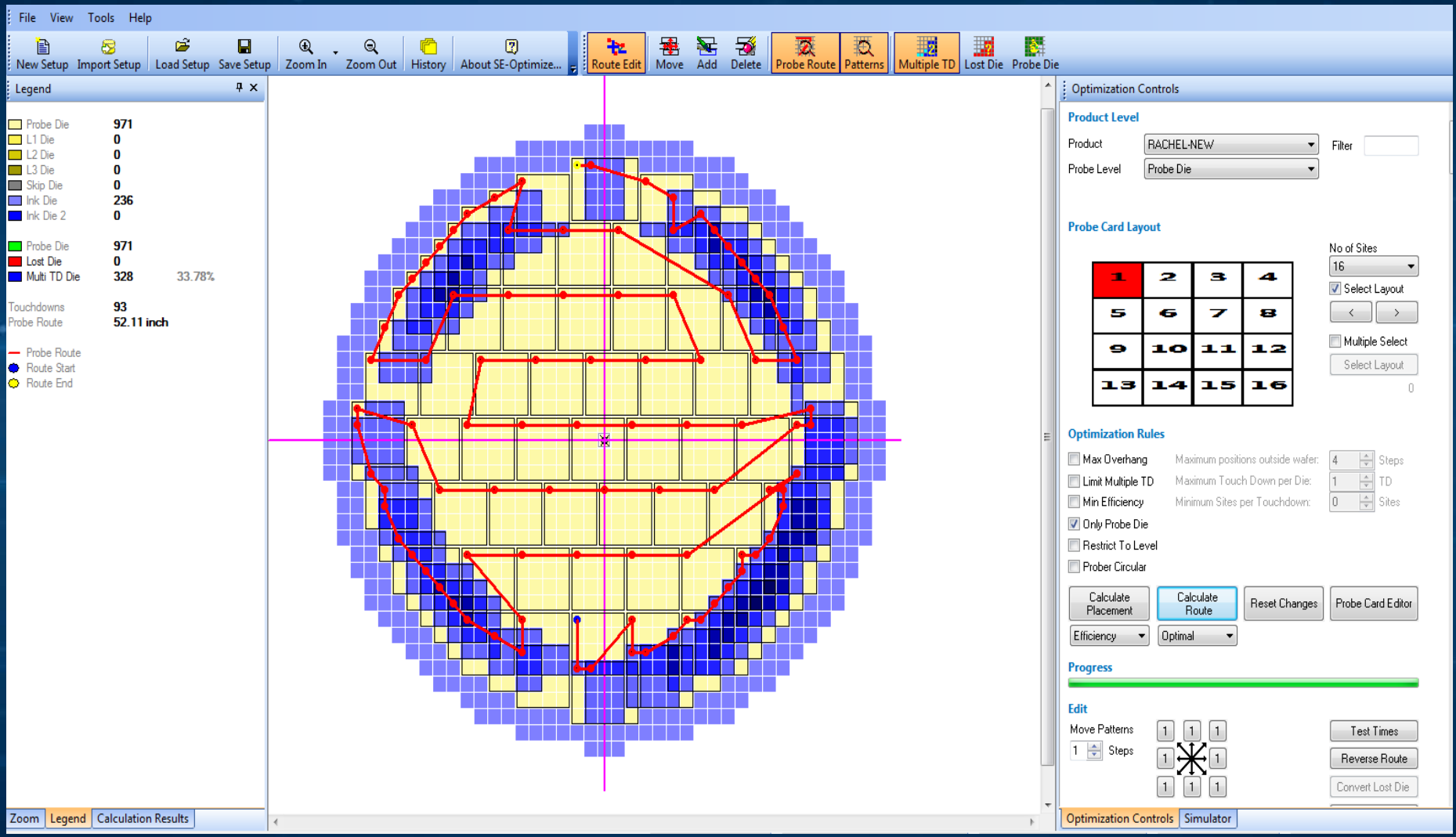




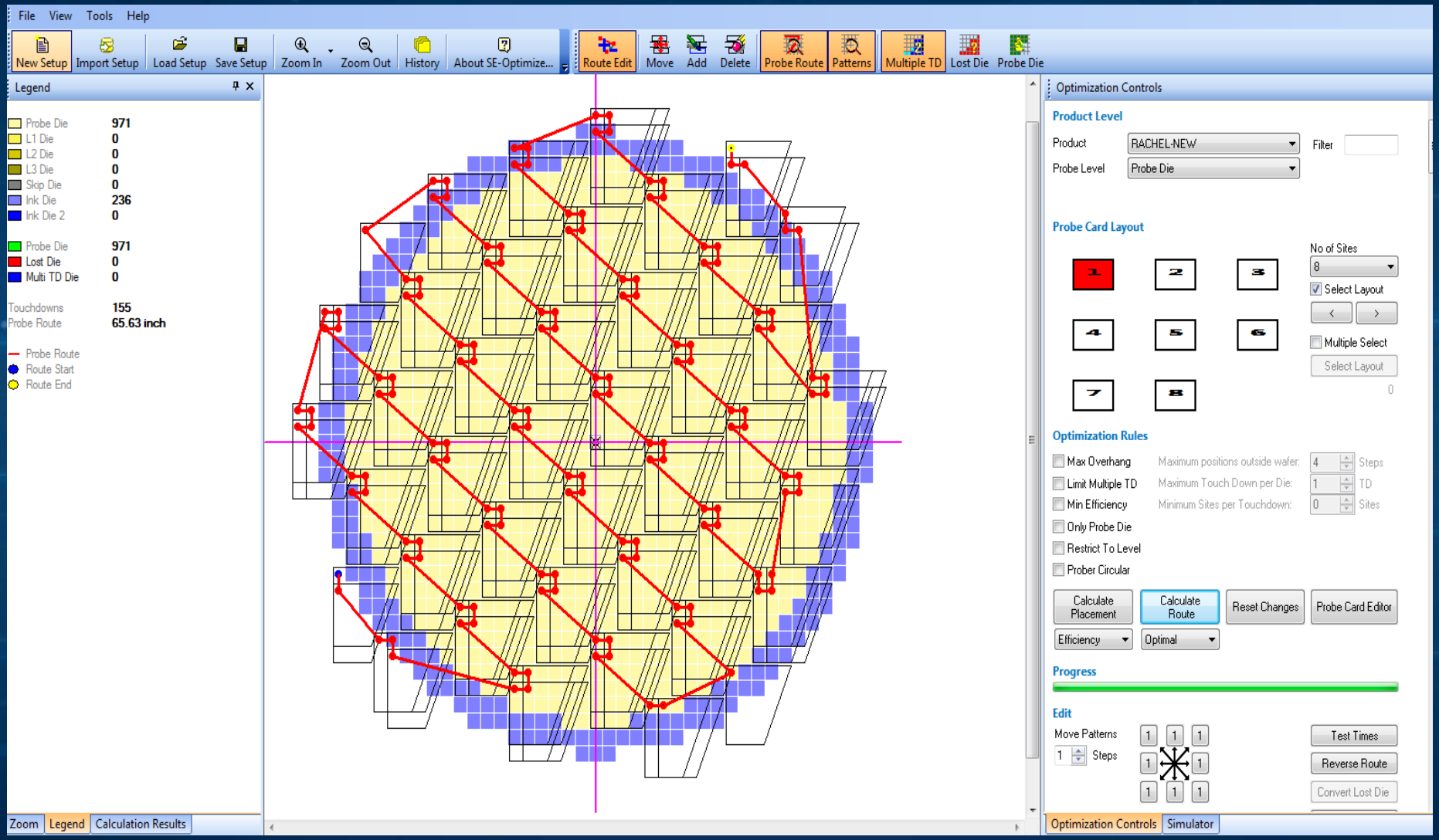
Ongoing WW Efforts

- Work with WW teams to implement optimizer tools across all factories.

Example of Third Party software interface



Example of Skip Row/Column

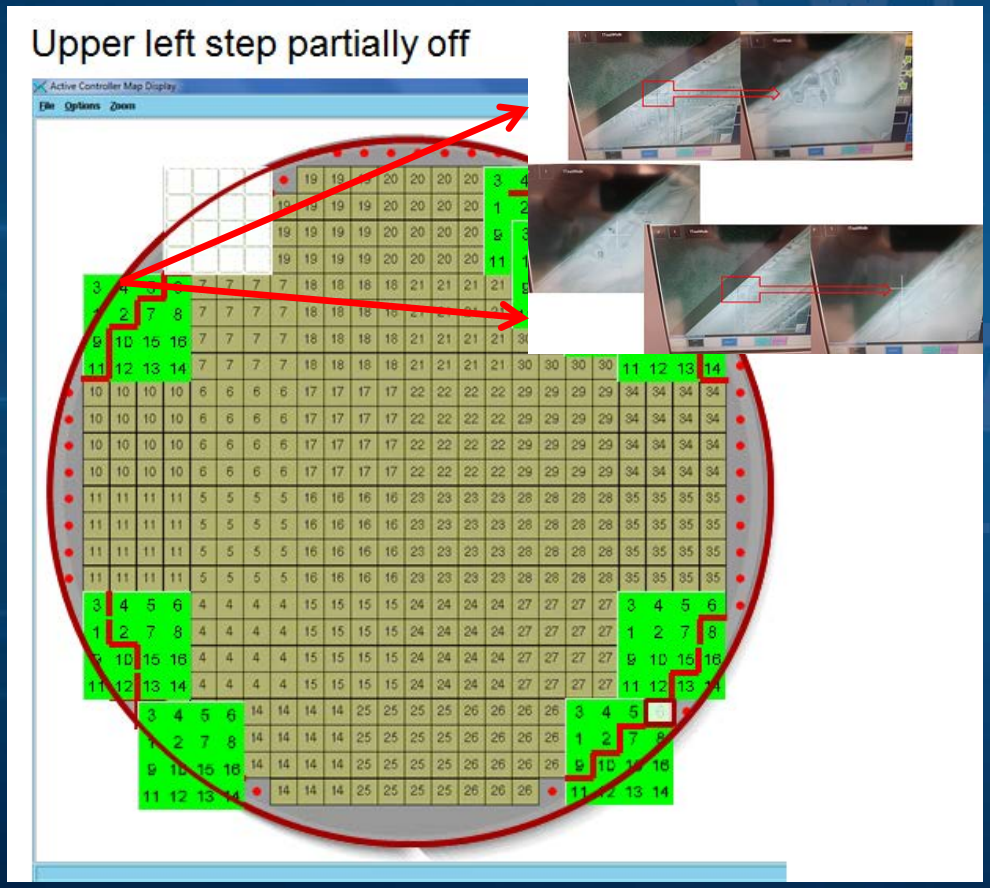


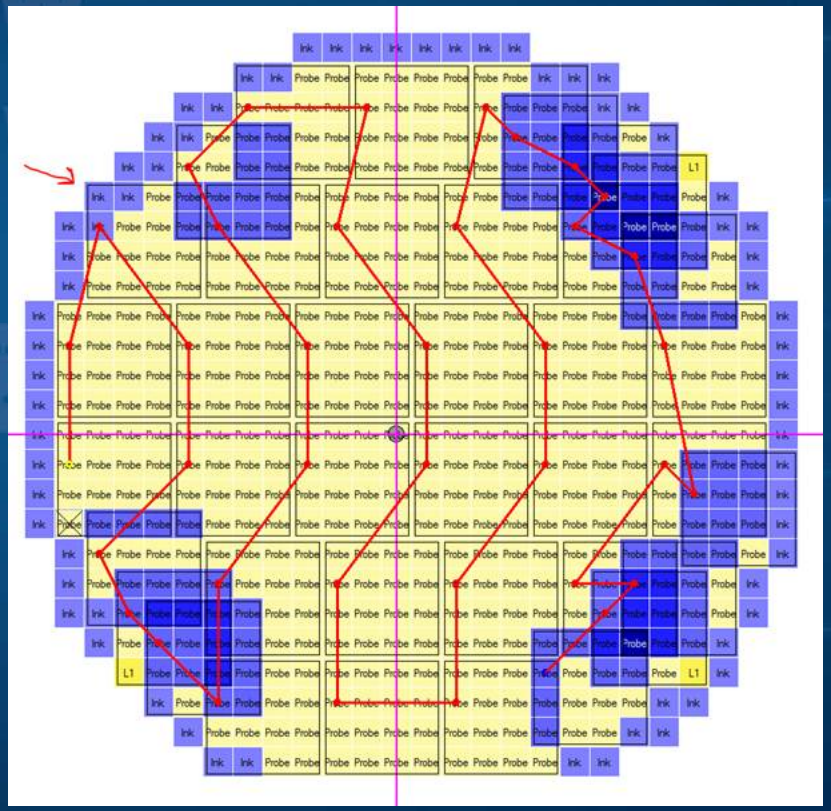
Real World Problems and Robust Solutions

Bent Pin Prevention

Stepping pattern had some steps with sites hitting the edge of the wafer resulting in chronic bent pins

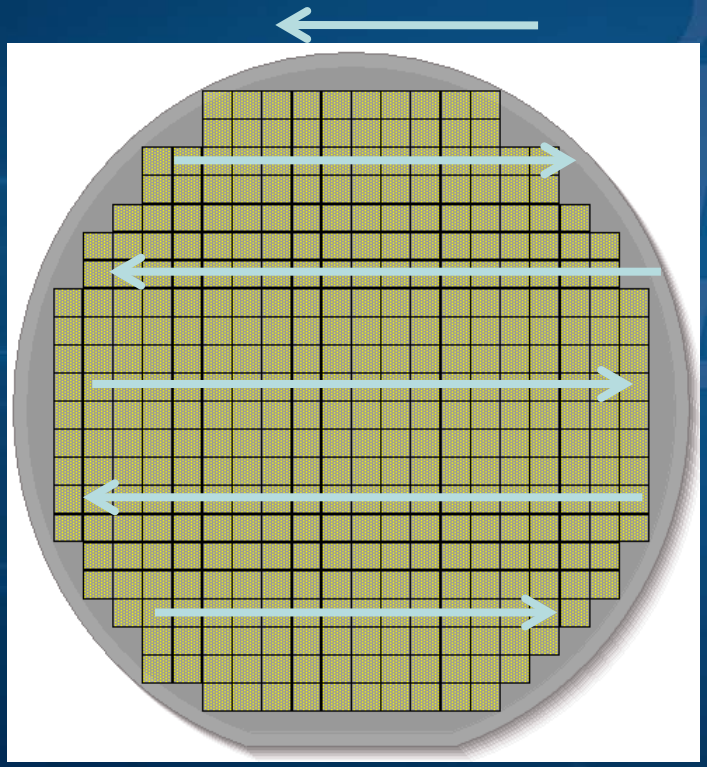
Stepping pattern adjusted to prevent any sites from hitting the edge of the wafer

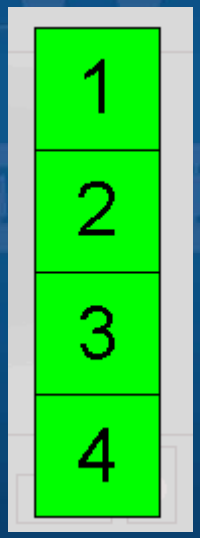




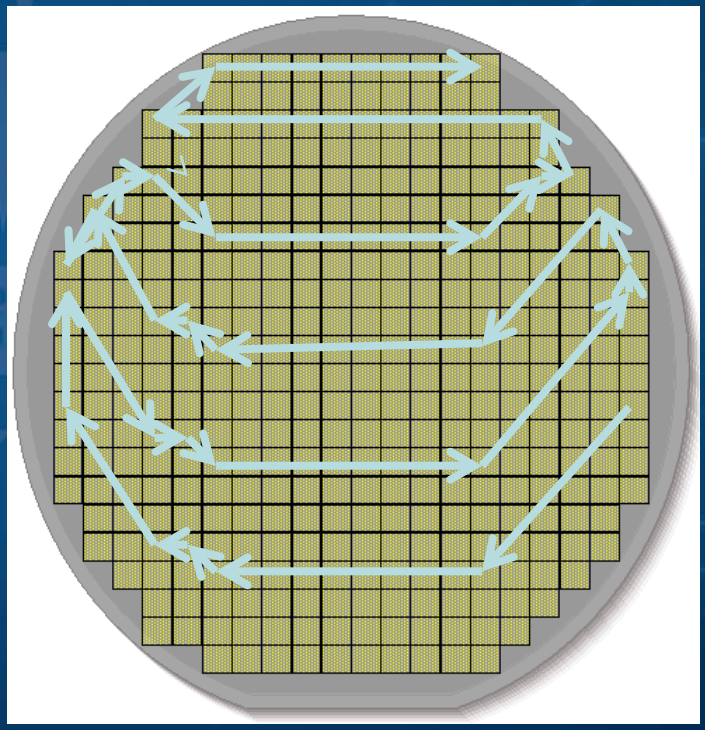
Current process vs. Optimized processes

Probe card steps off wafer using default option



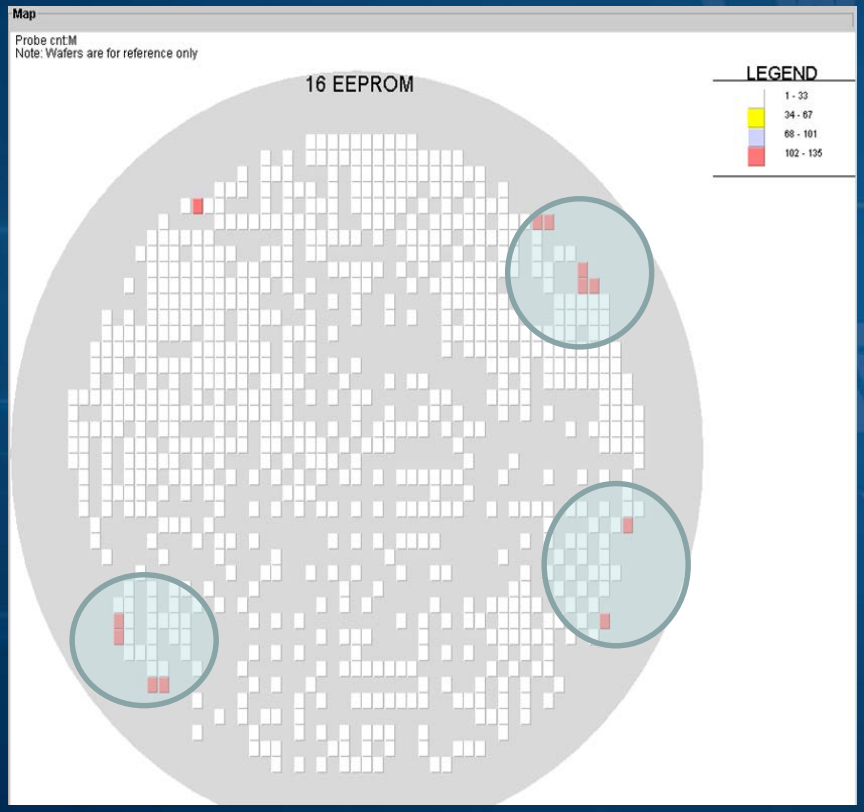


Probe card does not step off wafer

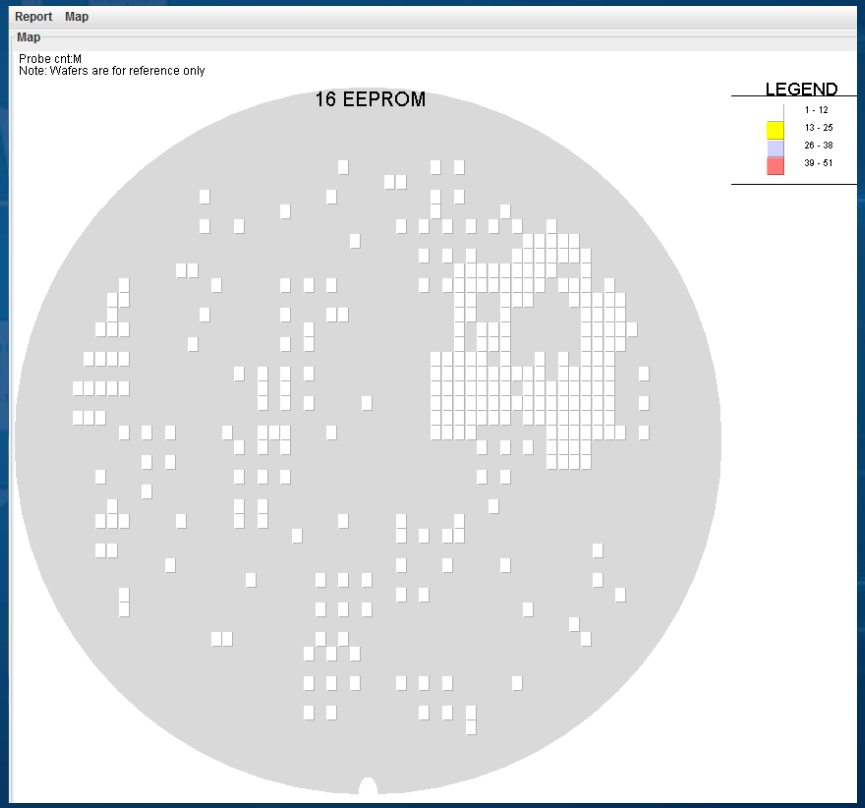


Signature Identification: Not All Die Enabled

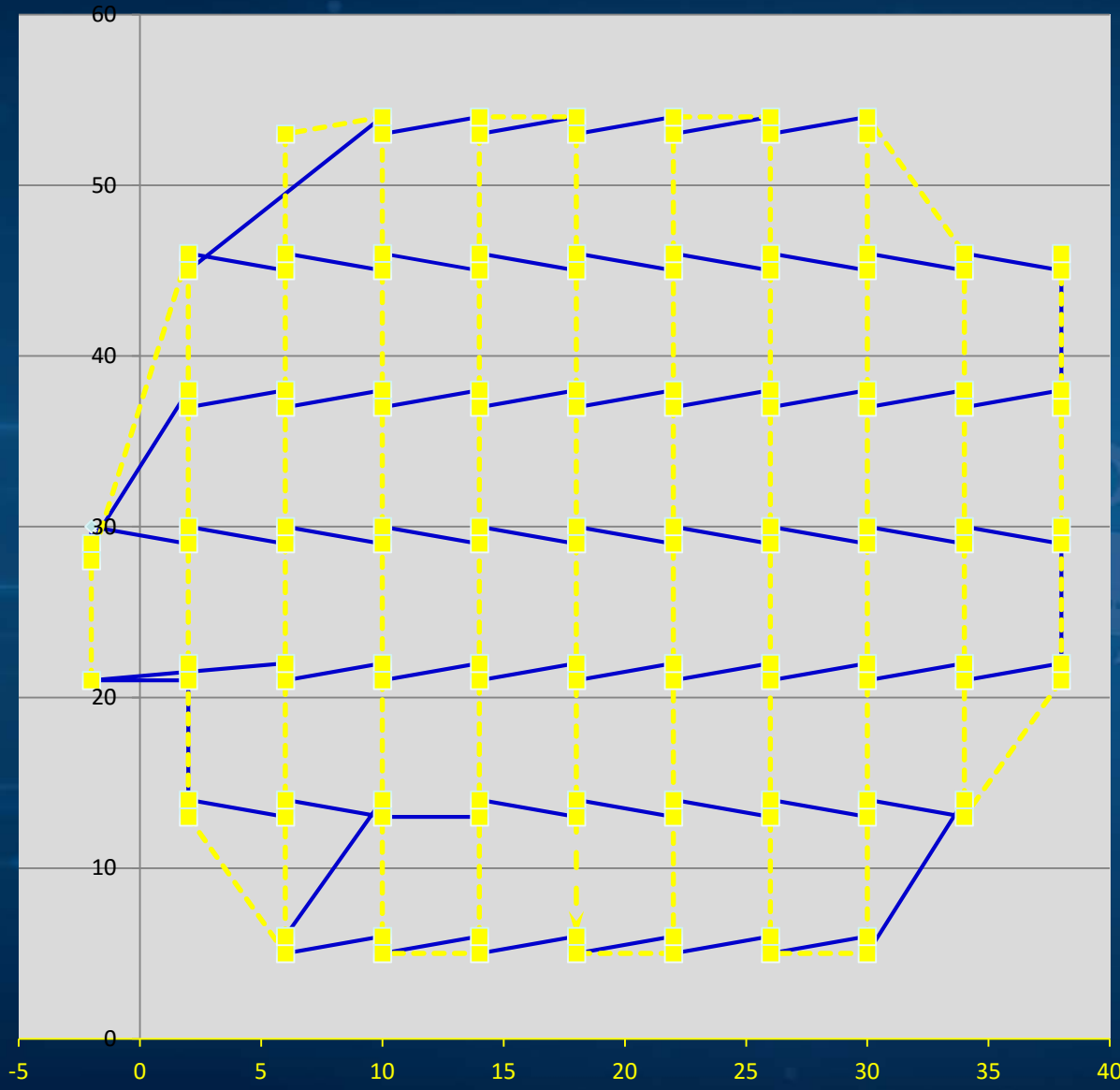
Repeat EEPROM fails



Edge signature identified and resolved



Row-mode vs. Column-mode Probing



- **Implementation resulted in ~1% improvement in AVI losses.**

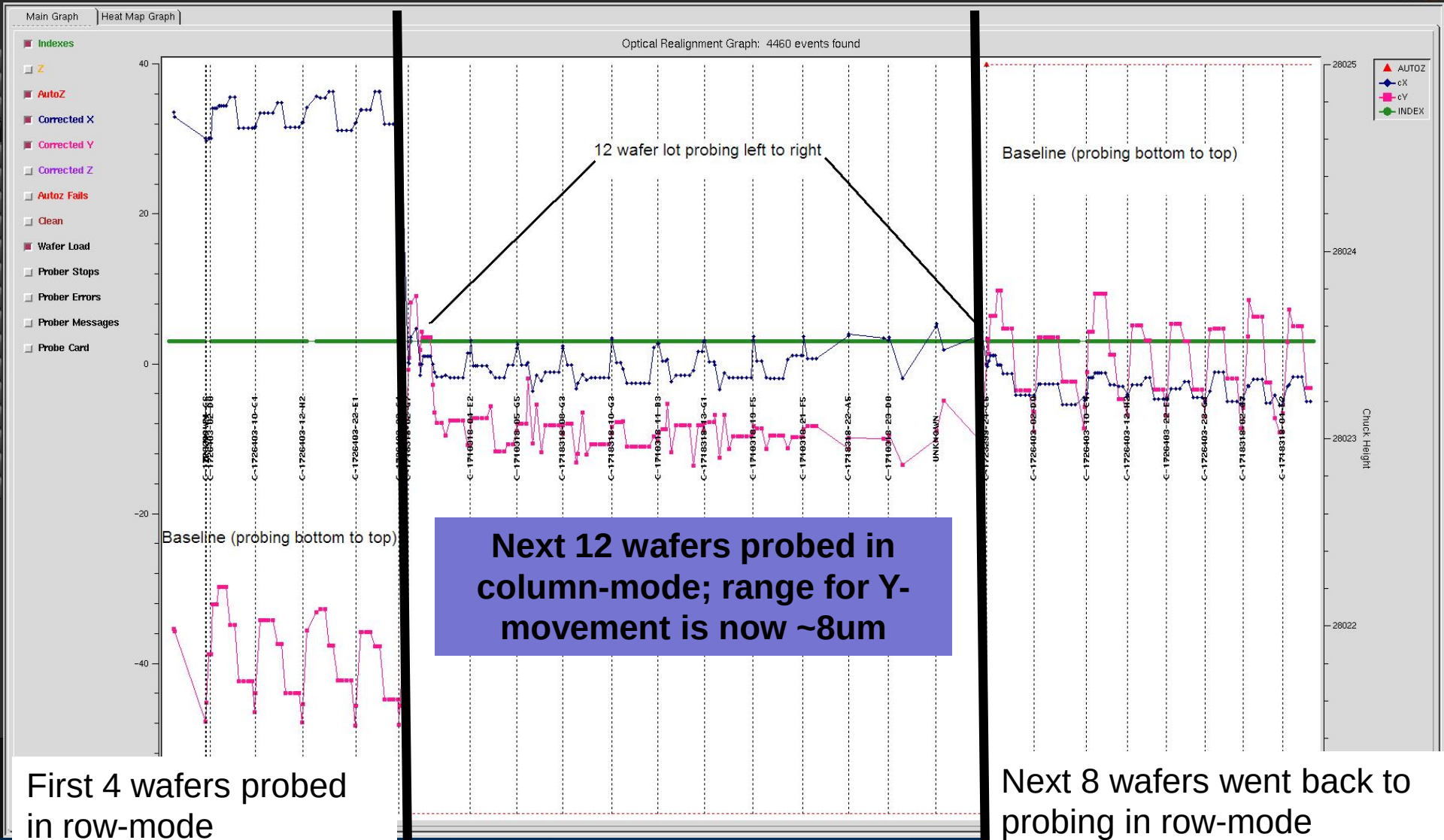
Row-mode (baseline)

Column-mode

{X,Y} stepping coordinates remain unchanged.

Only the order in which {X', Y'} is probed is changed.

Column-mode test study : prober needle movement



First 4 wafers probed in row-mode (baseline); range for Y-movement is ~20um

Next 8 wafers went back to probing in row-mode (baseline); range for Y-movement is back to ~20um

Optimizer Modeling - Database of Layouts and Design for Probe

Probe Card Flow Process Improvement

Problem Description

- DFP needs method to analyze layout efficiency quickly
- BU would like to review multiple site/layout configuration at design

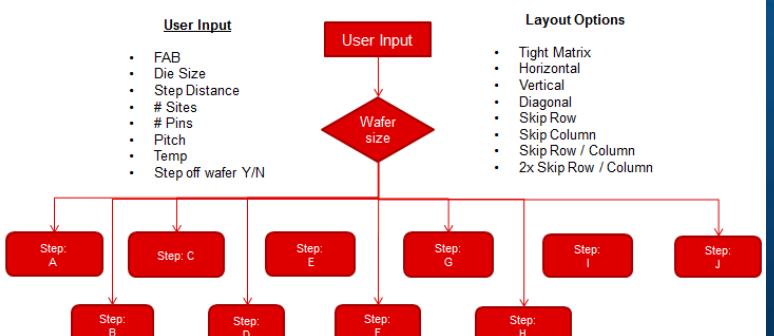
DFP Process Improvement:

- Develop a database of site/layout options for DFP team
- Export standard layouts options.
- Efficiency matrix grouped by top 10 step sizes

Parameters for modeling

- User input or DFP Twiki Page
- Step off wafer Y/N
- Touchdowns limited to 1 per pad

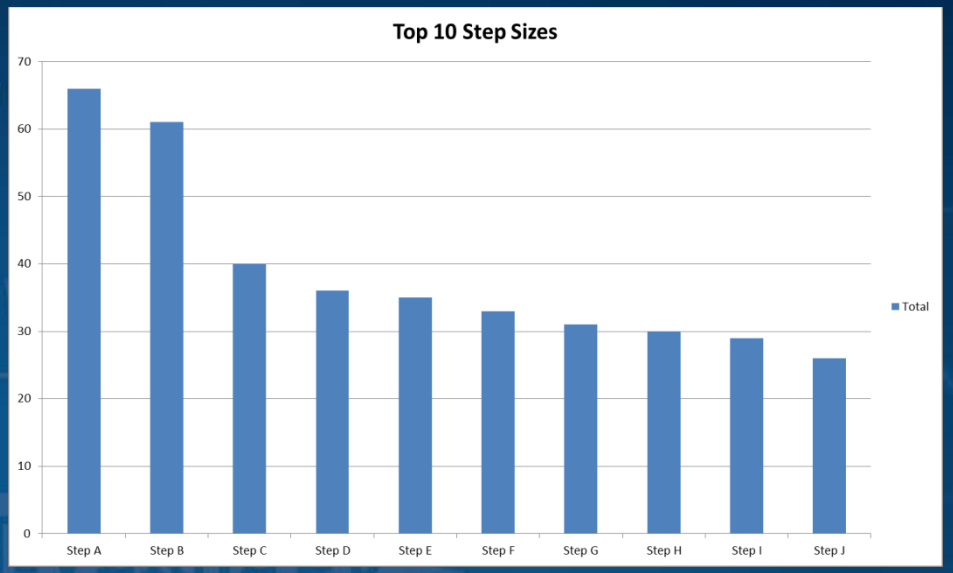
Decisionizer Flow



Output Example

Efficiency	Layout Type	Card Technology	# Sites	# Pins	Pitch	Temp
93.77	diagonal	Vertical	8	500	80um	85
95.62	tight matrix	cantilever	8	500	80um	85
93.77	Skip Row	Vertical	8	500	80um	

TOP 10 Step Size Groups



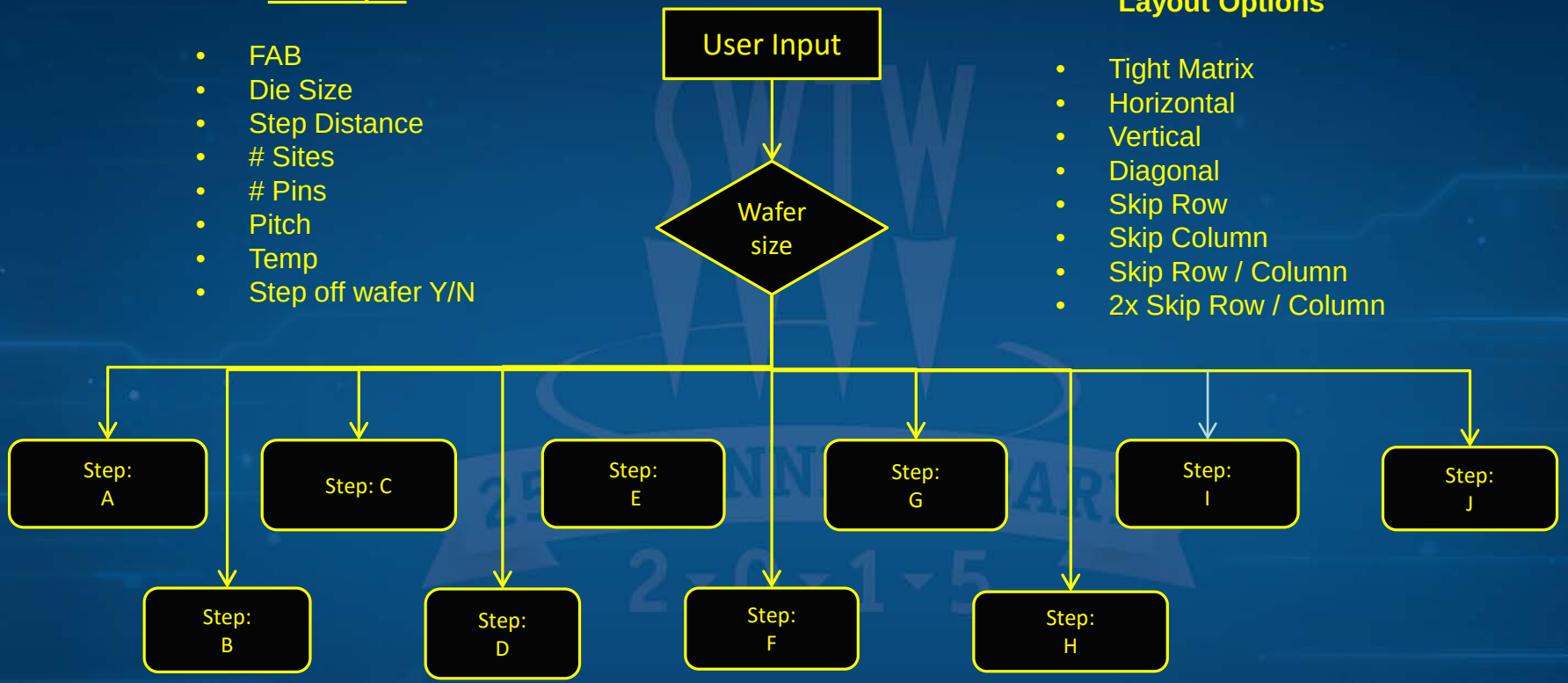
Improvement

- Streamline the Design for Probe process
- Provide BU needed information for the most efficient probe card layout
- Step Maps staged and available for implementation at device setup by PDE

Design for Probe Flow

User Input

- FAB
- Die Size
- Step Distance
- # Sites
- # Pins
- Pitch
- Temp
- Step off wafer Y/N



Layout Options

- Tight Matrix
- Horizontal
- Vertical
- Diagonal
- Skip Row
- Skip Column
- Skip Row / Column
- 2x Skip Row / Column

Output Example

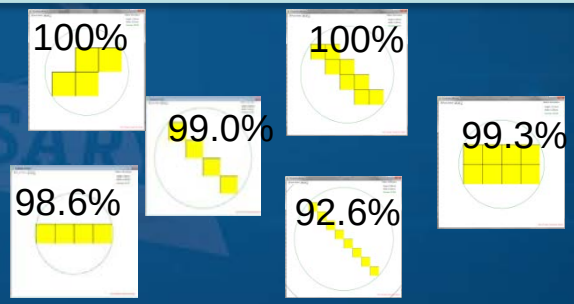
Efficiency	Layout Type	Card Technology	# Sites	# Pins	Pitch	Temp
93.77	diagonal	Vertical	8	500	80um	85
95.62	tight matrix	cantilever	8	500	80um	85
93.77	Skip Row	Vertical	8	500	80um	

Stepping Efficiency

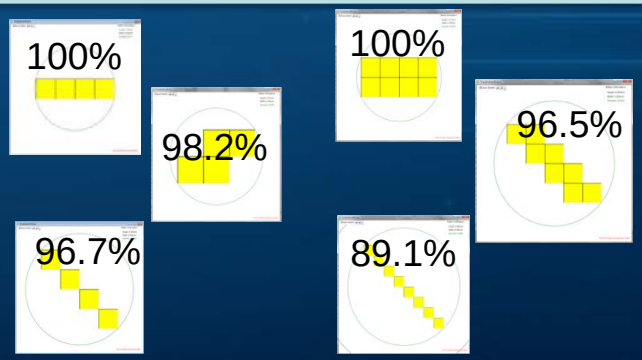
x4 x8

- **Design A, x4 & x8**
  - Best design is “special” pattern
  - Diagonal is worst

- **Design B, x4 & x8**
  - Best design is “special” FFI pattern
  - 1x4 is not good for x4
  - Diagonal is within 1% for x4, worst for x8



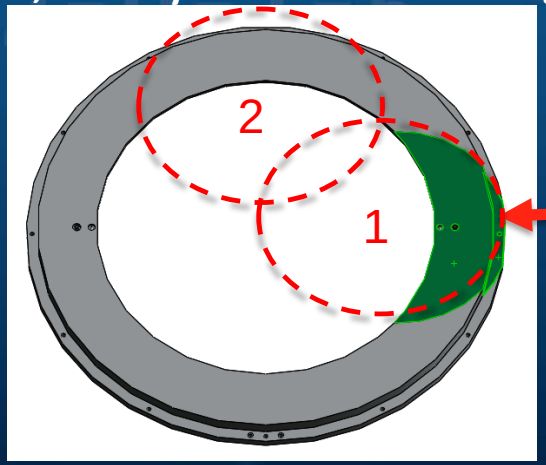
- **Design C,**
  - Best design is 1x4 & 2x4
  - Diagonal is worst



Thermal Challenges

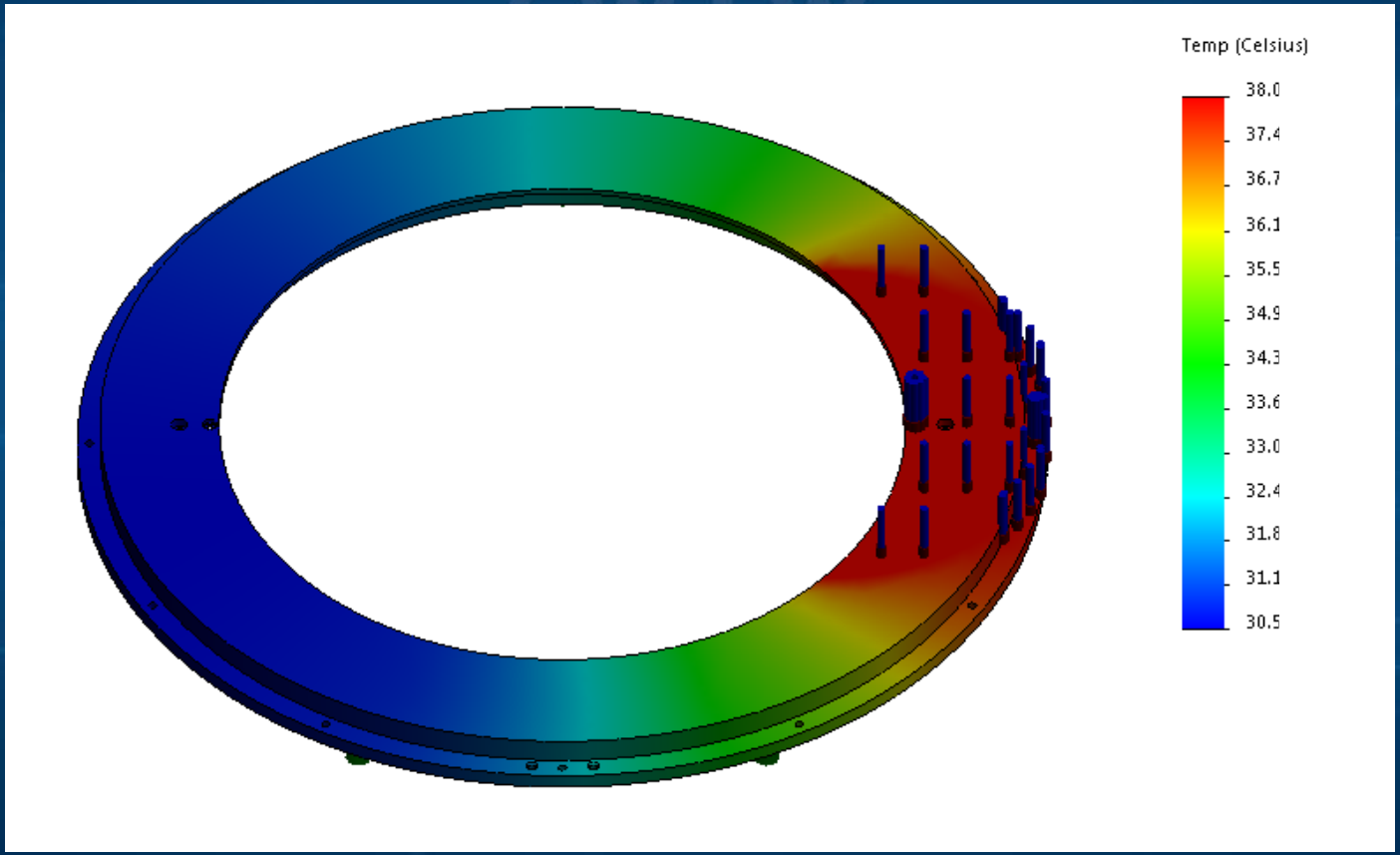
New Hardware Evaluations

- **The implementation of larger 18 inch probe cards along with the customer requirements to probe between -40°C – 150°C have created unique thermal challenges.**
- **The following is an off-center prober chuck study as it was applied to the bottom surface of the ring insert.**
  - **The temperature within the split line area (green) was set to 38C, as measured empirically.**
  - **Ambient temperature was defined as 30C.**
  - **A convection coefficient of 5 W/m-K was applied to the top surface of the insert.**
- **The split line representing localized heating was varied between two locations:**
  1. **The side of the insert (3 o'clock position)**
  2. **The top of the insert (12 o'clock, directly under the cutout region for the clamshell hinge)**



Temperature Profile Results

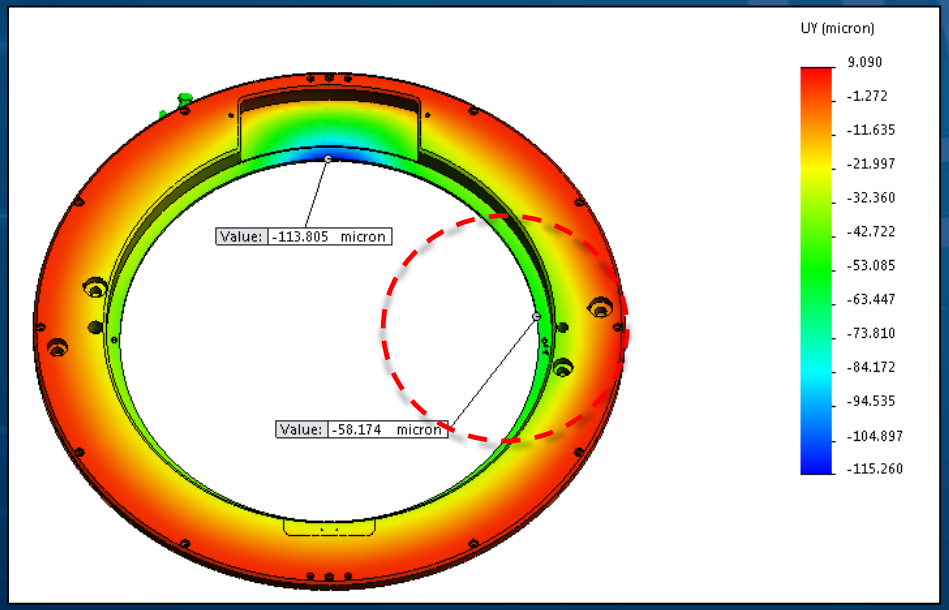
- **Temperature variation across insert: 38 C to 30.5C**



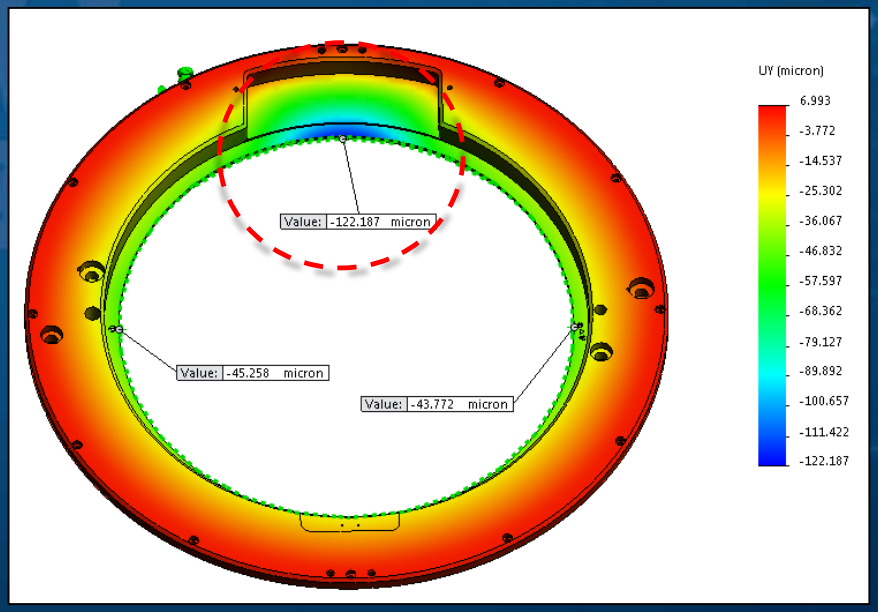
Off-center heating
Underside of insert shown

Thermal Z Deflection – Material A

- **Heating at 3 o'clock position**
  - Probe card lip deflection:
    - *Min:* -58 um
    - *Max:* -114 um
    - *Induced tilt:* 56 um



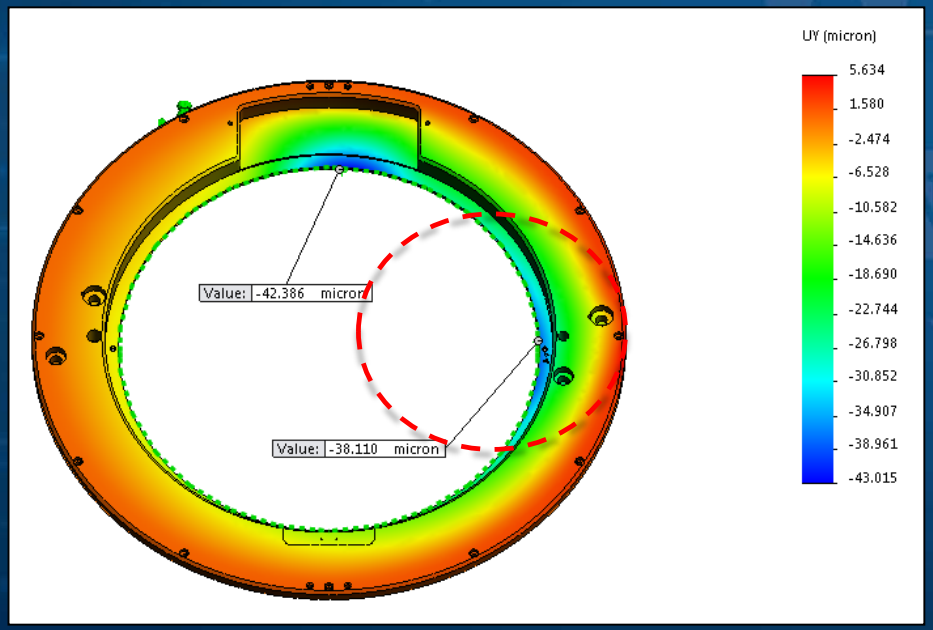
- **Heating at 12 o'clock position**
  - Probe card lip deflection:
    - *Min:* -44um
    - *Max:* -122 um
    - *Induced tilt:* 78 um

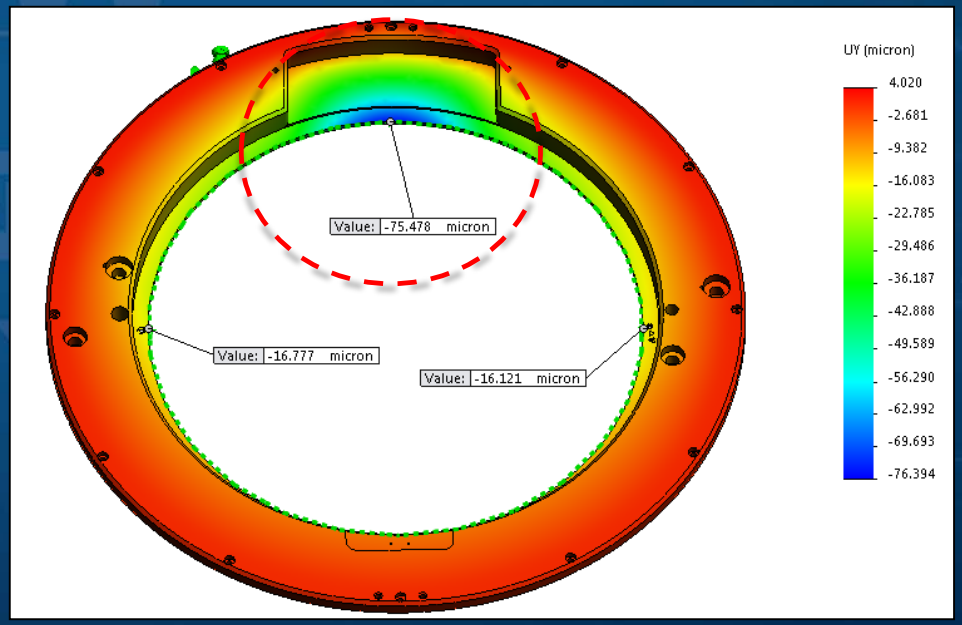


•With the revision 0 (Material A) cardholder insert, the magnitude of Z deflection and induced tilt is high: despite a 8-degree C temperature change.

Thermal Deflection – Material B

- **Heating at 3 o'clock position**
  - Probe card lip deflection:
    - *Min:* -6 um
    - *Max:* -42 um
    - *Induced tilt:* 36 um
- **Heating at 12 o'clock position**
  - Probe card lip deflection:
    - *Min:* -16 um
    - *Max:* -75 um
    - *Induced tilt:* 59 um

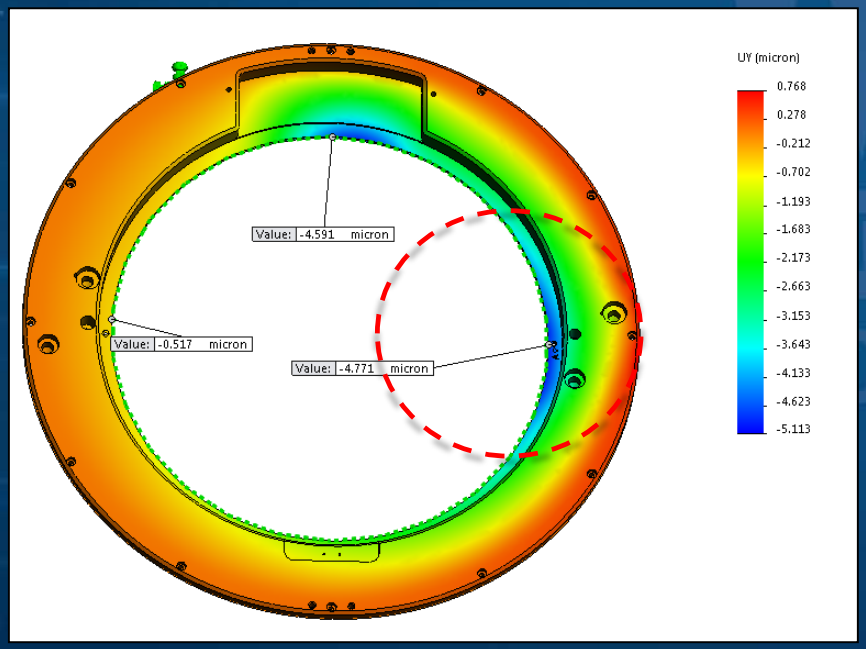




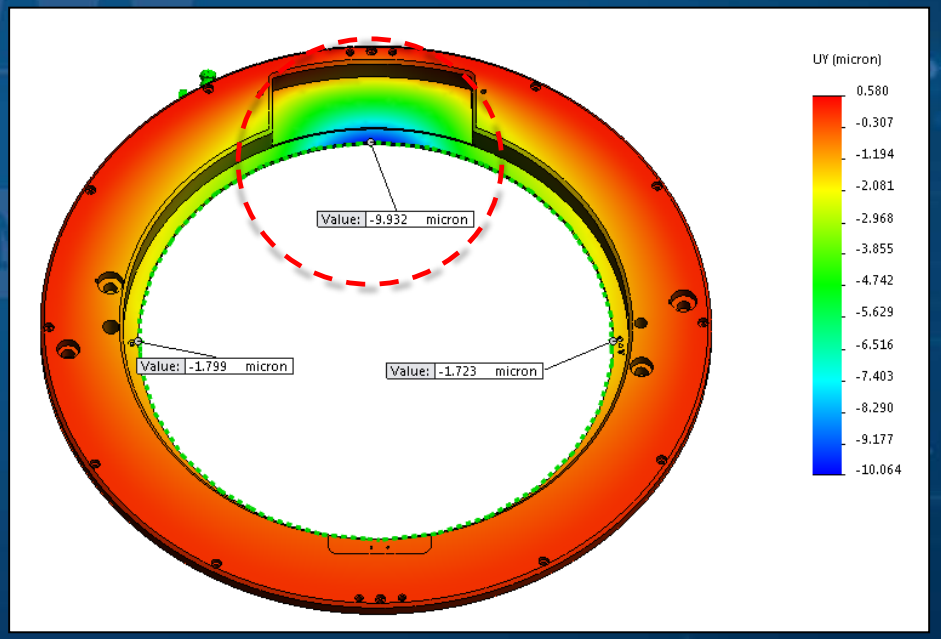
•The level of improvement expected from a material change to material B is fair, but still shows an induced tilt not conducive for a manufacturing environment.

Thermal Deflection – Material C

- **Heating at 3 o'clock position**
  - Probe card lip deflection:
    - *Min:* -0.5 um
    - *Max:* -5 um
    - *Induced tilt:* 4.5 um

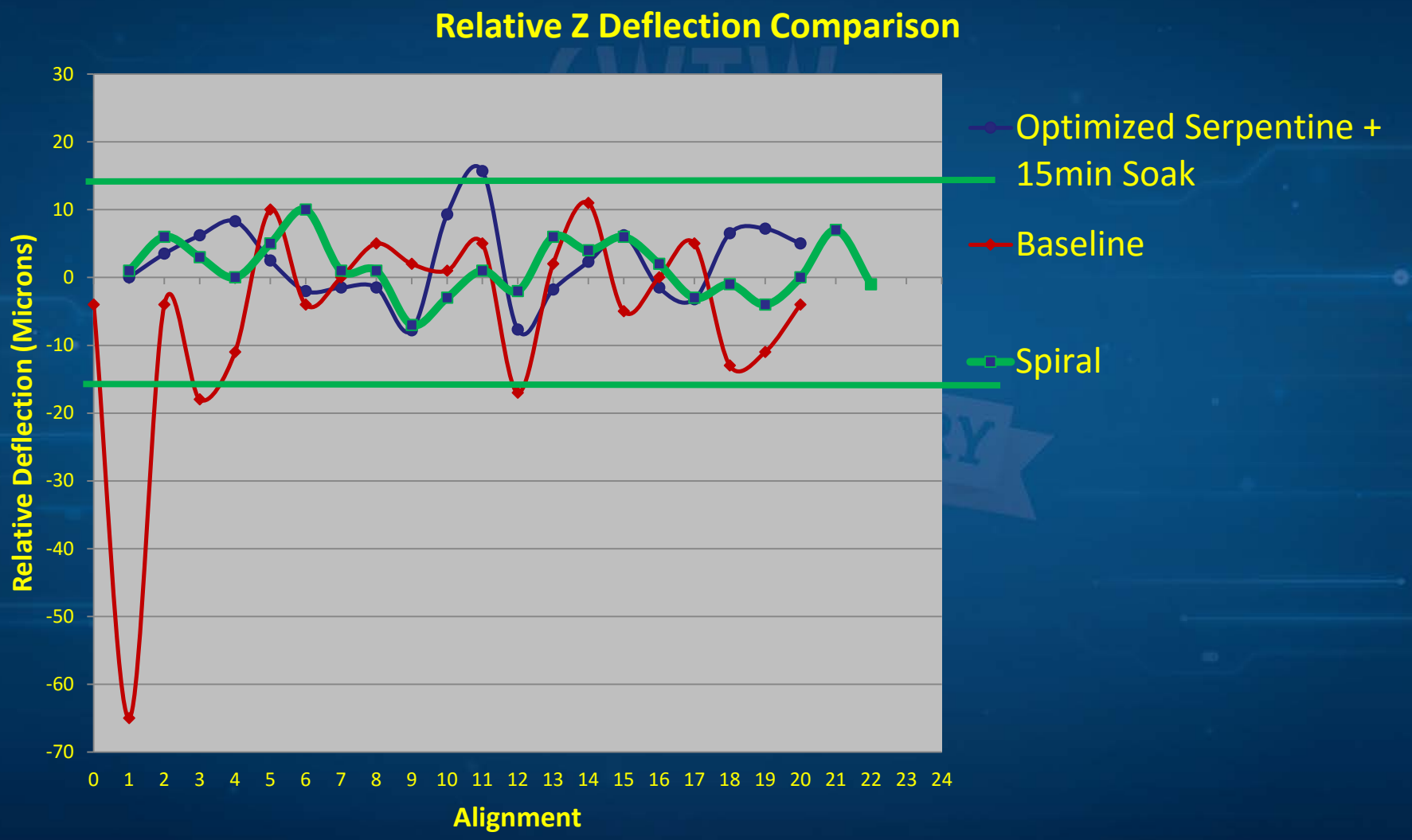


- **Heating at 12 o'clock position**
  - Probe card lip deflection:
    - *Min:* -1 um
    - *Max:* -10 um
    - *Induced tilt: 9* um



- The improvement expected from a change to low CTE material C is quite dramatic, in regard to both Z deflection and induced tilt.

Z Deflection Comparison (Delta)



Summary of Findings

What do we know:

- **Optimized touchdown positioning increases test efficiency, saves process time, and reduces the cost of test.**
- **Stepping optimizers are able to provide customized stepping routines enabling:**
  - Thermal compensation for at temperature probing.
  - Optimization of prober performance and identification of prober deficiencies.
  - Reduction of thermal soaks / needle realignment (probing overhead).

What is still to come:

- **Implementation at time zero allows users to design in probe efficiency**
  - Selection of the best card technology and the most efficient layout
  - Optimized step files allowed for avoidance of costly low CTE materials
- **Identification and mitigation of electrical signatures**
- **Design in quality and minimize probe damage for our customers.**

Acknowledgements

- Andre Stoelwinder
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