SW Test Workshop
Semiconductor Wafer Test Workshop
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AP to LPDDR Probe Card

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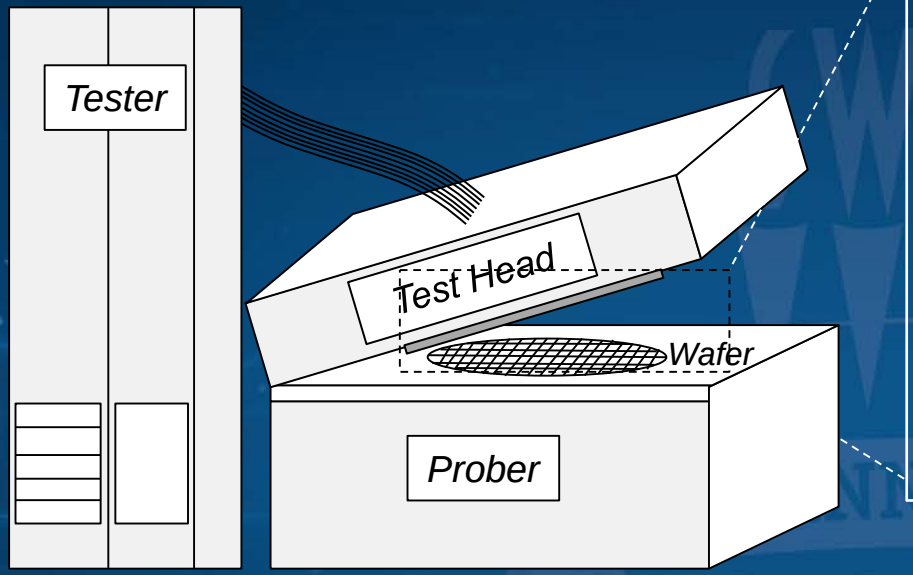
Will Technology

Overview

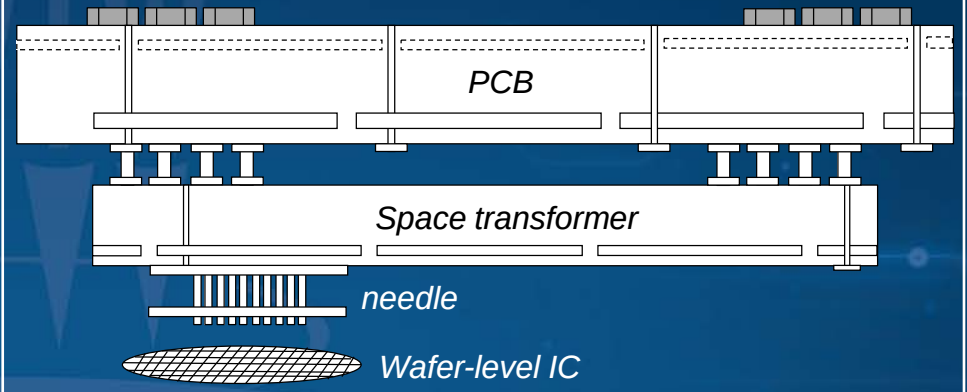
- Introduction
- Probe Card Architecture
- SI / PI Simulation
- Measurement
- Conclusion

Introduction

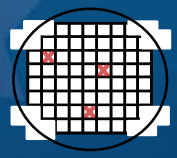


< ATE for the wafer-level test >

< Schematic diagram of the vertical probe cards >



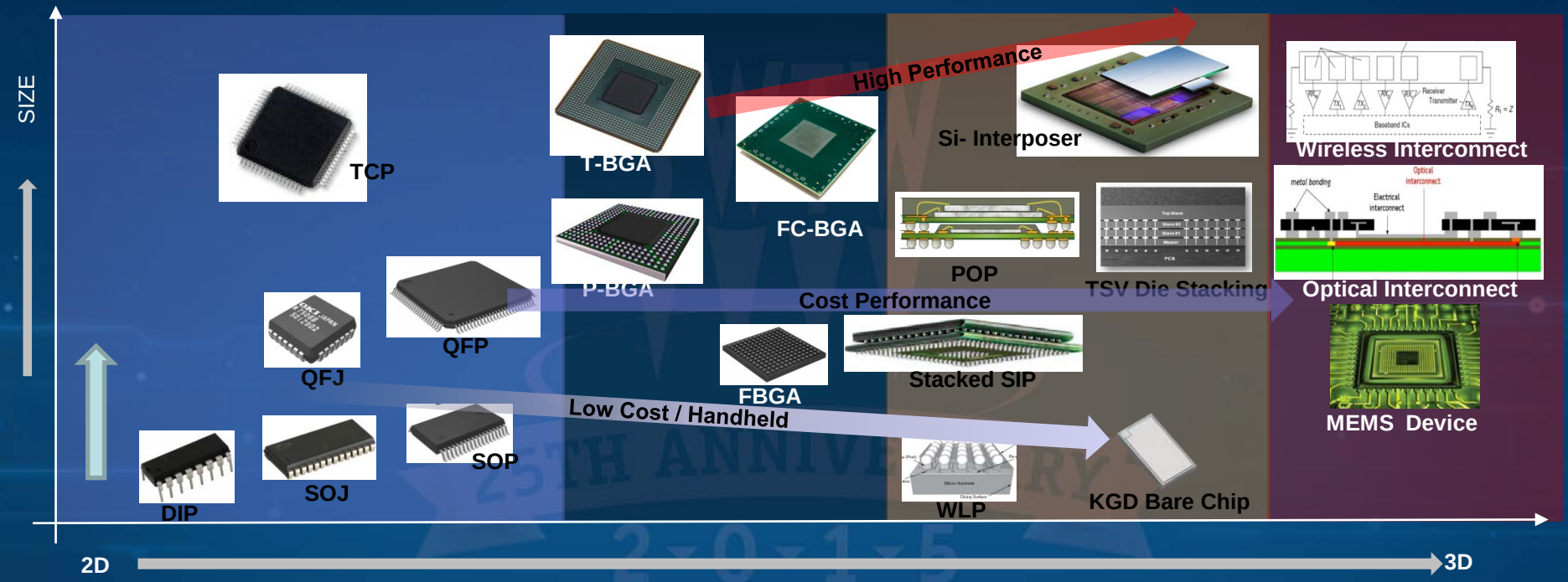
Wafer-level test



Pass / Fail ?

- Decrease the overall cost of testing by detecting chip fail before packaging .
- As the quality of the probe card has a strong influence on the IC yield, high reliability on the probe card is required in the wafer test process.

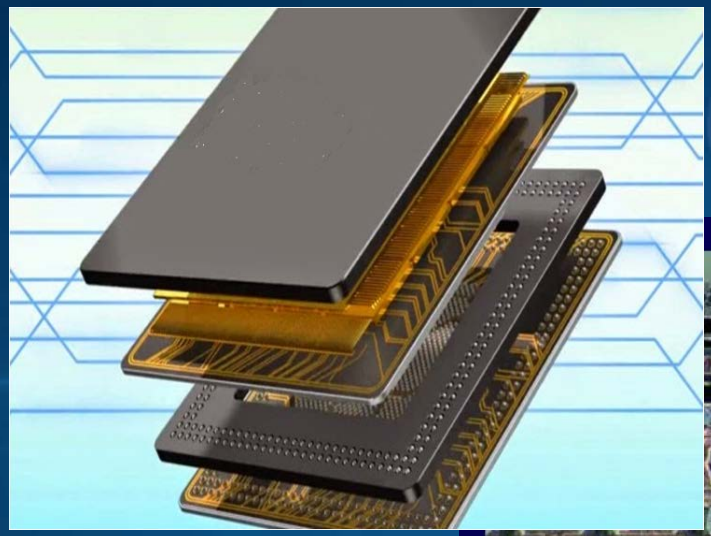
Introduction



- 3D structure of TSV or POP is generally applied for the Package Types.
- When problem occurs between package to package on POP structure,

→ **Will Technology proposes a probe card structure that will elliminate unnecessary cost and time that may occur at package level through increasing test credibility at the Wafer Level.**

Introduction



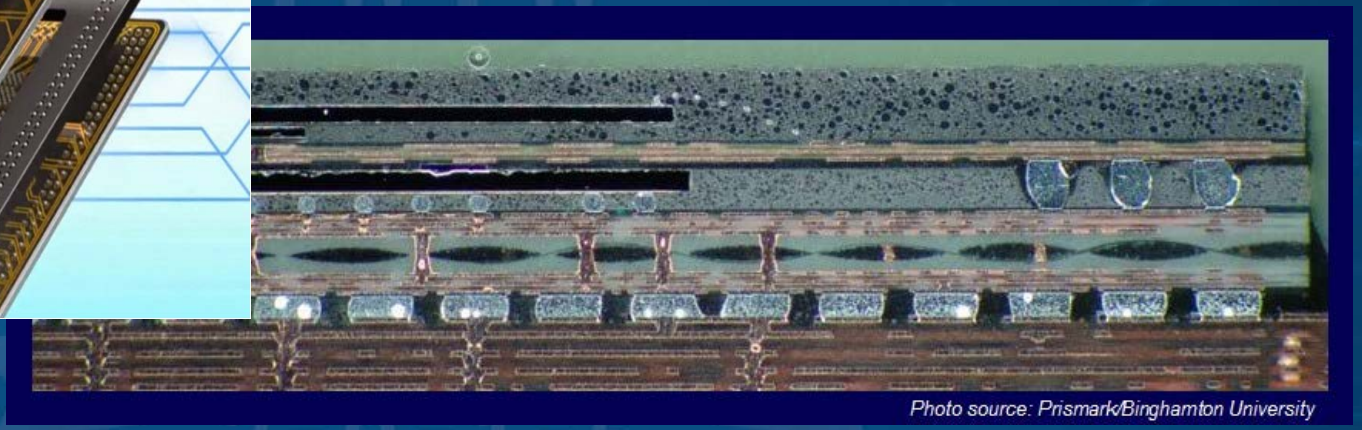
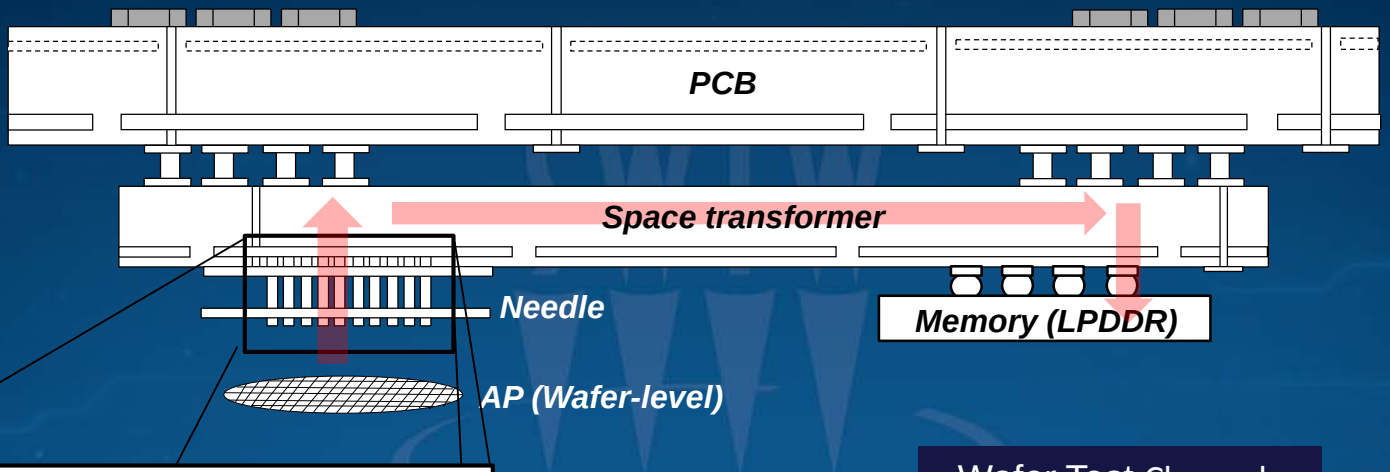
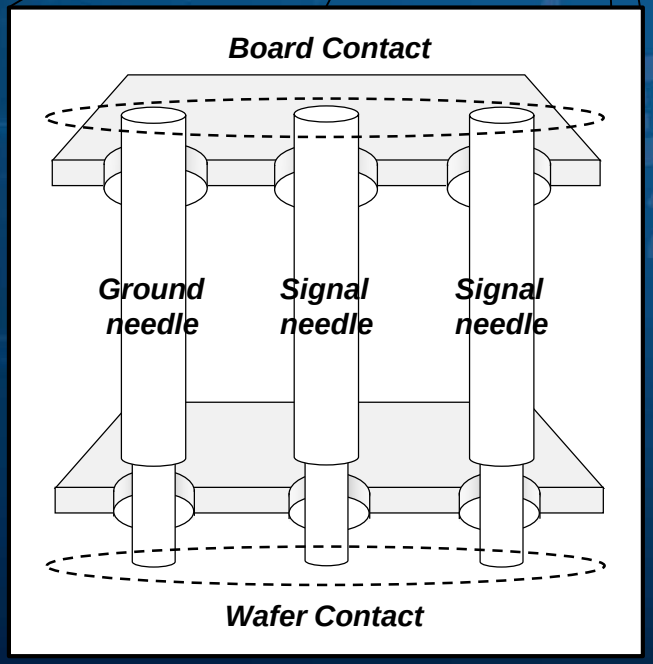


Photo source: Prismark/Binghamton University

- **Development Plan**
  - Current: Unable to test AP & Memory at Wafer Level
  - AP & Memory is tested at Package on Package
  - Extra cost occurrence from untested AP & Memory
  - High Speed performing Probe Card development need for AP & Memory

Probe Card Architecture



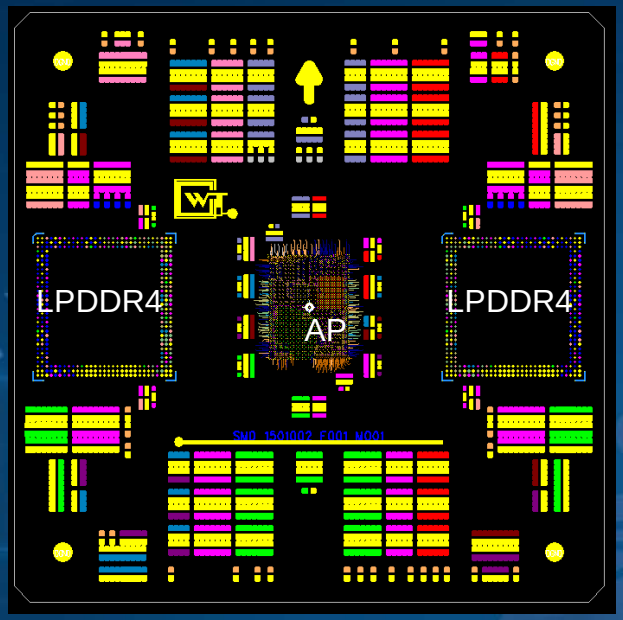


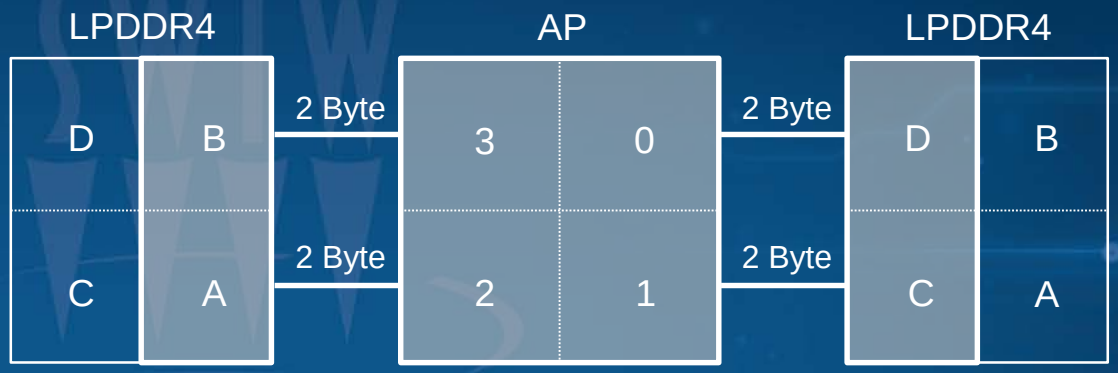
Wafer Test Channel

AP → Needle → Space transformer → Memory

- The test signal transfer between Application process and memory.
- The needle and the space transformer are utilized as the interface for signal routing.

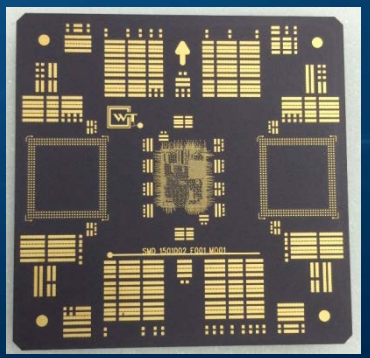
MLC Design





2 Byte x 4 Channel = 8 Byte

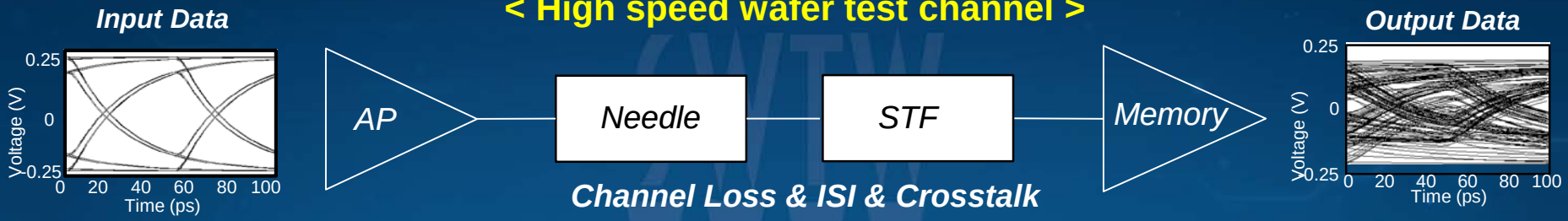
- **MLC Design**
  - Place LPDDR on Left/Right of AP for shorter path between AP-LPDDR
  - Short Routing Length



<MLC>

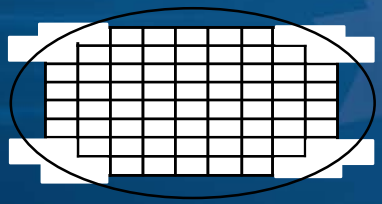
Simulation Condition

< High speed wafer test channel >



Channel Loss & ISI & Crosstalk

- Increasing pad density
- Narrowing pad pitch



AP (Wafer-level)

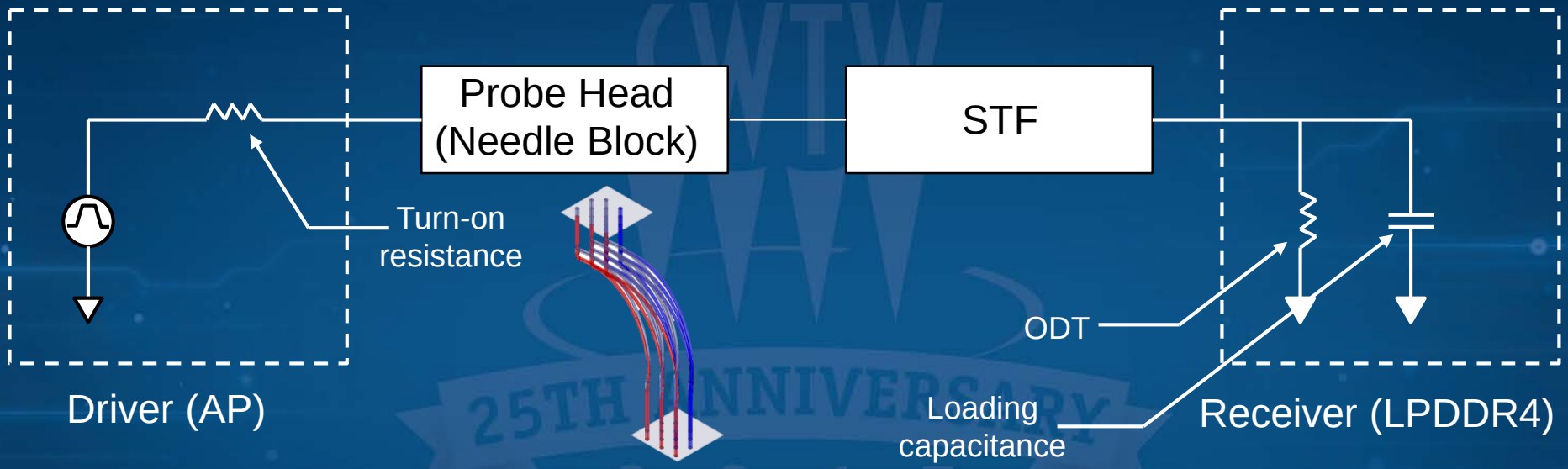
		LPDDR3	LPDDR4
Perform	B/W	12.8GB/s	25.6GB/s
	Data rate	***1.6Gbps***	***3.2Gbps***
number of IO		x64	X64

<LPDDR target electrical specification>

- Input data is degraded by channel loss, ISI and crosstalk in high-speed test channel
- To improve reliability of wafer test channel in probe card, it is necessary to analyze Signal integrity & Power Integrity

Simulation Condition

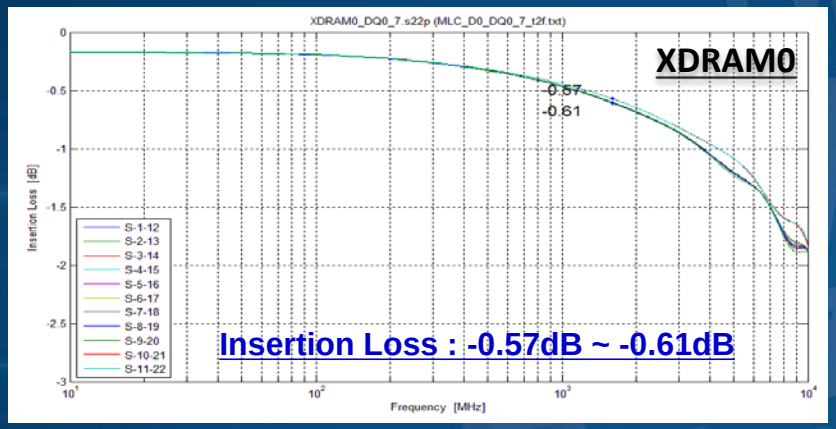
- **SIMULATION CONDITION**

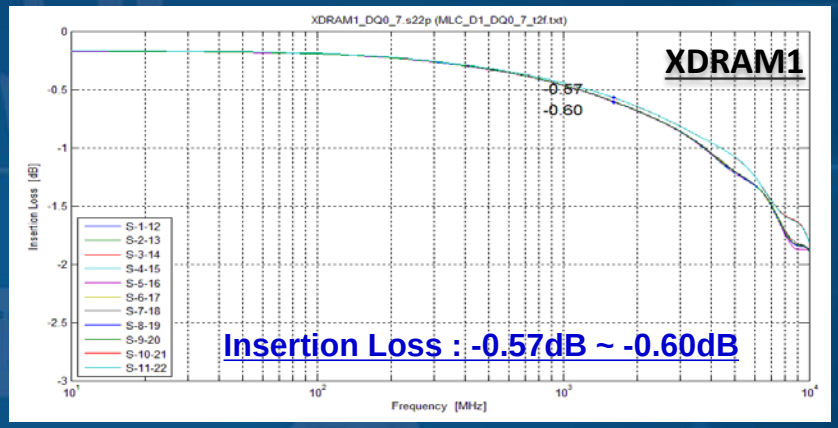


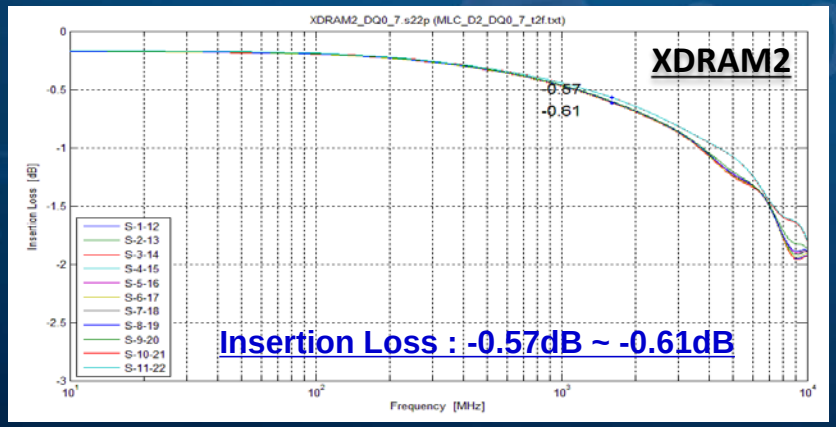
- Input Voltage: 1.1 V
- Data rate: DQ group → 1600 Mbps, 3200 Mbps, CA group → 800 Mbps, 1600 Mbps
- Rise / Fall Time: UI/4
- Turn-on resistance: 48 ohm
- Data pattern: PRBS 2^5
- Loading Capacitance: 2pF
- ODT: 48 ohm

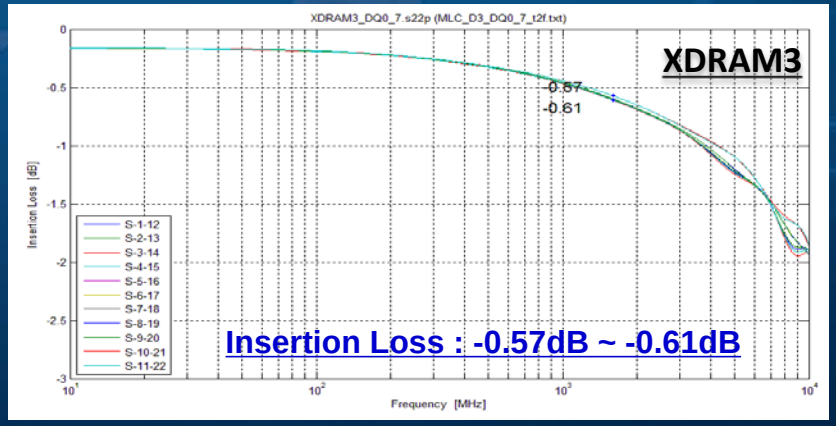
Signal Integrity

- **Insertion Loss**
  - DRAM Channel SI Simulation
  - Low Insertion Loss (Approx. -0.6dB)



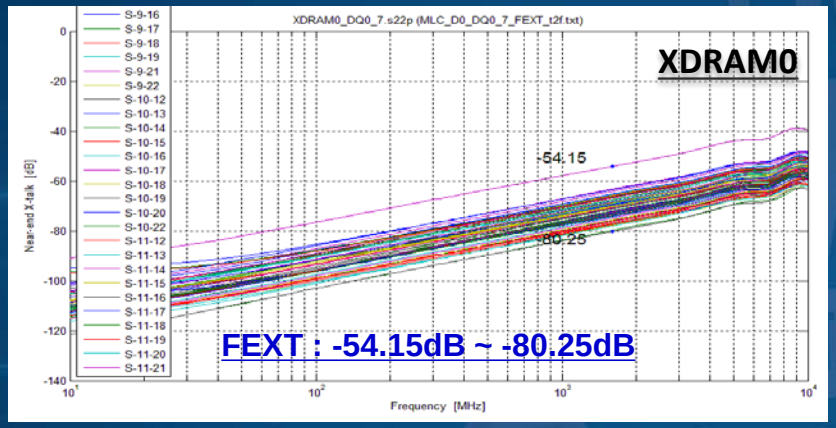


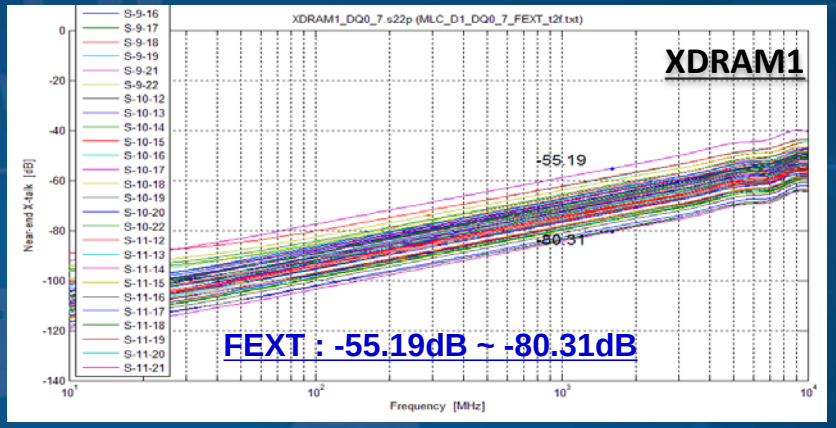


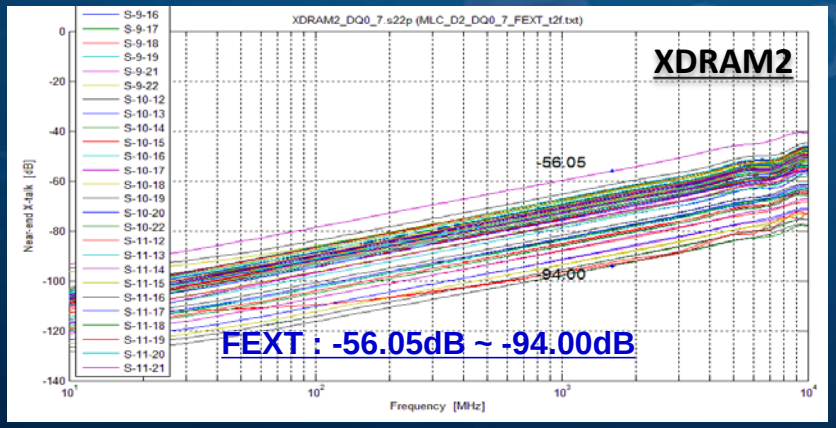


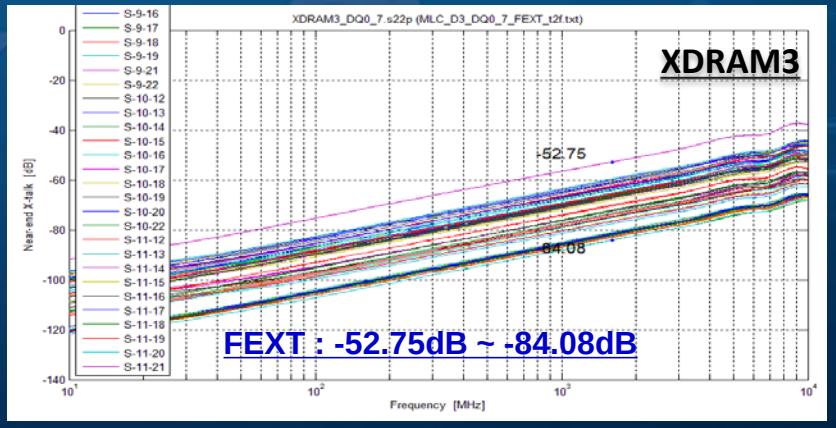
Signal Integrity

- **Crosstalk Noise**
  - DRAM Channel SI Simulation
  - Low Crosstalk Noise (Approx -52dB ~ -90dB)



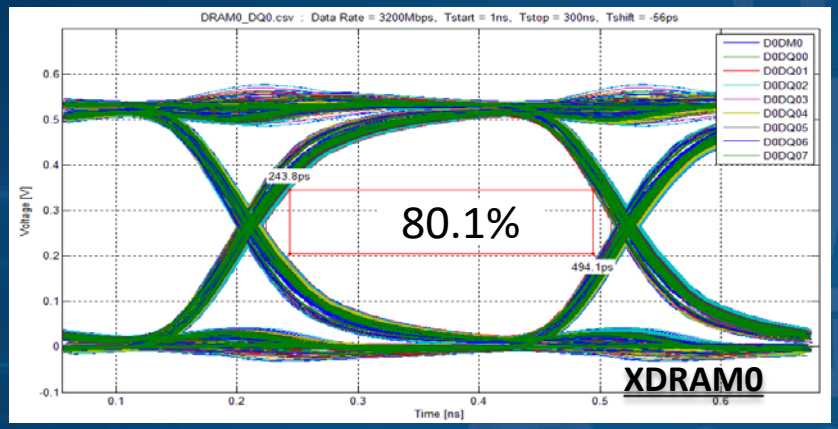


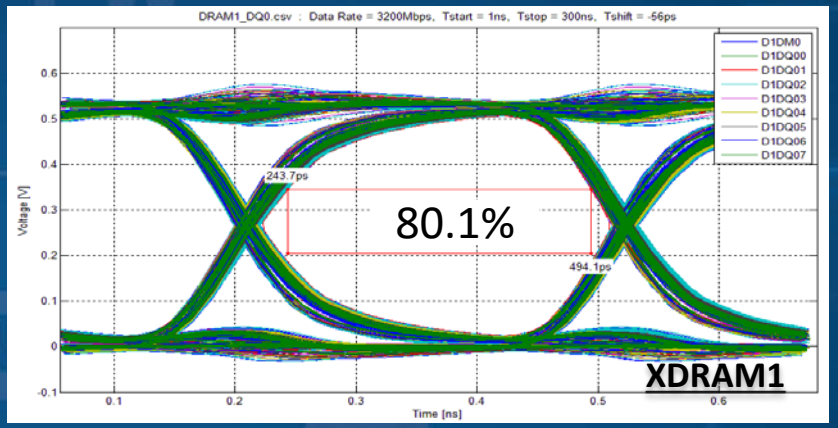


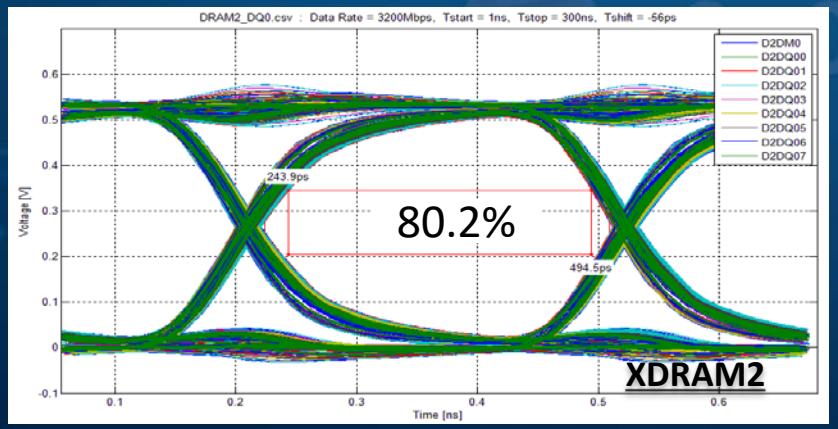


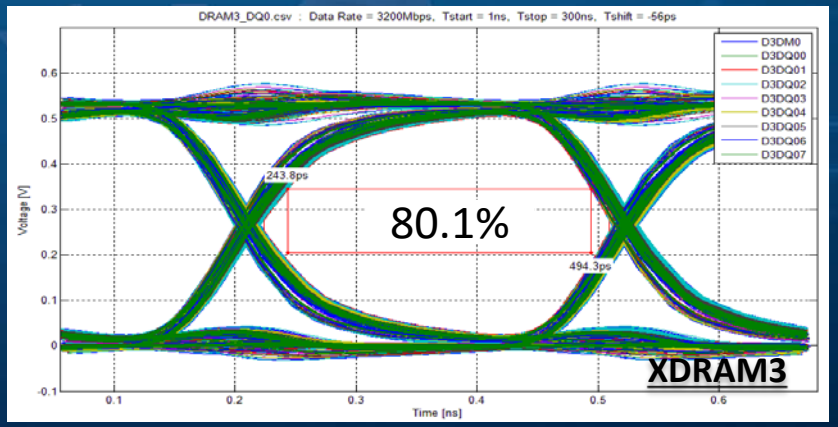
Signal Integrity

- **Eye Diagram**
  - DRAM Channel Eye Simulation (@3.2Gbps)
  - Eye Opening : Approx. 80%



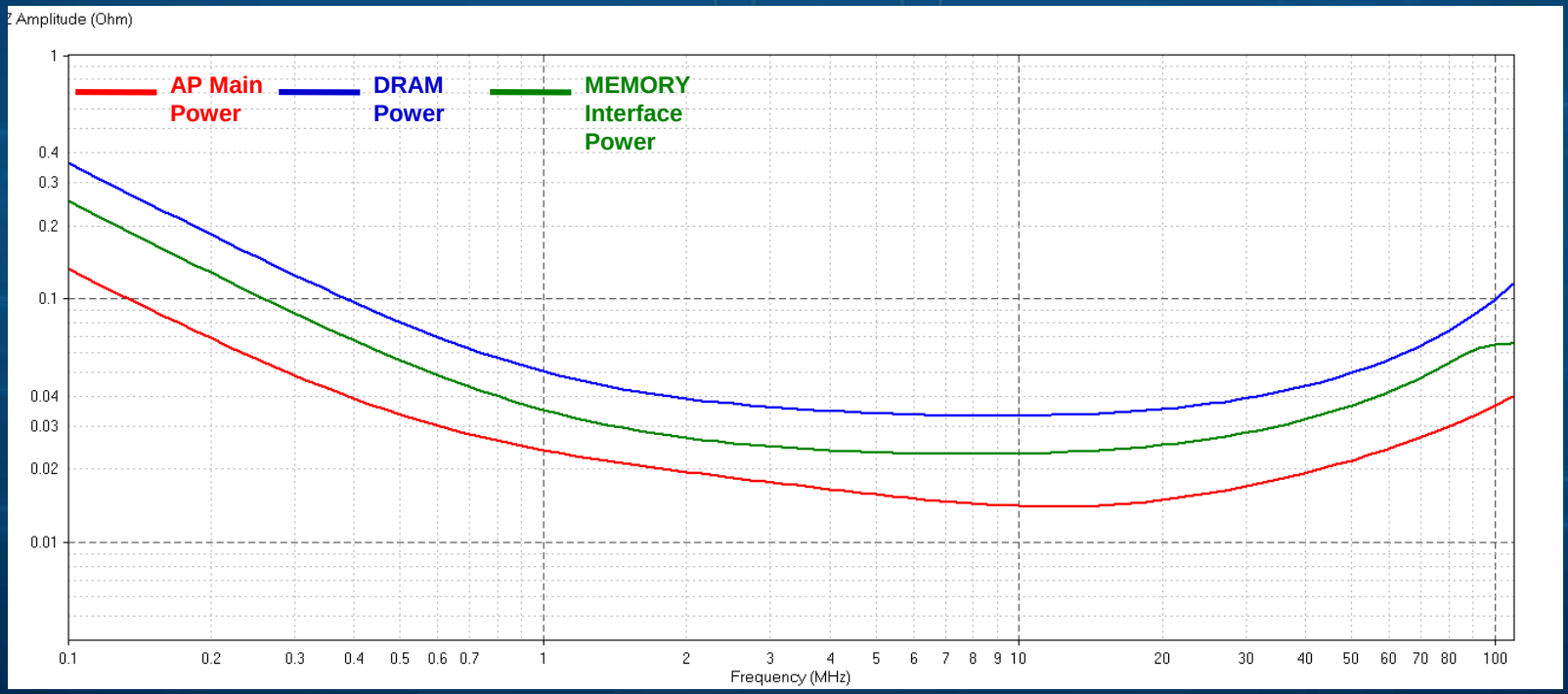






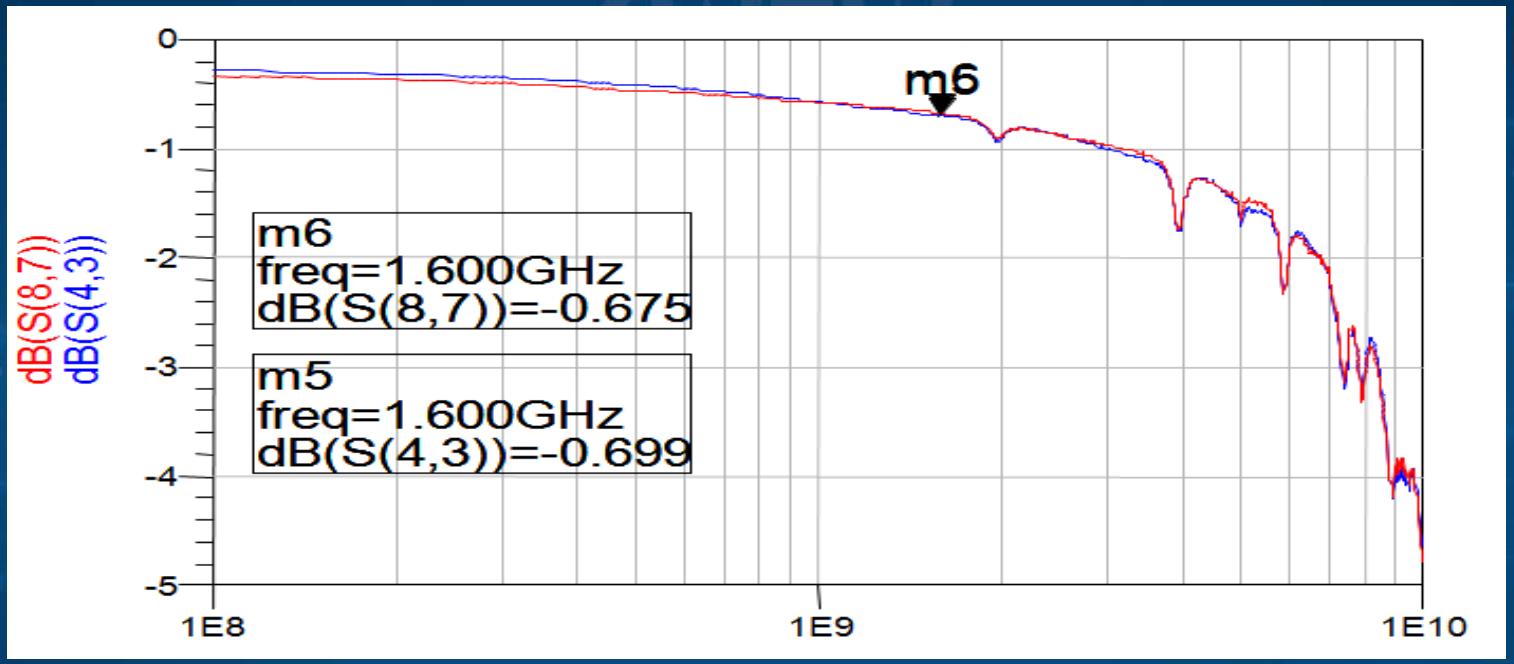
Power Integrity

- **Power Impedance**
  - PI designs for Low Z implementation
  - Design based on prioritizing Power / AP Main Power related to Memory



Measurement

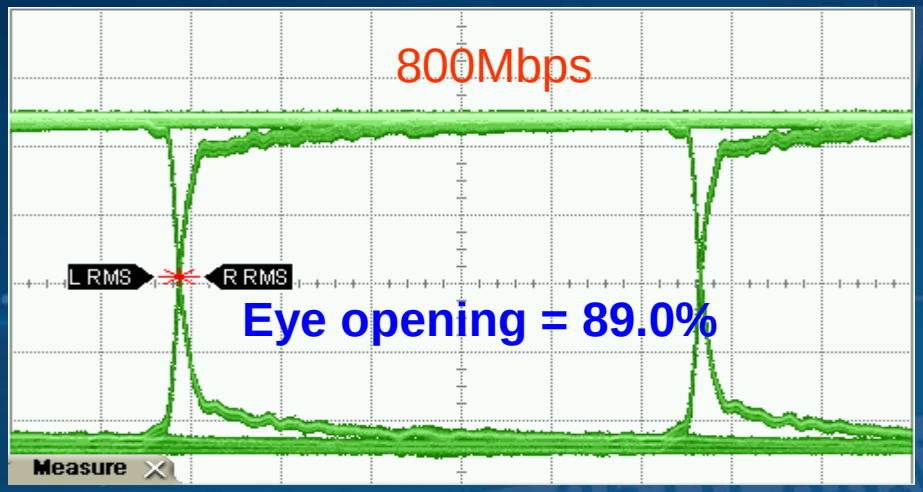
- **SI Measurement (Insertion Loss)**

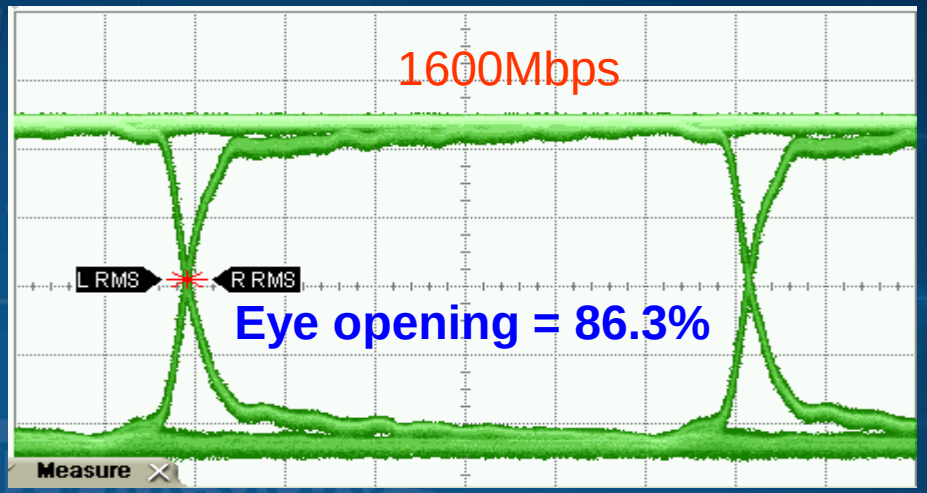


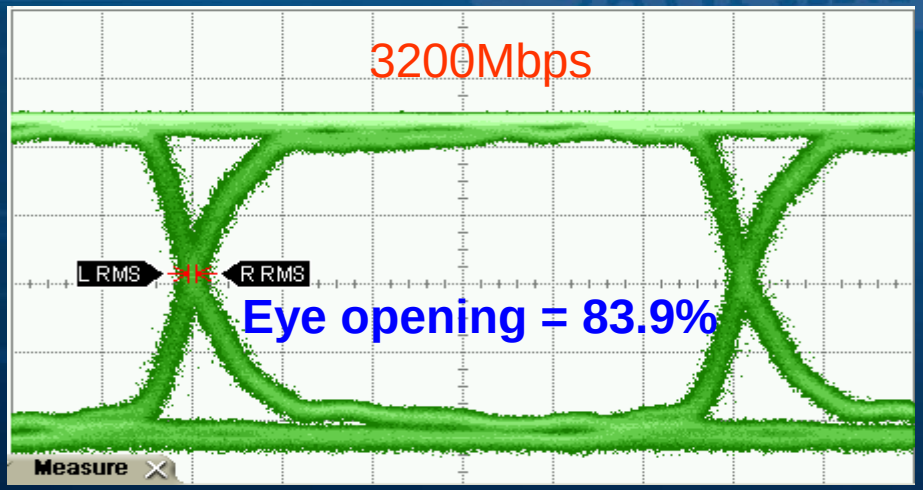
Insertion Loss Measurement	• Measure Insertion Loss (S21) similar to simulation result • Confirm low Insertion Loss through actual measurement

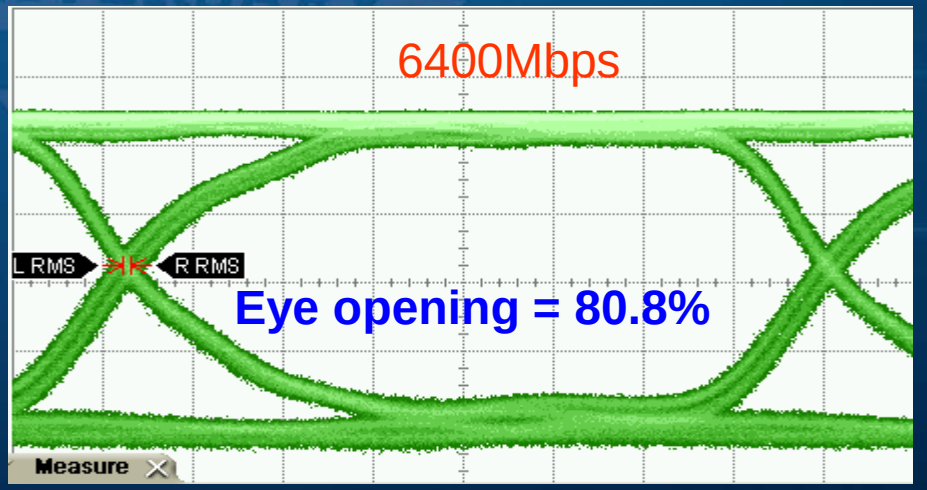
Measurement

- **SI Measurement (Eye Diagram)**



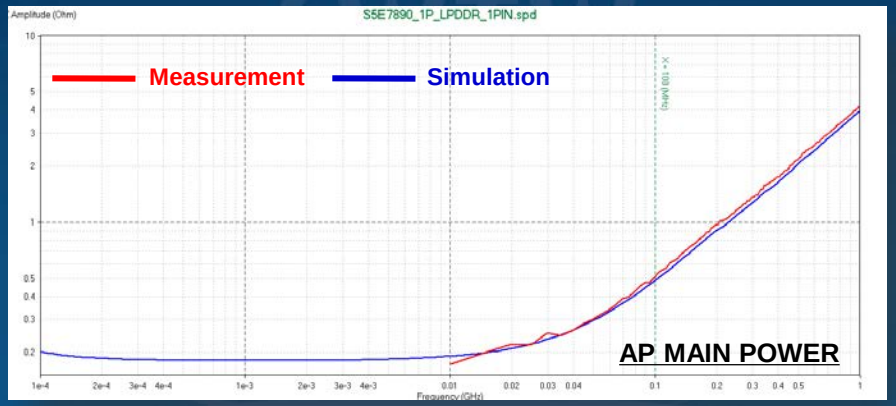


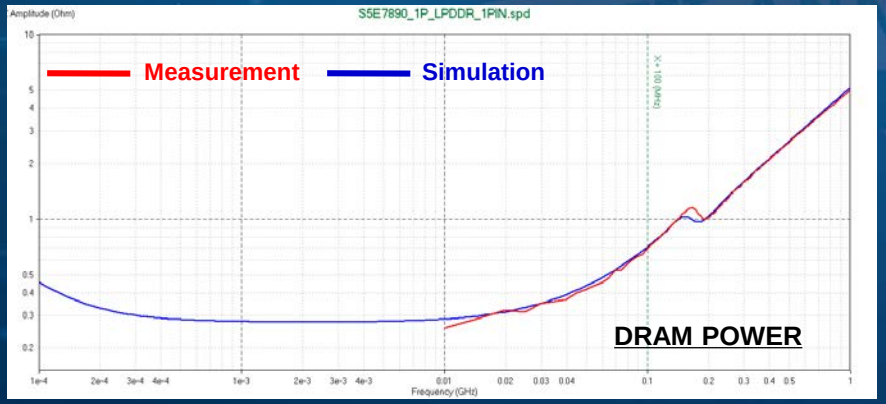


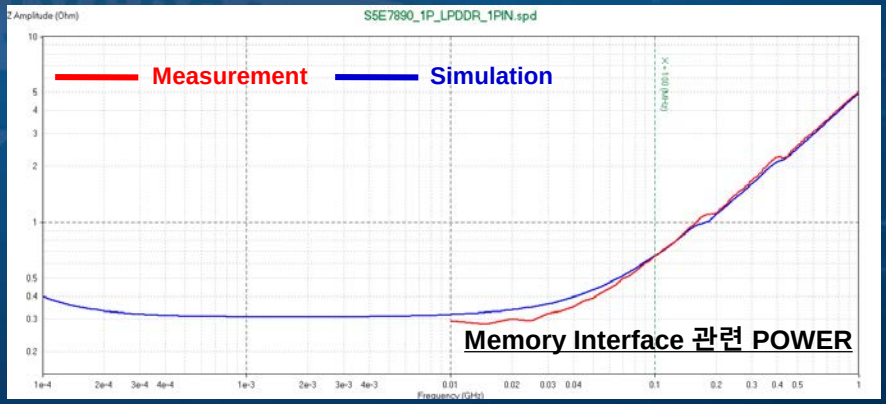


Measurement

- **PI Measurement (1Pin Power Impedance)**







Confirm Power Impedance through Simulation & Measurement Correlation

Conclusions & Future Works

Expected Benefits

- Yield increase through AP-Memory Channel Test at wafer level before Packaging
- High Speed Test (Ables Testing at Actual Operating Speed)

- Target :
  Production of Probe Card capable of performing at 3.2Gbps or faster

Thank You