Silicon, Interconnect, Packaging and Test Challenges from a Foundry Viewpoint

SWTC June 2015

GLOBALFOUNDRIES®

Keynote Perspective

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EDA & IP Partners
Development and validation

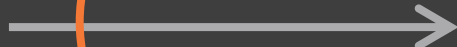
Memory Partners
Integration and characterization

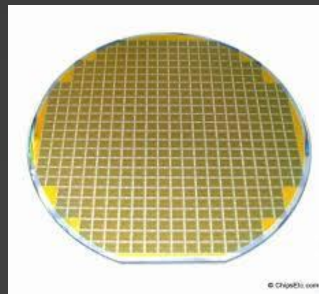
Design → Test Dev (DFT) → Reticle Sets → Wafer Fab & FSI → Bump → Probe → Thin & BSI → Ass'y & Test

Design Partners
Design flow, rules and tool alignment

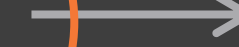
OSAT Partners
Process development and characterization
For 3D and 2.5D, µbump is owned by the OSAT

Customer Design





Bump and Probe



Assembly, Package Test, Board Mount

Agenda

1 Trends in Silicon

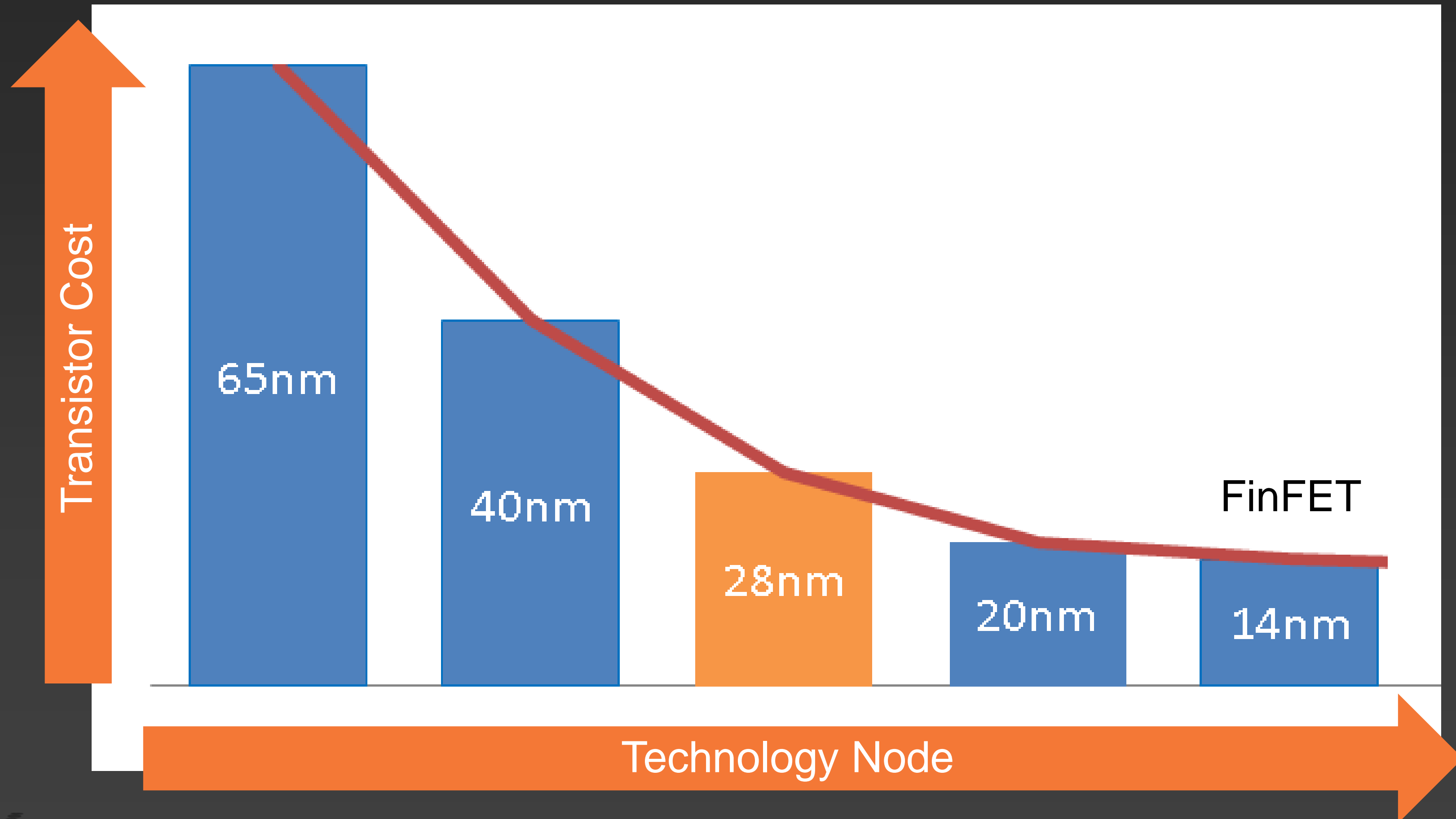
2 Packaging Drivers and Solutions

3 Materials and Design: Challenges and Learning

4 Test Challenges from Foundry Viewpoint

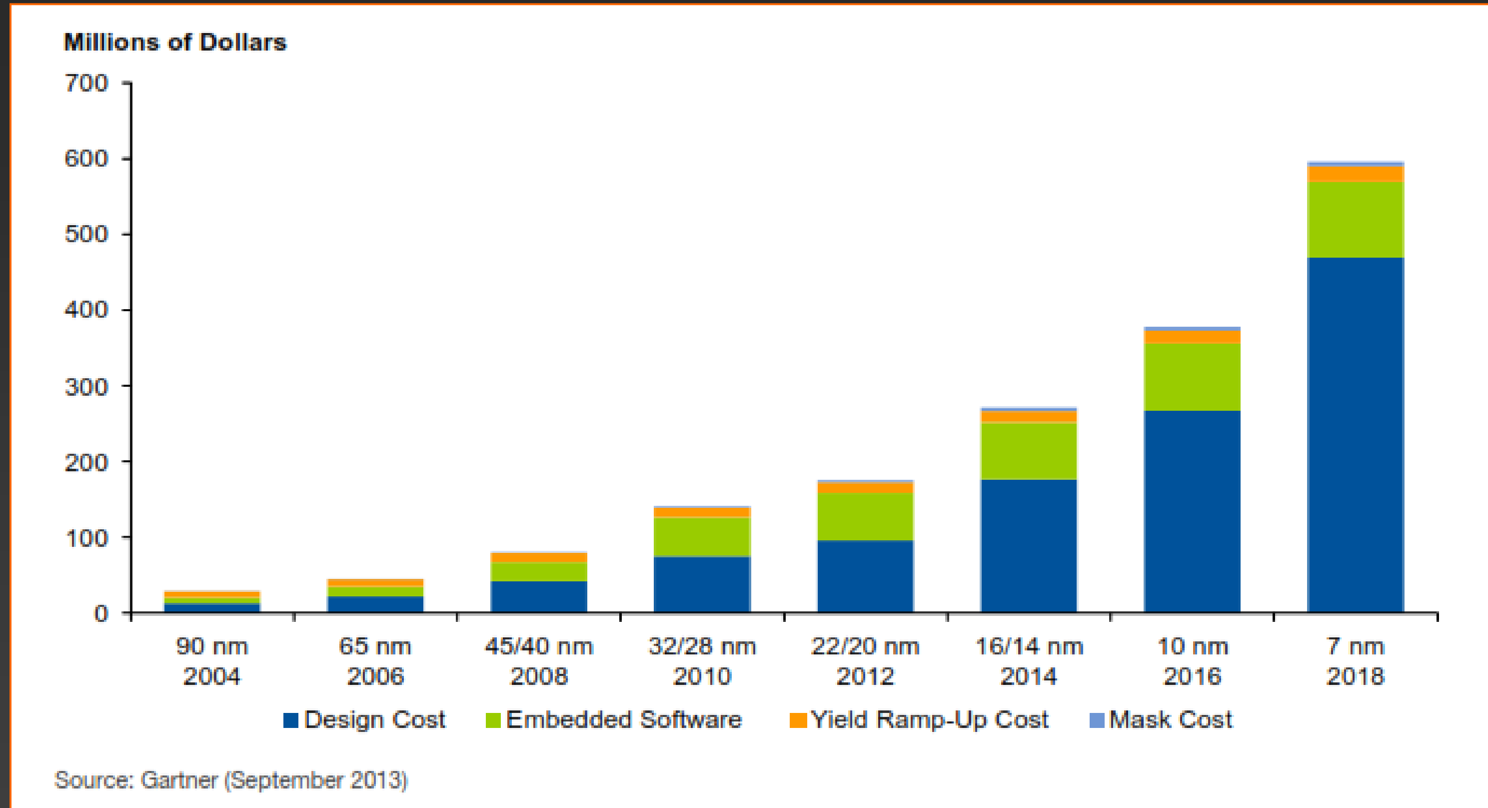
5 Supply Chain Solutions

Cost of Scaling per Transistor is no Longer Decreasing



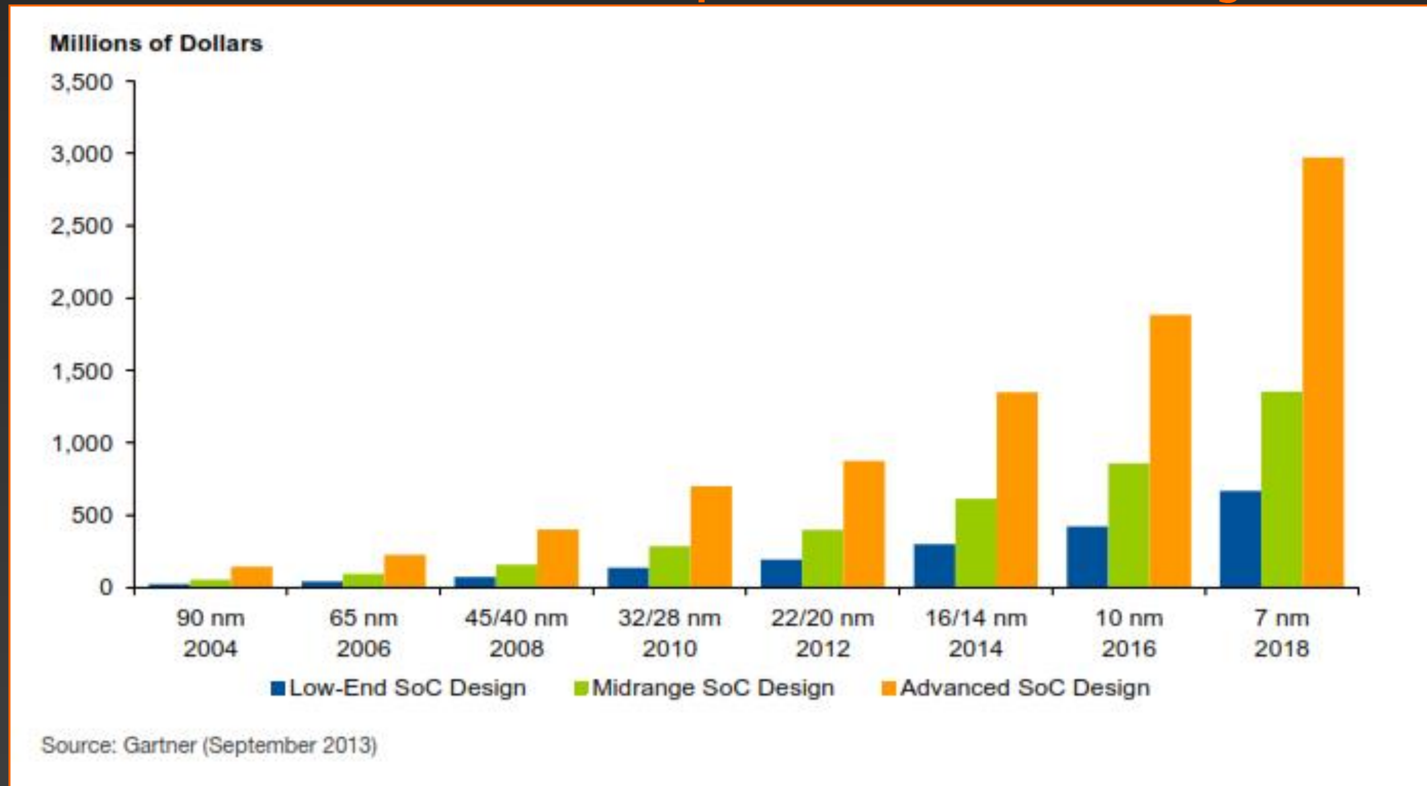
Cost of Scaling is Rapidly Increasing

Estimated Design Costs for an Advanced SoC



- Development cost for 10nm design will approach $400M

Cost of Scaling is Too High



- Requires multi-$B lifetime revenue to be economically feasible per design
- Forces foundries to push customers into “good enough” solutions to drive volume
- Must find other solutions

1 Trends in Silicon

2 Packaging Solutions

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4 Test Challenges

5 Supply Chain Solutions

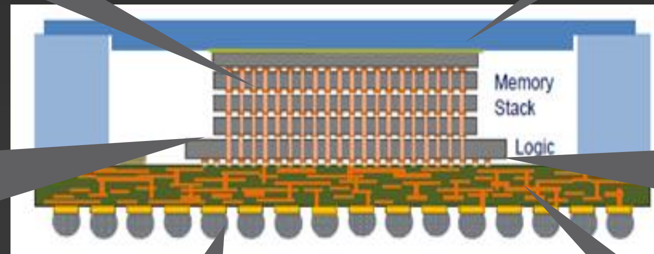
Solutions have to balance performance, power, and cost

Packaging Challenges

TSV Process Challenges
- TSV integration
- Device KOZ
- Pumping

Wafer Test
- Contact technology
- Pitch / Parallelism
- Probe card cost
- Supply chain

Thermal
- Heatsink
- TIM



Bump
- Pitch
- Cu Pillar induced stresses
- EM challenges

Silicon
- BEOL stacks
- Low K modulus
- Thinness (warpage)

Assembly Challenges
- Die attach and die stacking
- Underfill flow vs gap and pitch
- Warpage management

Substrate
- Core CTE
- Warpage
- Routability

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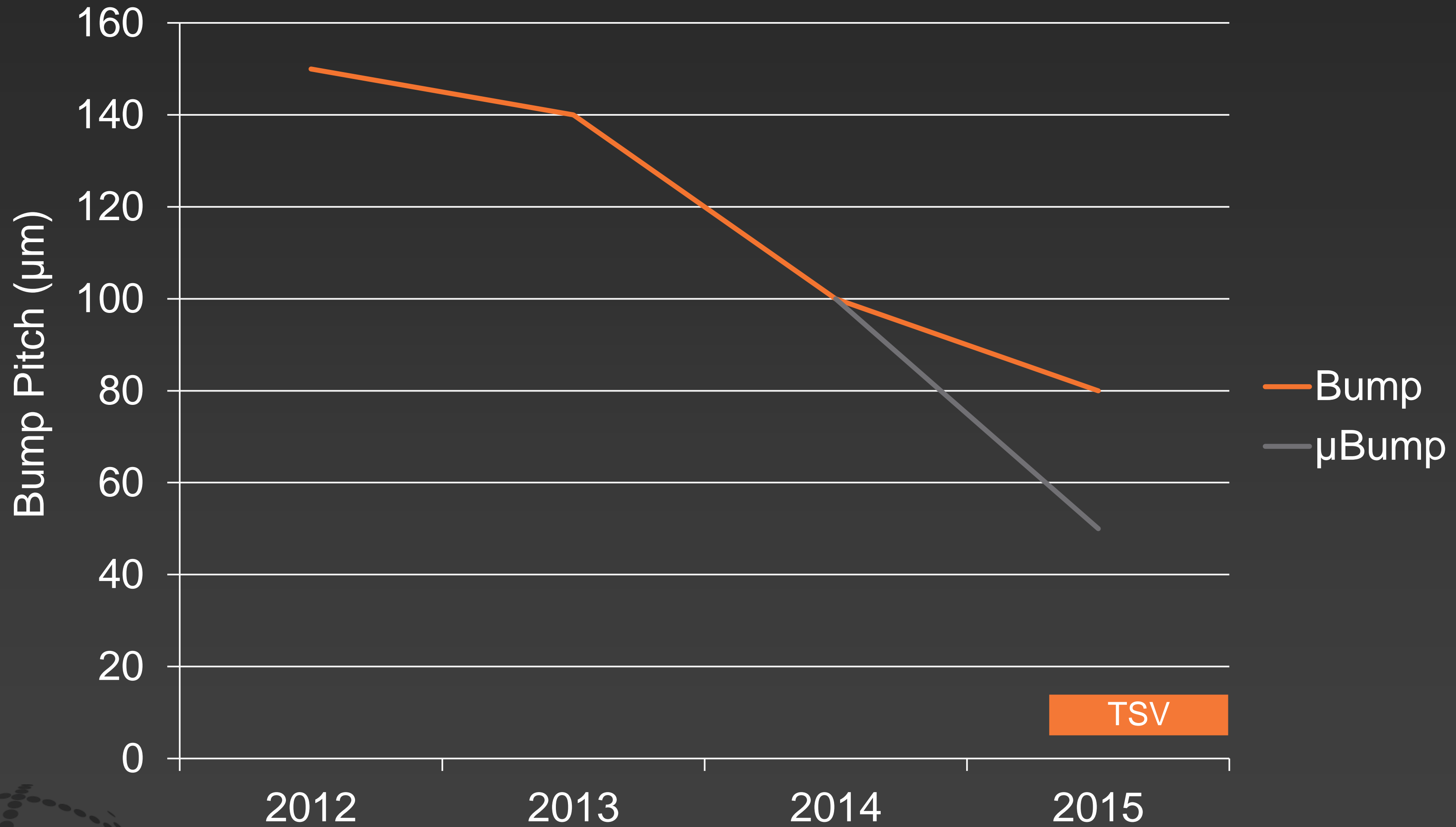
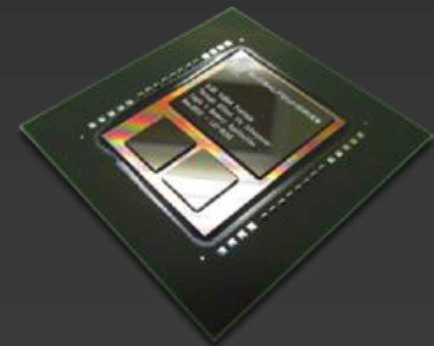
Bump Pitch (µm)

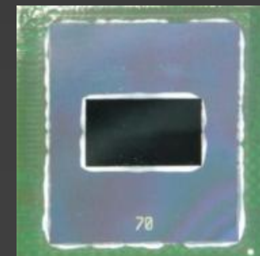
Bandwidth Drive I/O Density



But Single Die Bump Pitch Isn't Enough
Applying Packaging to Solve Scaling Limits

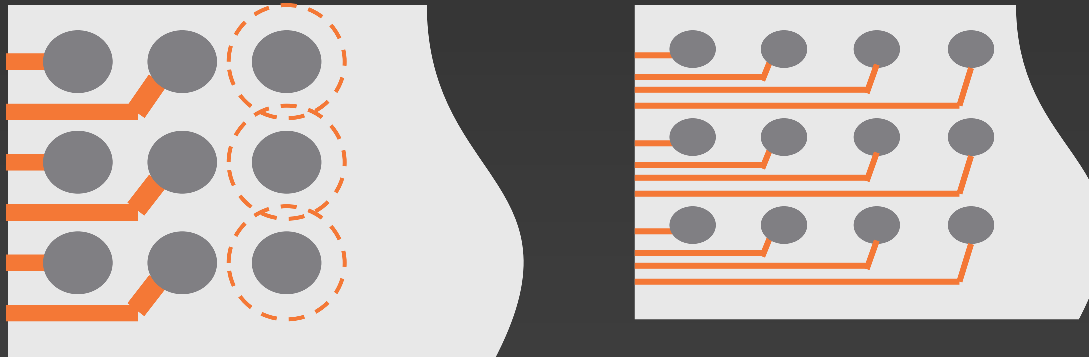
- SoC Partitioning
  - Cost optimization: Logic-Logic side by size or stacked
    - Reduced die size
    - Increased yield
  - Functional optimization: Best fit node per function
    - Design reuse without redesign
    - Lower risk – lower cost
- Logic-Memory Power & Performance
  - Logic & memory integration:
    - Increased bandwidth
    - Higher performance per watt
- Logic-Logic for Performance





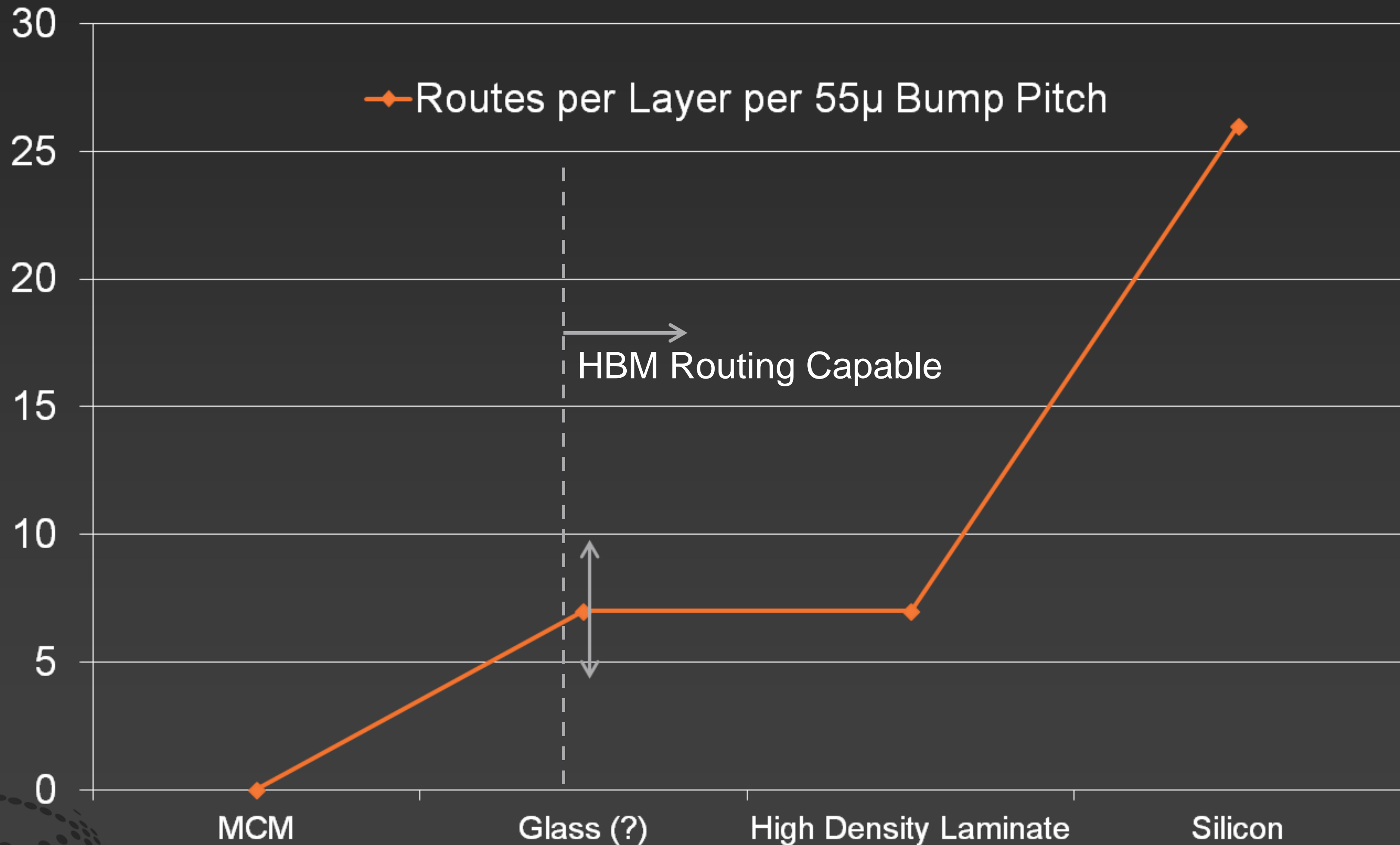
Interconnect Density: The Enabler

- Edge Routing provides challenges (side x side solutions (2.5D, WLFO) routing density:
  - 0.5µm (silicon interposer) - 5µm (WLFO)
  - Small vias needed to enable multi-layer routing
  - Shielding
  - 1 edge of 10mm die at 2µm L/S, 1/3 of lines used for shielding: 1675 interconnect
  - 1 sided routing challenges on design



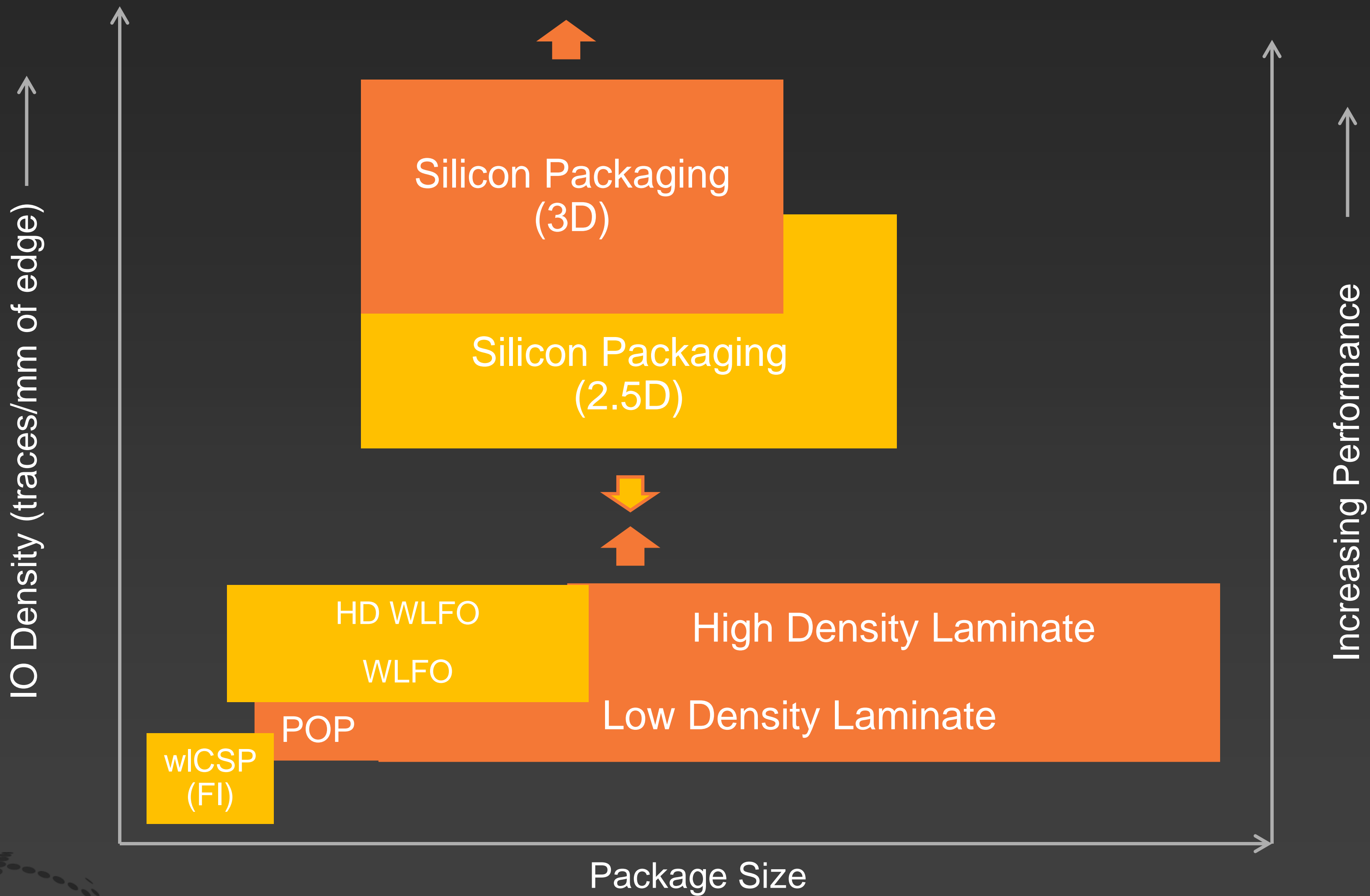
- Stacked (3D) solutions:
  - Area based: 5um vias, 2um keep-outs, 1/3 of TSV used for shielding, limit TSV to <1% of die area

HBM Memory: Routing for 55um Bump Pitch



Glass will be technology/supply chain dependent

Routing Density Solutions

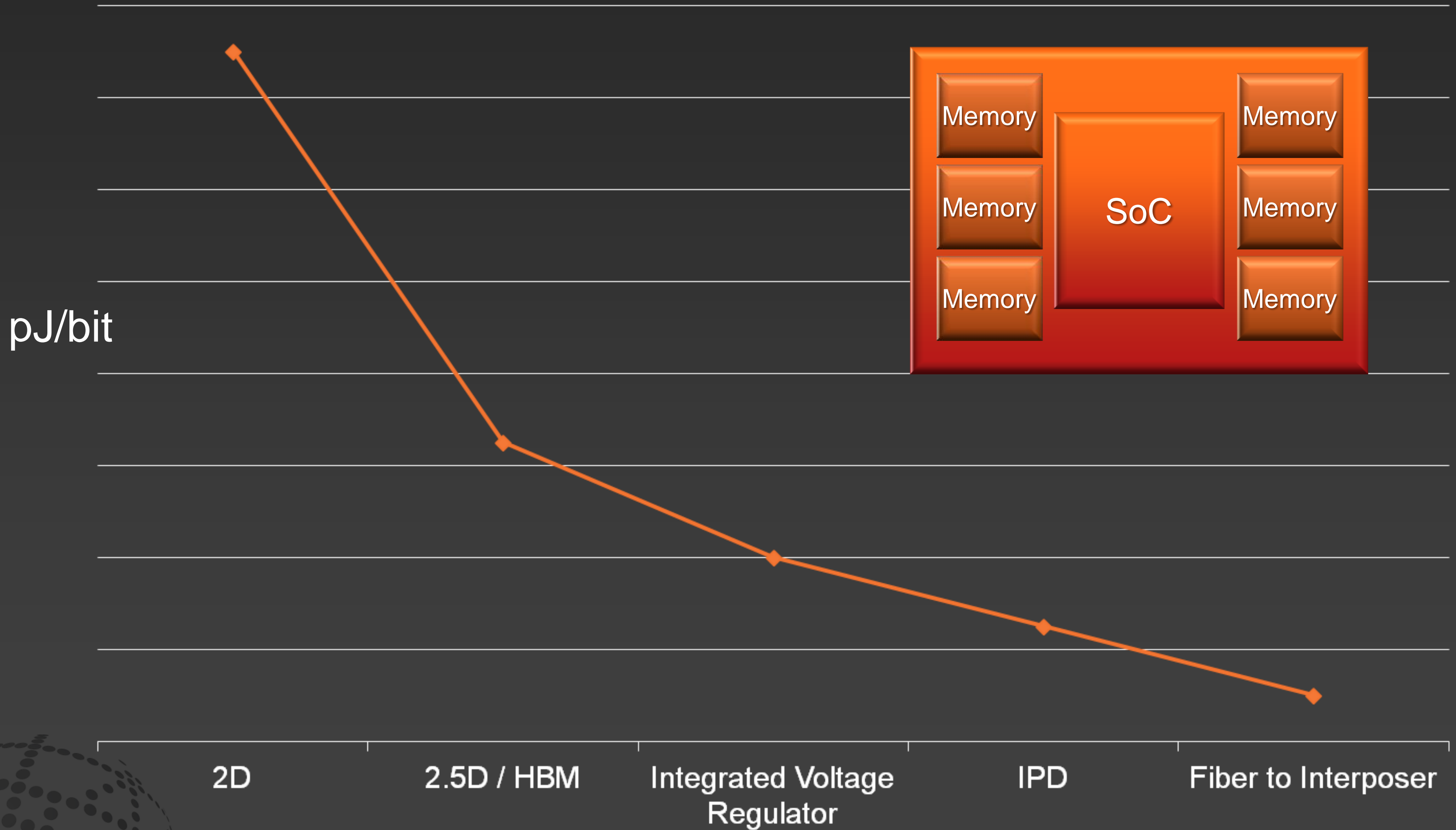


Power Envelope is Limited and Costly to Manage

- Mobile: Maximum skin temperature in smart phones requires shutdown of cores
- Computing: Power required to drive off substrate memory reduces graphics or processor performance
- Networking: > 50% of data center cost is cooling
- Memory: T_j > 80C increases the required DRAM refresh rate, increasing power and heat
- SerDes greatly reduces I/O density required between processor and memory but generates significant heat

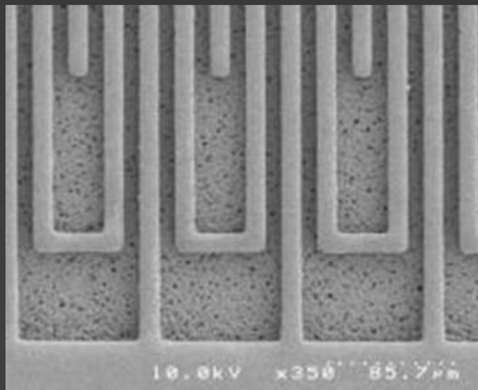
- Solution 1: Massively parallel I/O solves the heat problem but requires new technologies with very dense routing capability on substrate

Solution 2: Technological Innovation
Power Management 2.5D Roadmap

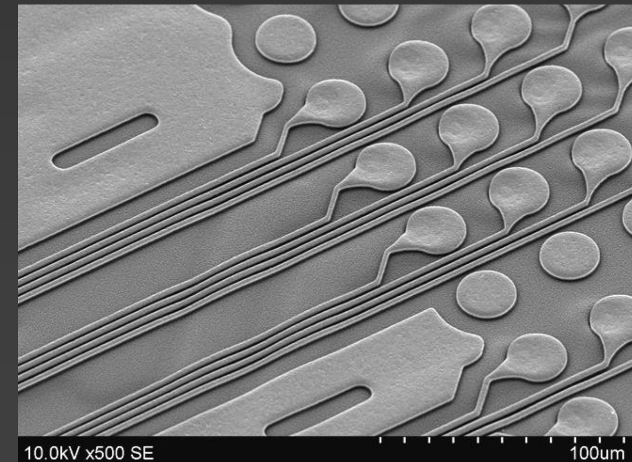


Solution 3: Are We Over-Designing?

- Architecture decisions drive interconnect density
- Decisions are often made without understanding impact on cost (and number of suppliers with capability to meet)
- Affects cost at multiple levels: interconnect, wafer test, substrate, assembly
- We need to drive cost impacts prior to design decisions Interconnect, wafer test, substrate, assembly



12/12µm L/S



2/2µm L/S

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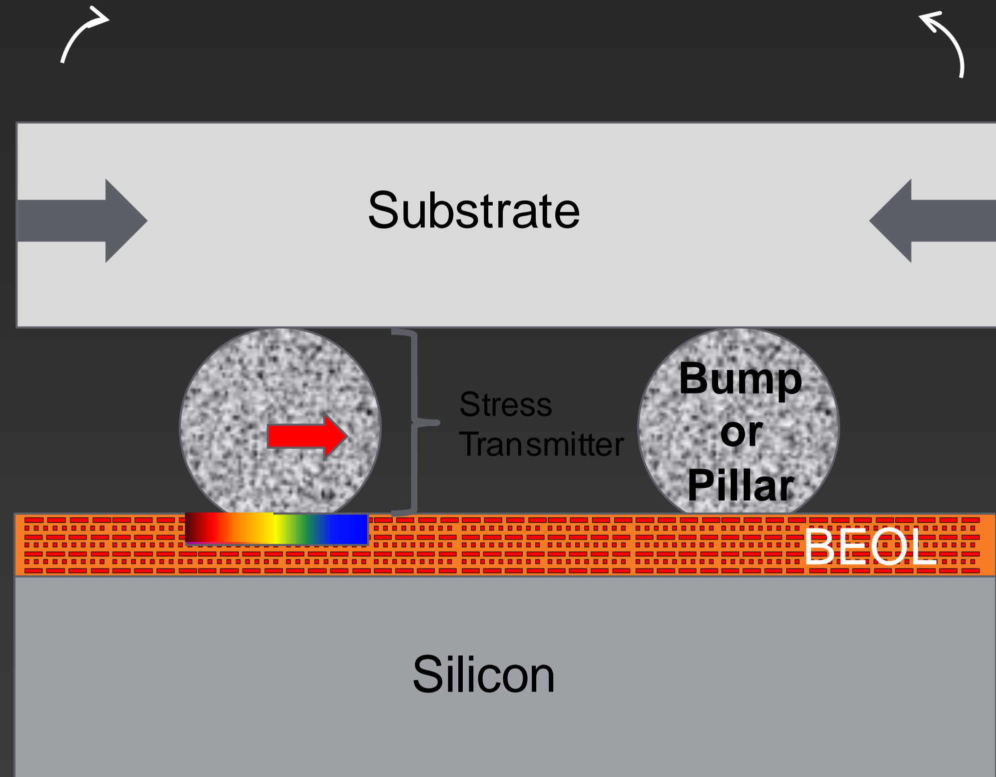
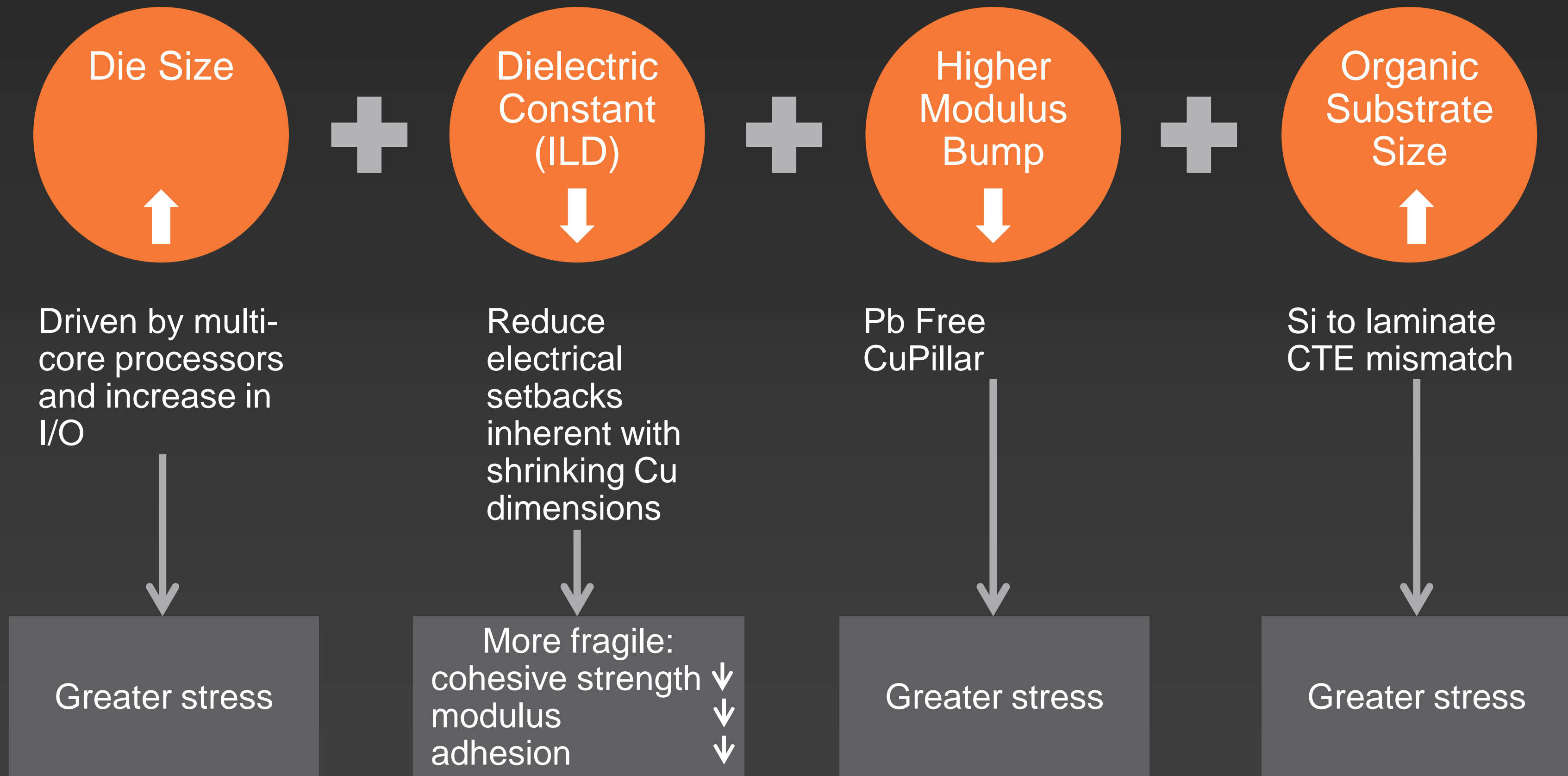
Chip – Package - Interaction

- Polyimide and BEOL layers on one side warp wafers
- There is a decreasing amount of solder to join each bump (or pillar) as pitch shrinks – ie more sensitive to warpage (O/S)
- Substrates, with higher bulk CTE than silicon, dominate warpage from reflow cool down
- Resulting stress is exerted on bump and on BEOL stack, which can break
- Detect separation by ultrasonic imaging

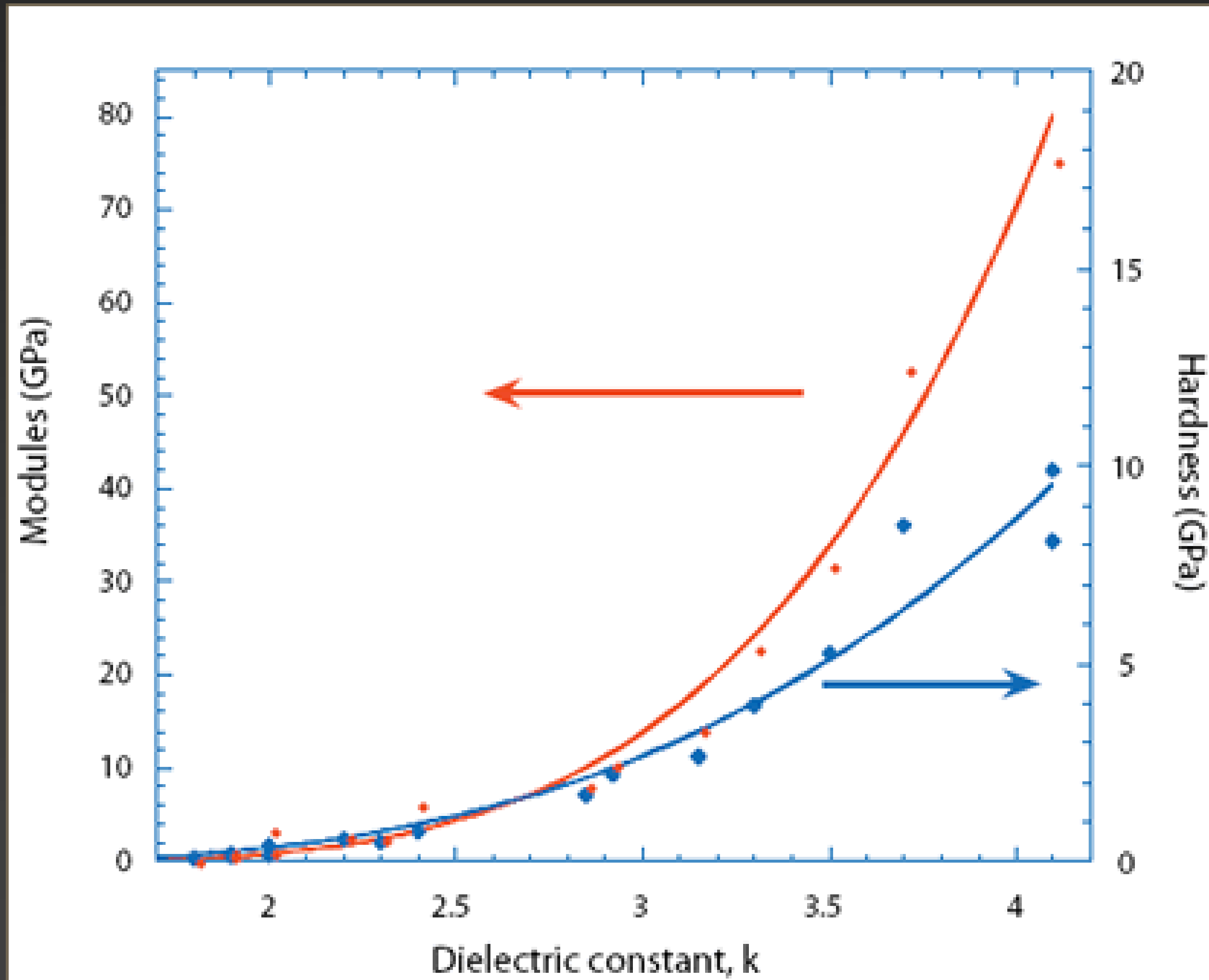


Driving CPI at Leading Edge Nodes



S.Kengeri, Semicon SGP 2014

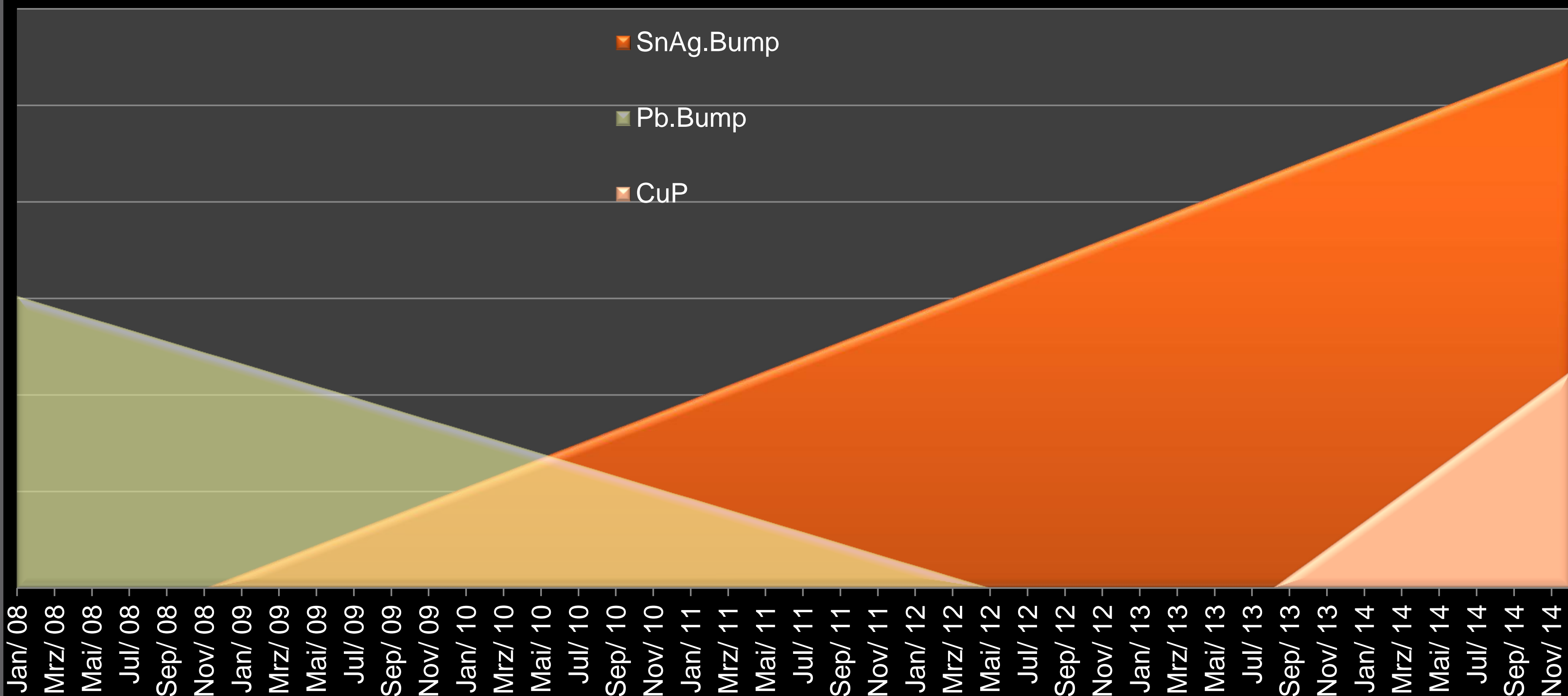
Lower-K ILDs vs. Modulus vs. Hardness



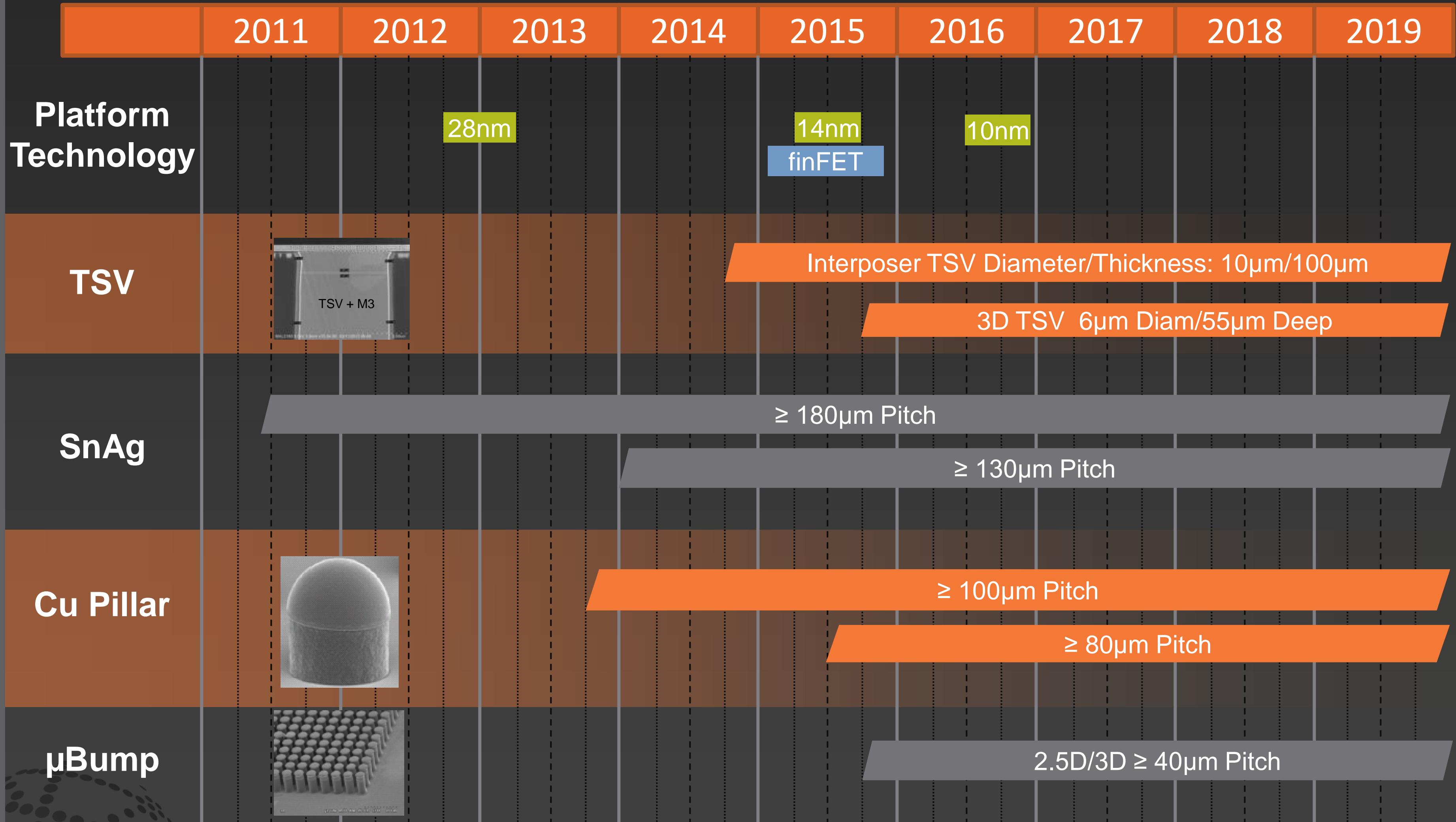
B.Chandran, intel Future Fab 2004

Bump Interconnect “Nodes”

GLOBALFOUNDRIES Bump/Probe Shipments

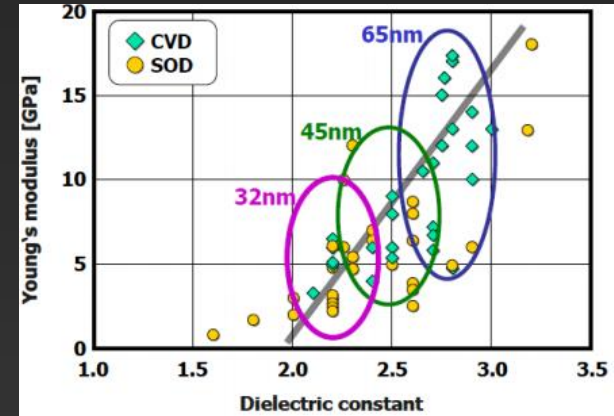


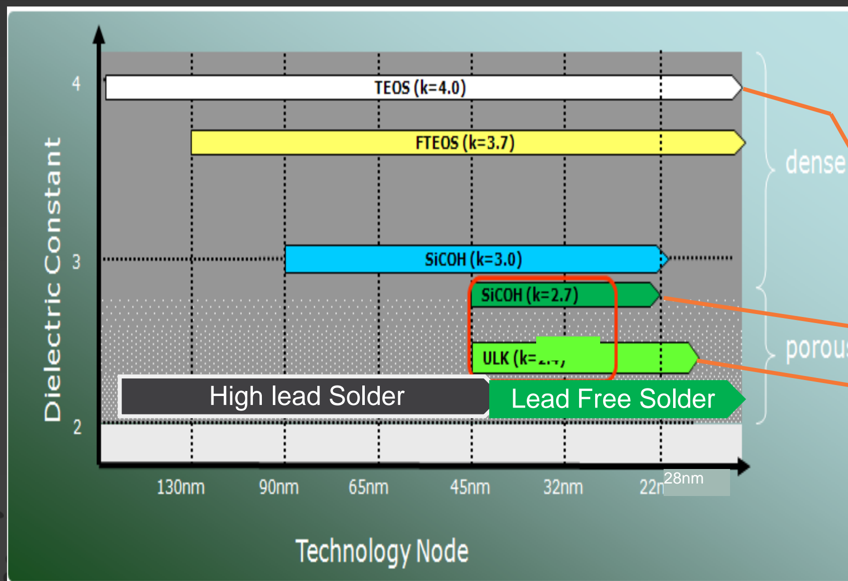
GLOBALFOUNDRIES Interconnect Roadmap

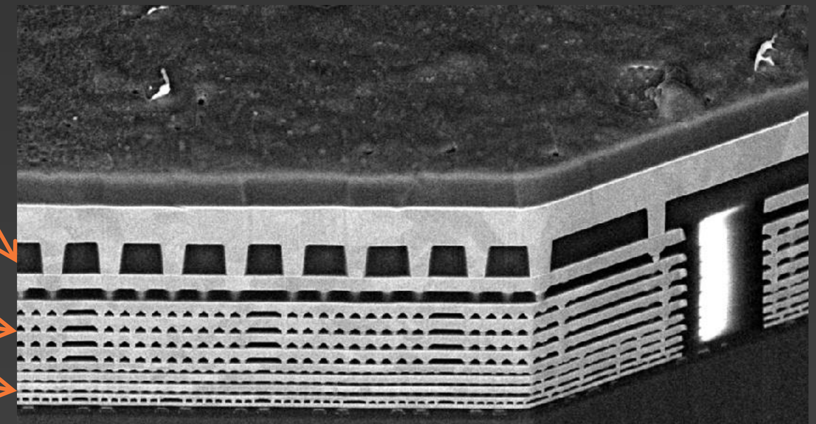


Interaction Between Design and BEOL Stack

- Weaker dielectric
- Cost driver to eliminate layers
- Tougher mechanical reliability requirements







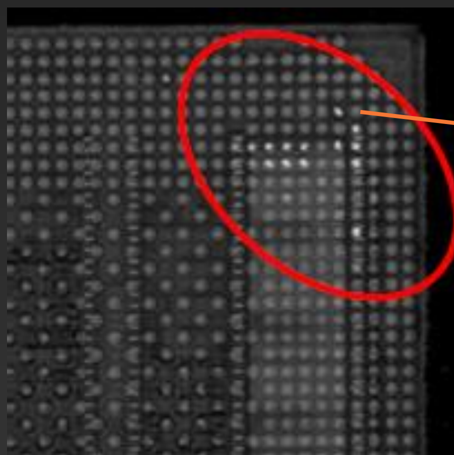
Almost 3 orders of magnitude

100um bump pitch

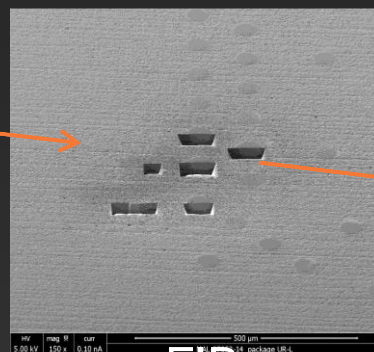
64nm silicon routing pitch

D.Breuer et al. MAM2014

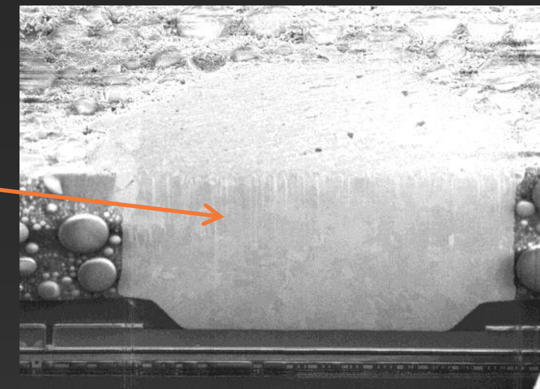
White Bump – Localized Crack Under Bump



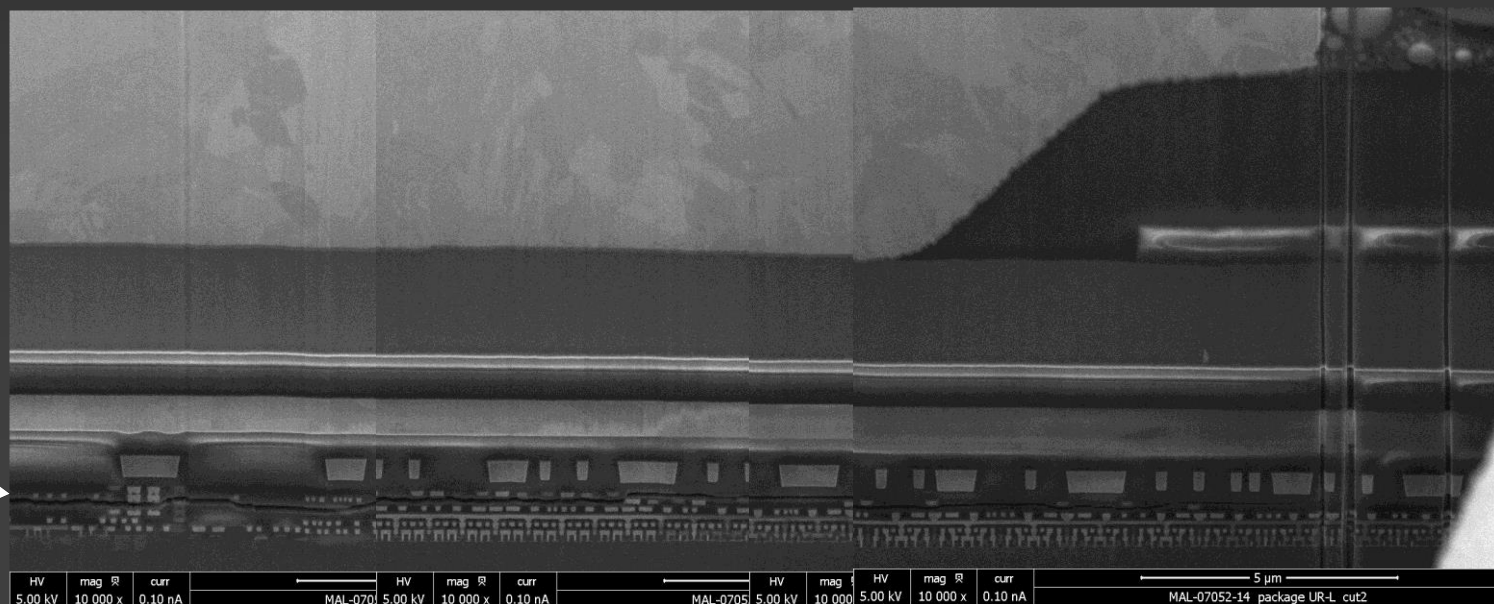
CSAM example of white bump



FIB

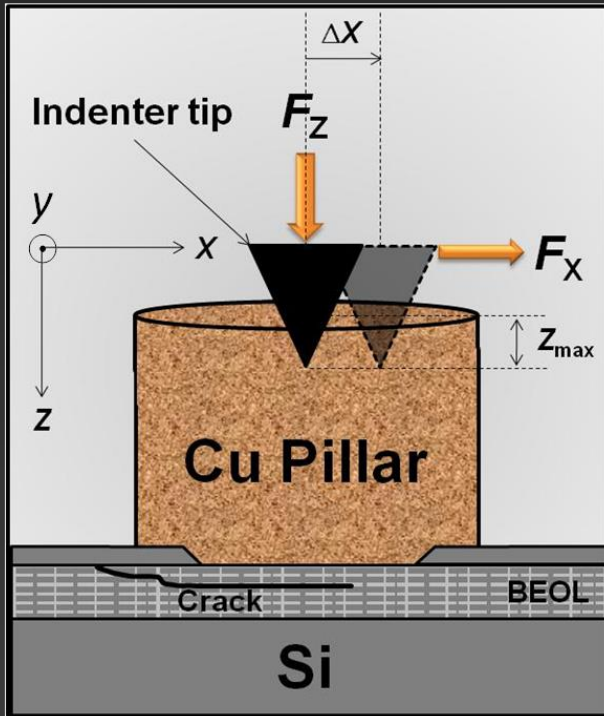


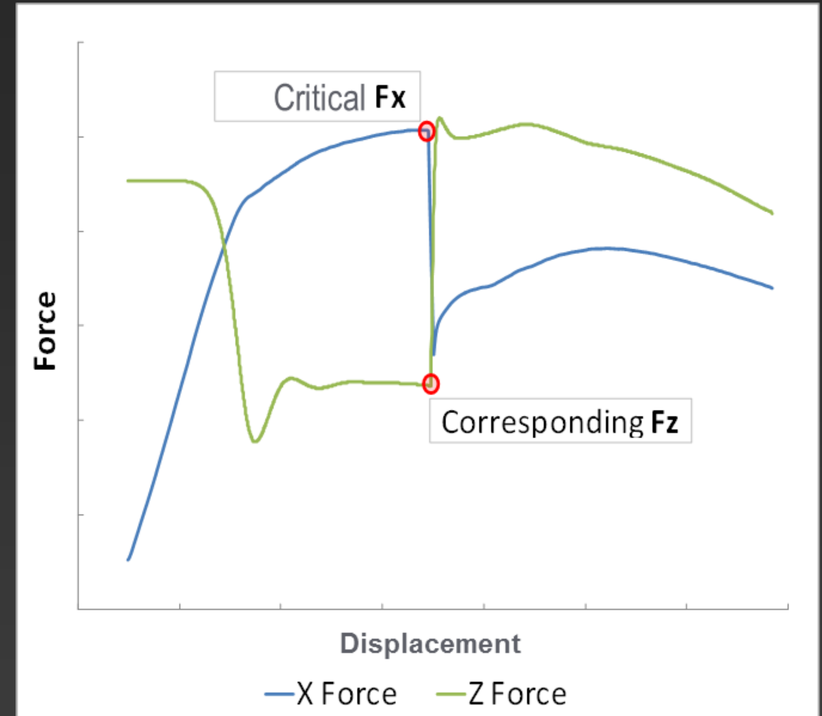
SEM

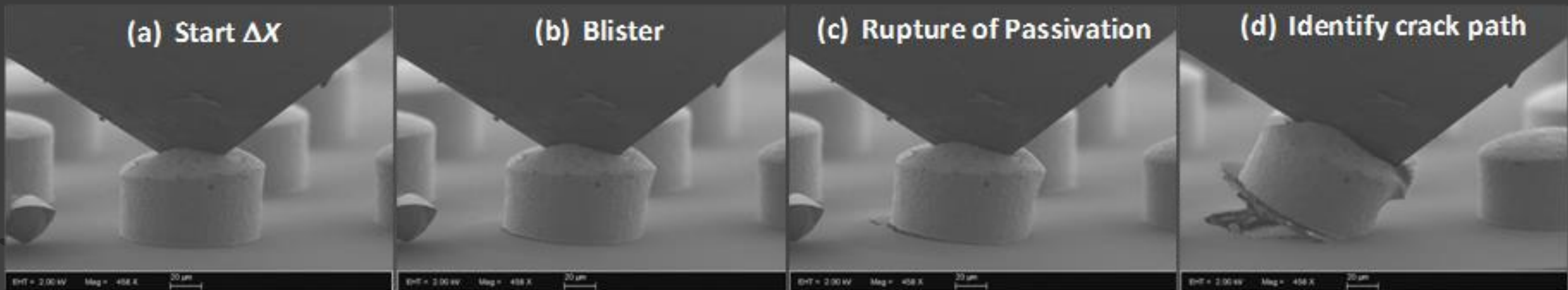


BABSI

Bump Assisted BEOL Stability Indentation





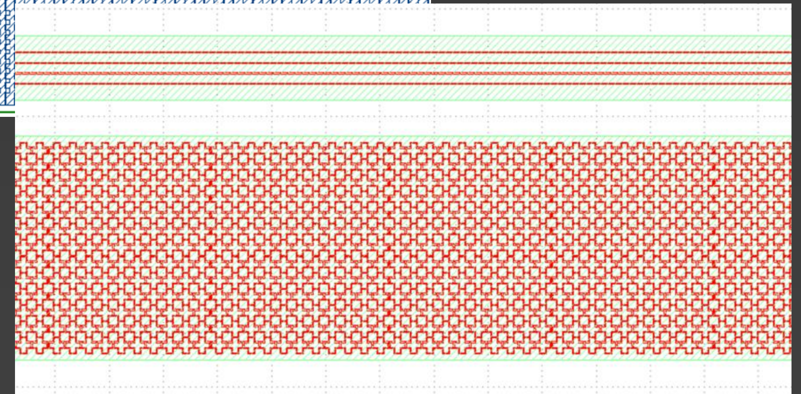


[1] H. Geisler, M. Lehr, F. Kuechenmeister, M. Grillberger, German Patent DE 10 2010 002 453 A1 (September 01, 2011).
[2] H. Geisler, E. Schuchardt, M. Brueckner, P. Hofmann, K. Machani, F. Kuechenmeister, D. Breuer, H. Engelmann "Experimental Analyses of the Mechanical Reliability of Advanced BEOL/fBEOL Stacks Regarding CPI Loading" IRPS 2013

Improve Robustness

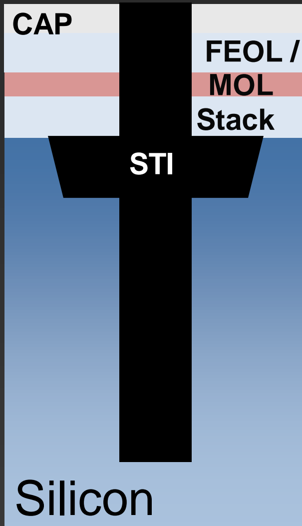
Die Edge Design

- Crack stop with interconnected metal walls; wider = stronger
- Metal fill with vias in corners to increase robustness
- Complex metal “walls”

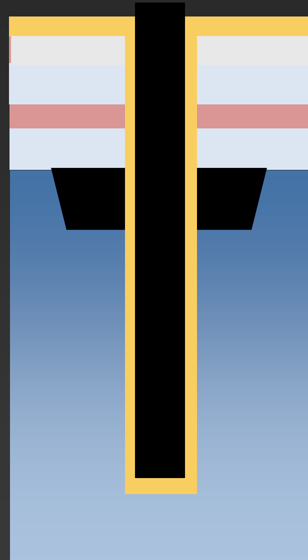


TSV Process Flow and Challenges

Post TSV Etch
Post resist strip
TSV clean

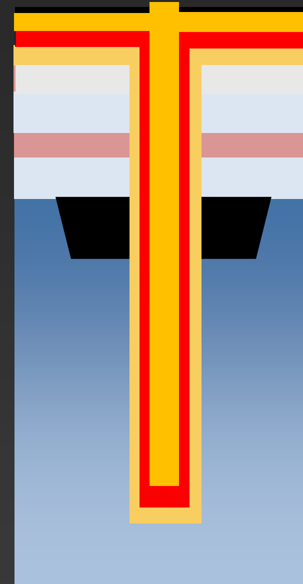


Post TSV Liner
TEOS 03

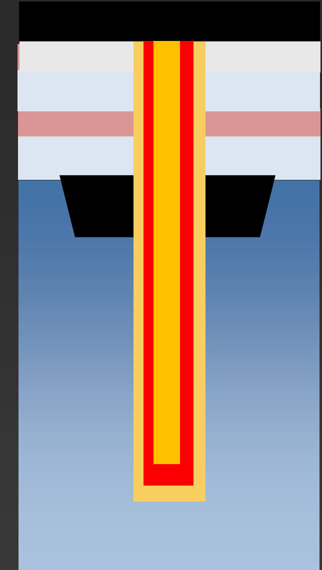


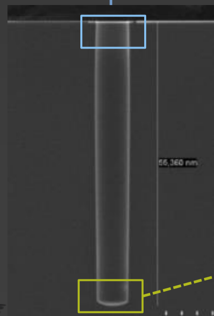
Post TSV
Barrier Seed

Post TSV ECP
& Anneal

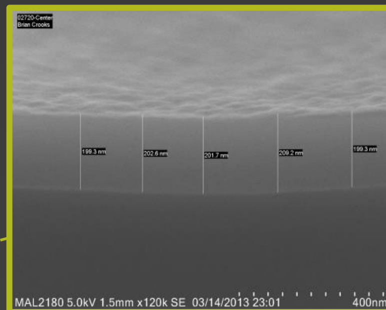


Post TSV CMP
Land on Cap

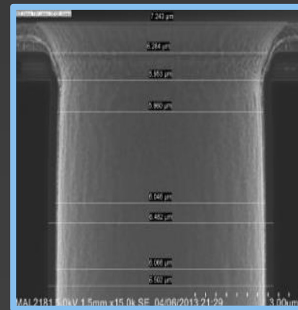




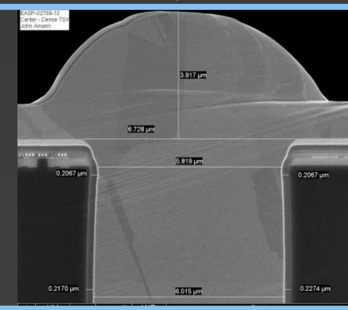
- TCD / Depth / BCD uniformity



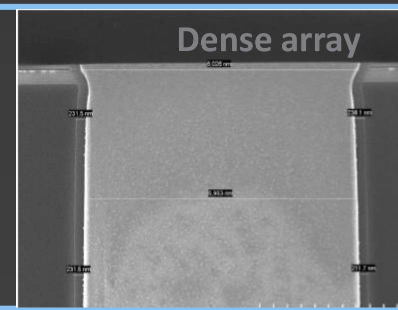
- Liner step coverage



- Barrier Seed continuity



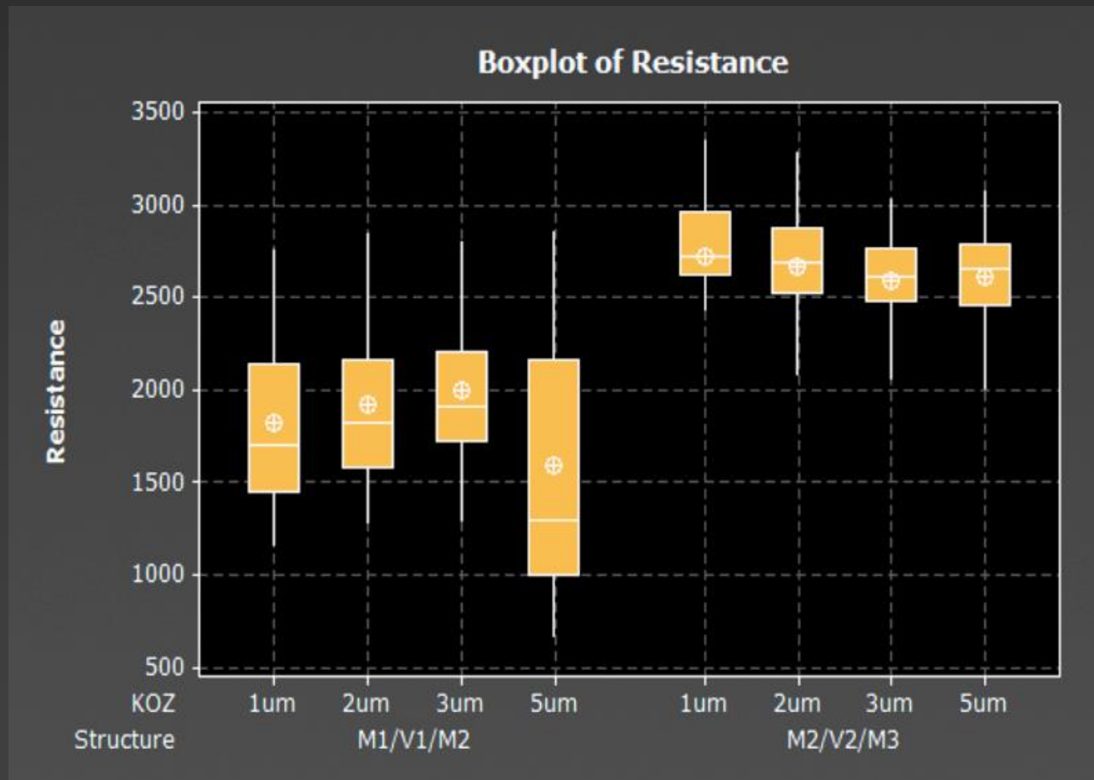
- Void free gap fill
- Overburden



- Cu step height
- Cap uniformity

Via Chains and Pop-up Structures
Electrical Test Summary

- Very low impact due on via chains with KOZ at 1μm and 2μm
- TSV pop-up structures show negligible impact of TSV and meet the target specs



No degradation as move from 5um to 1um KOZ

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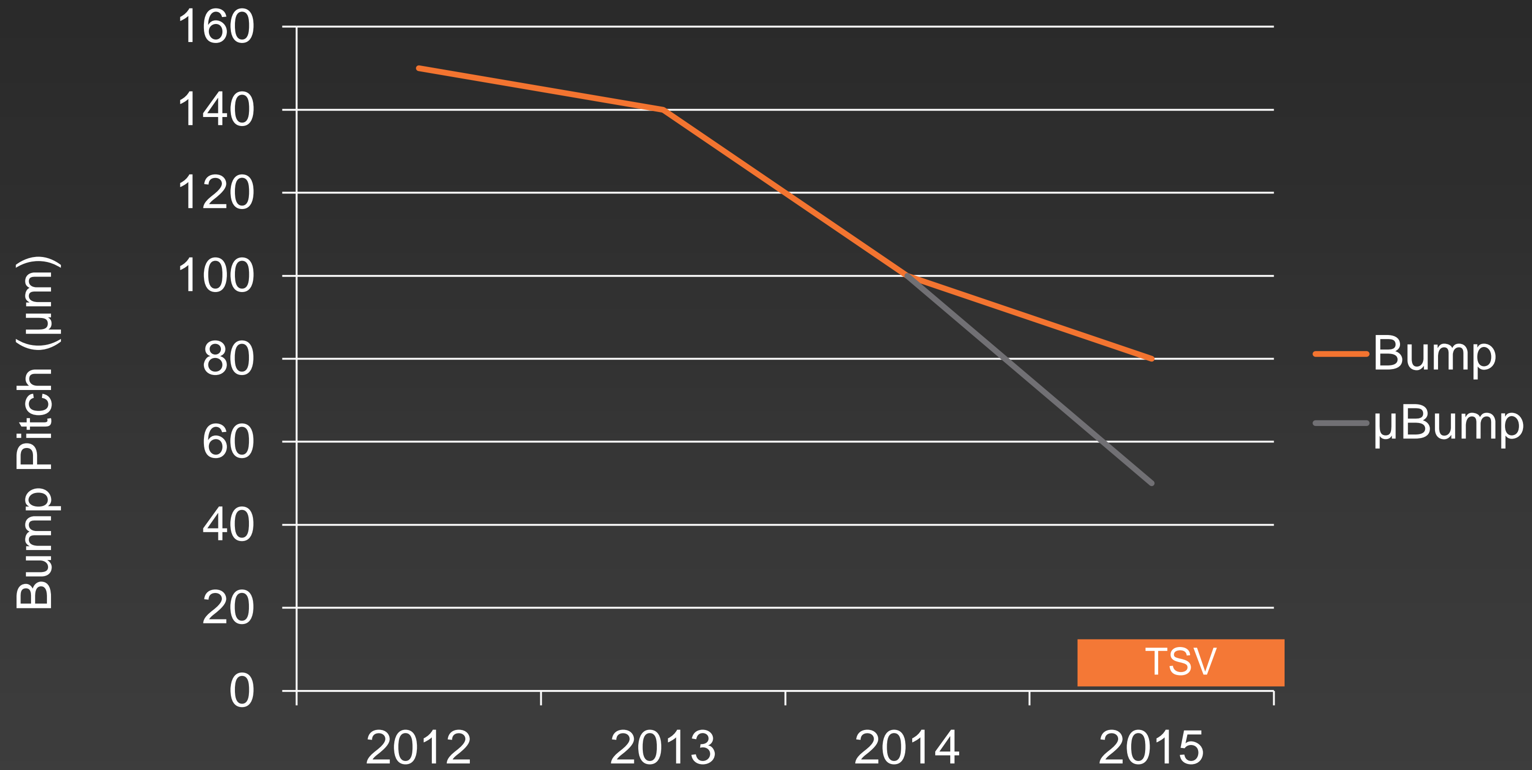
Foundry Test Business

- The Foundry does wafer test to provide fast feedback on yield to the fab
  - Critical for devices in leading edge fab processes
  - Particularly FA drives probe at the Foundry
  - Bump is required to get to wafer test
- Cost drives location of bump and probe for mature devices and nodes
- Thus bump and probe are generally at the foundry for leading edge and generally at the OSAT for HVM and trailing edge
- Customers generally provide probe cards because for the Foundry, the customer controls all input probe card costs (I/O, parallelism, product ramp, product lifetime)
- The Foundry (mostly) does not do final package test

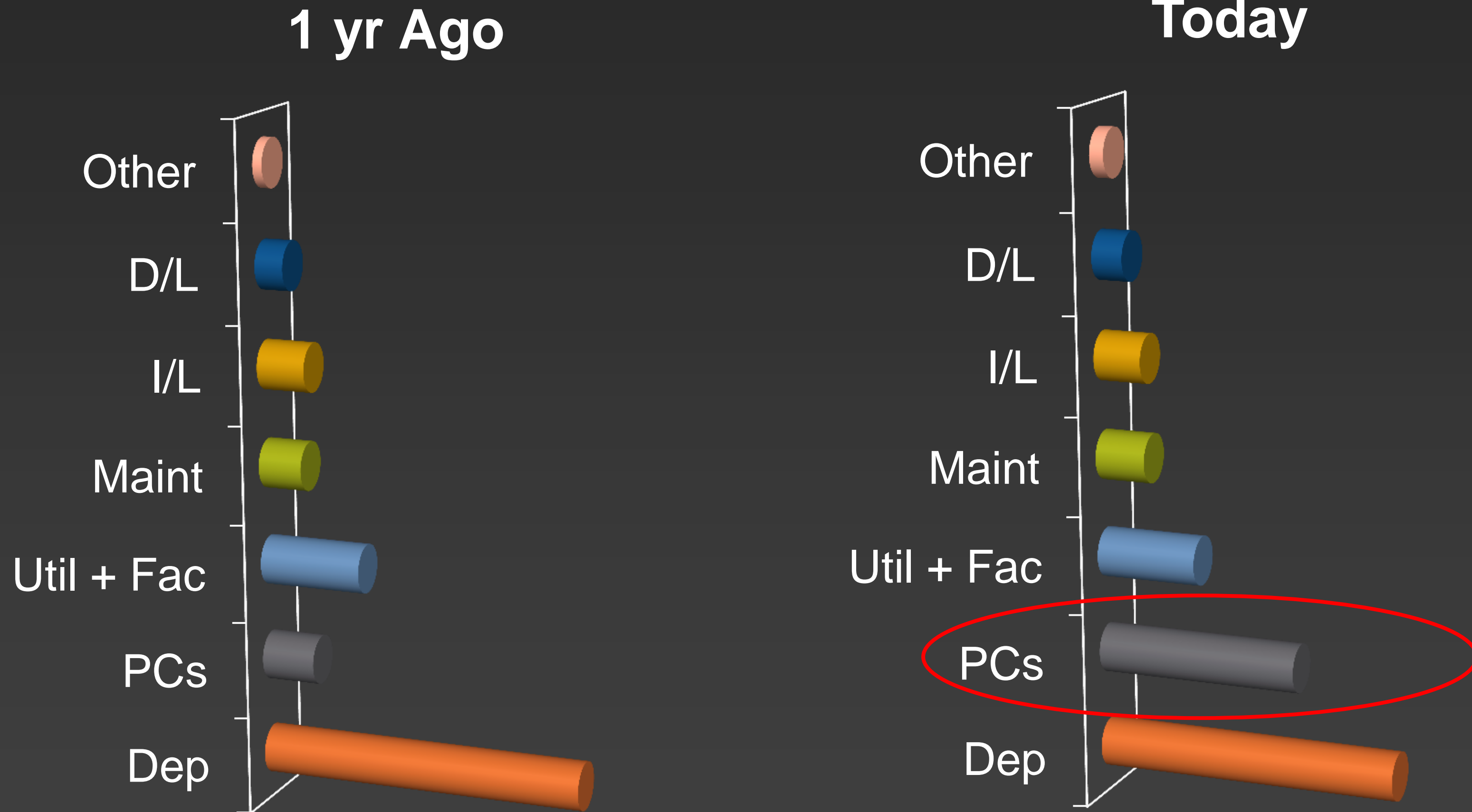
Bump Pitch (µm)



Bump Cost Trend

2012	2013	2014	2015

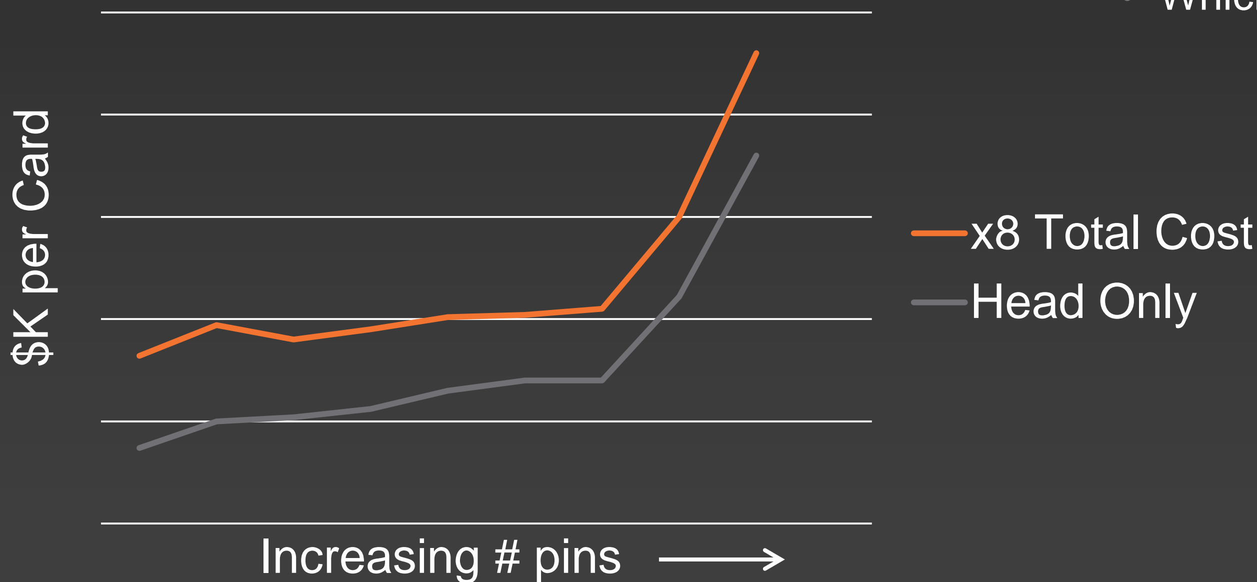
But Wafer Test Cost Composition is Changing



Probe Card Cost

- Design impacts
  - Cost of test is determined largely in device design

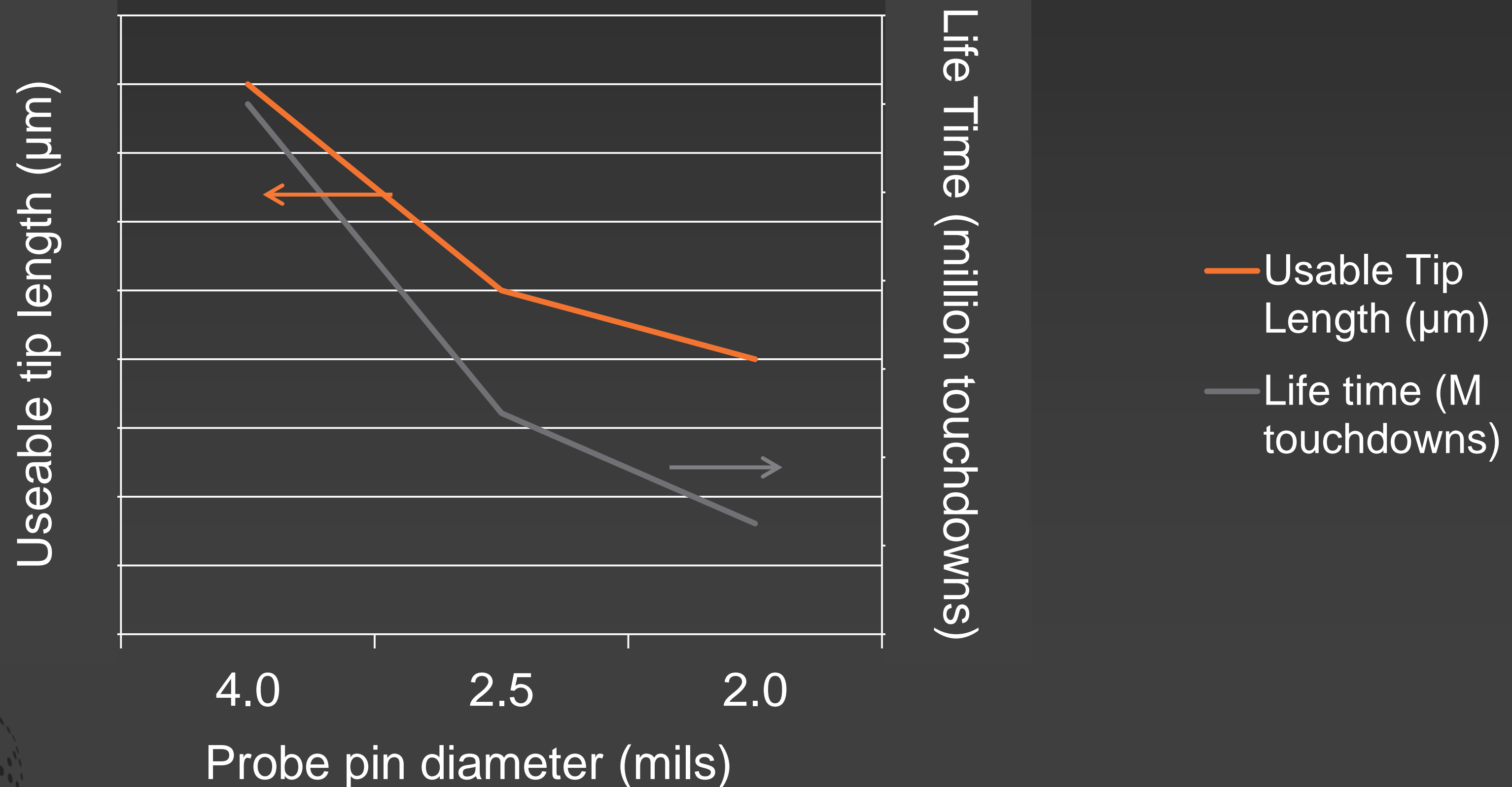
- Cost is increasing with
  - Decreasing pitch
  - Increasing probe count
  - Increasing parallelism
    - Which also drives tester cost



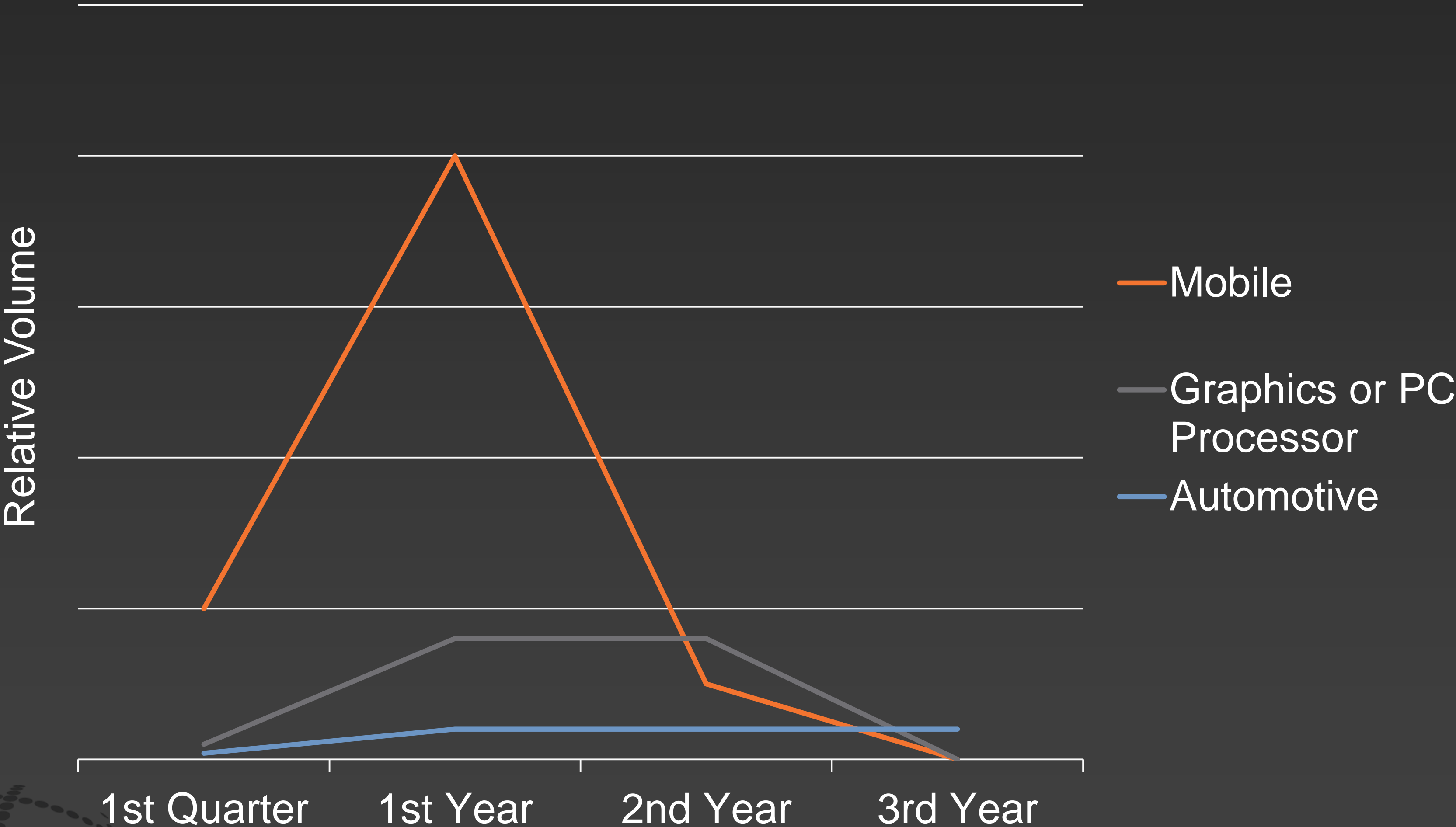
Current cost model ($10/probe) is not scalable with IO quantity and pitch

Probe Card Lifetime

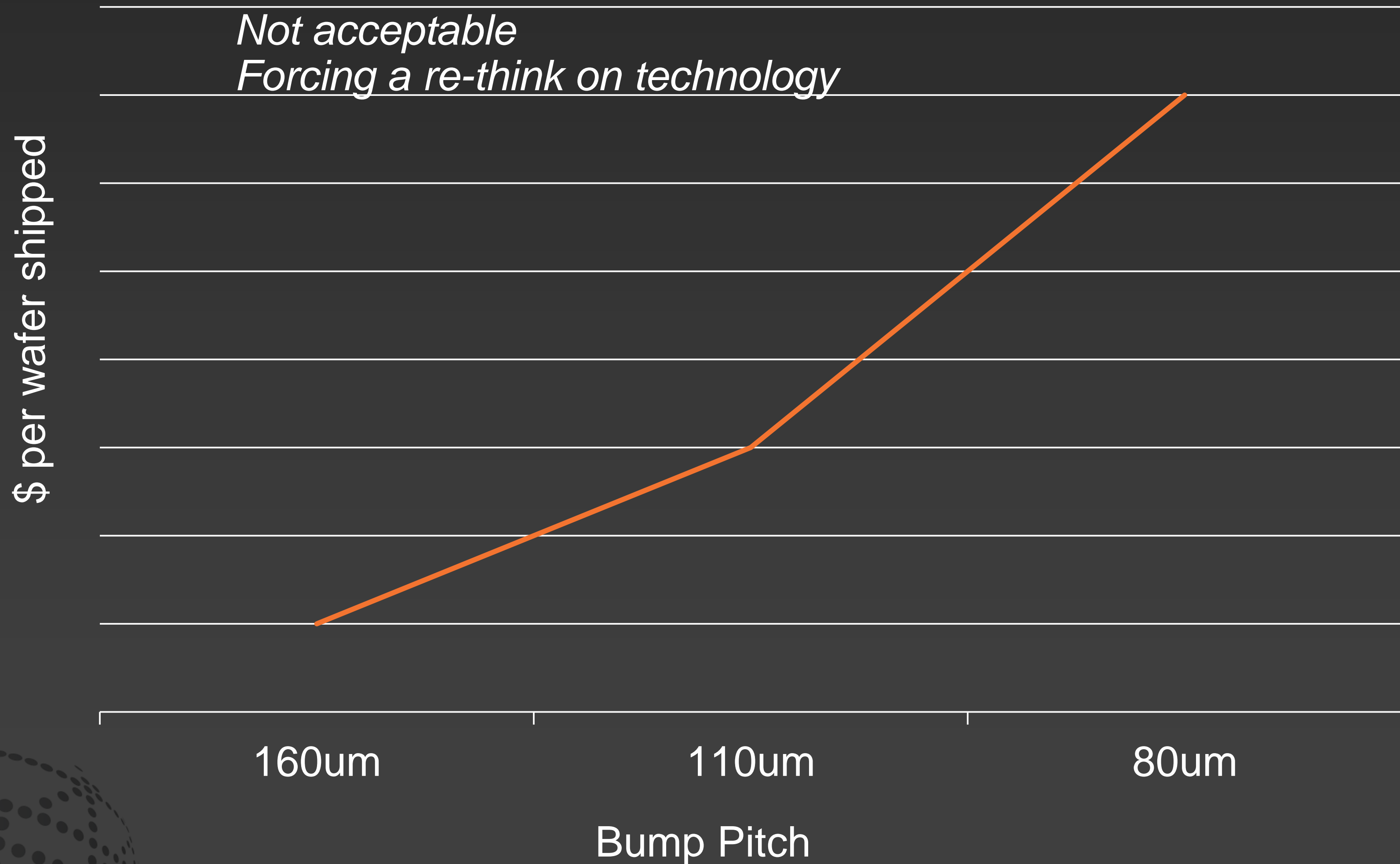
- Pitch reduction drives PC lifetime reduction
  - Pin diameter reduction
  - Shortening usable tip length



Typical Product Ramps



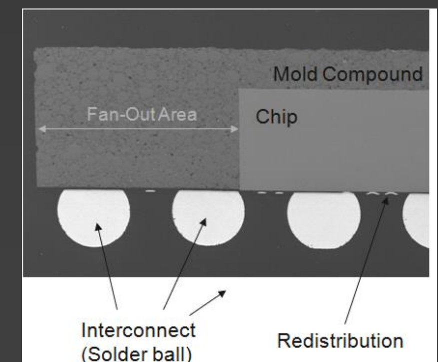
Net Probe Card Cost per Wafer Shipped



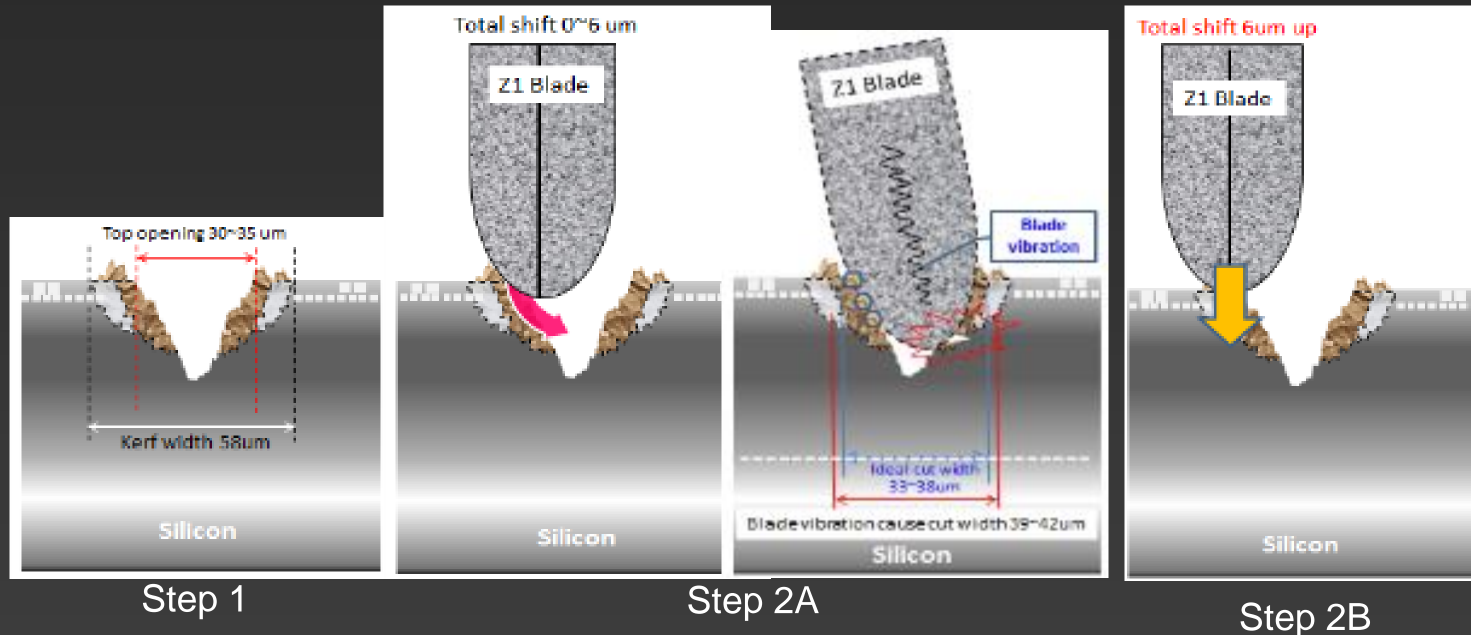
Wafer Level (wICSP) Test

WL Fan-In

- Large Turn-key Business for Foundries
- Business model is selling net-good-die
  - Close OSAT partner relationships
- Challenge is processing after test: no electrical failure detection
  - Capability and process control at blade and laser saw, pick, inspection, and in tape design critical and tends to drift out of control
  - Saw more difficult on wICSP because of high stress in thick one-sided RDL layers
- WLFO enables molding a small ring around die. Issues:
  - Cost: no satisfactory solution
  - Need either cheap safe die bare die handling or
  - Installed capacity



wICSP Crack Risk from Saw Process



Street width makes a net good die difference at these small die sizes
Laser energy decreases over time
Detection difficulty post test
Continuous attention on process control essential

Note: Drawing is not to scale.

Confidential

Wafer Probe Roadmap Challenges

- Probe card cost , particularly <100μm
- Probe technology < 80μm
  - Probe on Microbump?
  - √ Sacrificial pad?
- Utilize DfT with wrappers to reduce the number of I/O that need to be contacted?
  - Ability to re-use tester assets
  - Ability to use less dense and cheaper cards
  - But difficult for the Foundry to implement
- wICSP testing methodology

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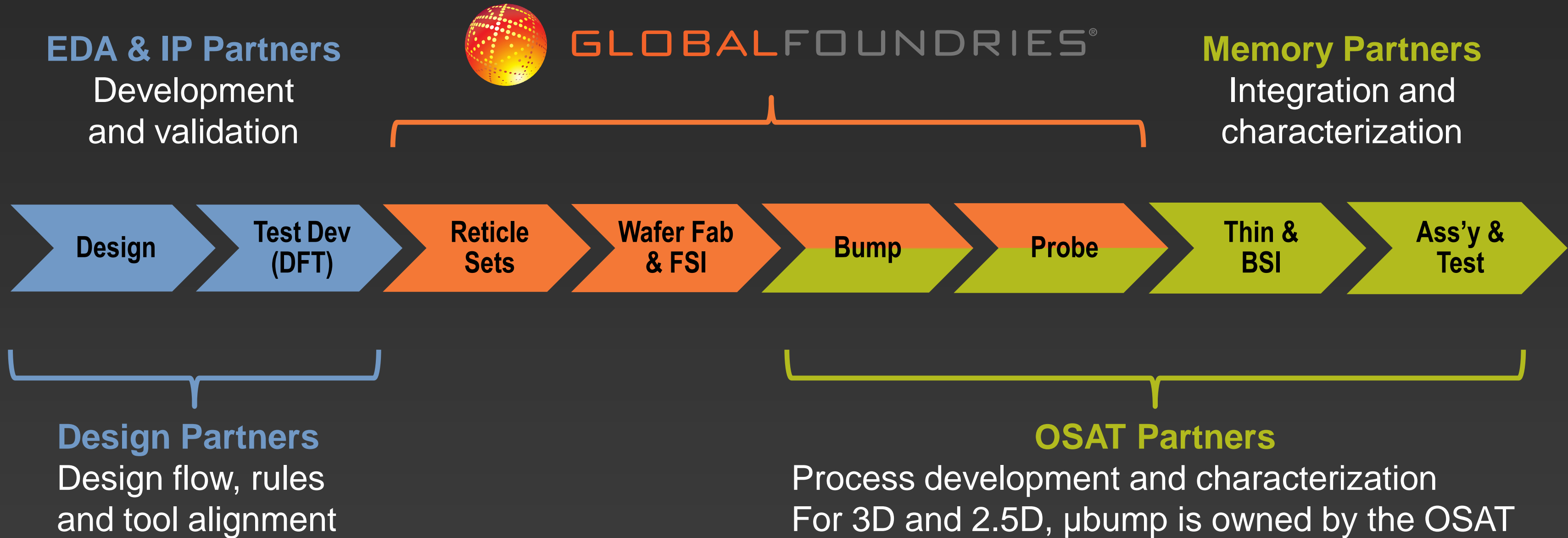
Deep Partnerships
A Collaborative Supply Chain



Customer benefits

- Open, flexible, cost-effective supply chain
- Aligns with customer's preferred partners
- Active co-development to ensure smooth volume ramp
- Suppliers don't duplicate investment and thus cost is lower

Business Model Challenges for the Foundry

- Don’t invest in what an OSAT can do better/cheaper
- Do invest in leading edge differentiating technology
- For multi-chip techologies:
  - Will competitors ship die to a competitor for multi-chip product assembly?
  - Who owns the cost of failed IC’s on multi-chip products?
- Close collaboration on development
- Priority as a ‘non-customer’

Collaboration Drives GLOBALFOUNDRIES Packaging

- ✓ CPI Qualified at 28nm with low cost FC solutions at two major OSATs
- ✓ 14LPP 2D, 2.5D & 3D Package qualifications at multiple OSATs
- ✓ 2.5D package qualified with GF interposer
- ✓ 3D TSV package qualified
- ✓ Seamless supply chain models in setup for 2.5D products

Design Capabilities
- Co-Design Reference Flows
- DFx support and tools

- ✓ Validated Interposer reference flow
- ✓ DFT enabled interposer flows

OSAT Partnerships
- JDAs at leading edge nodes
- Innovative business models

Internal Capabilities
- Bump & probe
- Turnkey solutions
- Investment in emerging technologies

- ✓ 60K/month Bump & Probe Capacity
- ✓ >15 years experience providing turnkey solutions
- ✓ 2.5D and 3D TSV enabled at Leading Edge

Memory Partnerships
- Logic-Memory Demonstrators
- Innovative business models

- ✓ 2.5D HBM integration demonstrator
- ✓ Seamless supply chain model in setup

Summary

Summary

- End of scaling at always lower cost
- Alternatives driver higher I/O density and new packaging solutions
- The new solutions drive higher cost test and downstream costs (substrate)
- Advancing silicon technology presents material and stress challenges that must be characterized.
- Must have significantly cheaper probe card technology and questioning of cost of test at design
- Need high density substrate solutions at lower cost
- The collaborative supply chain enables accessing best expertise at lowest cost

Thank you to:

Jens Kober – Probe Dev and Production

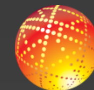
John Carulli – Test Development

TM Mak – DfT and IP 2.5D/3D

Jens Paul – CPI Reliability

Rama Alapati – Product Mgt for Packaging

Thank you



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