SW Test Workshop
Semiconductor Wafer Test Workshop
June 7 - 10, 2015 | San Diego, California

Reduce wafer test with 3% to 10%+ by optimizing touchdown patterns

André Stoelwinder

OrangGO - PDF Solutions Service Provider

Aagje Dekenstraat 51, 8023BZ, Zwolle, The Netherlands

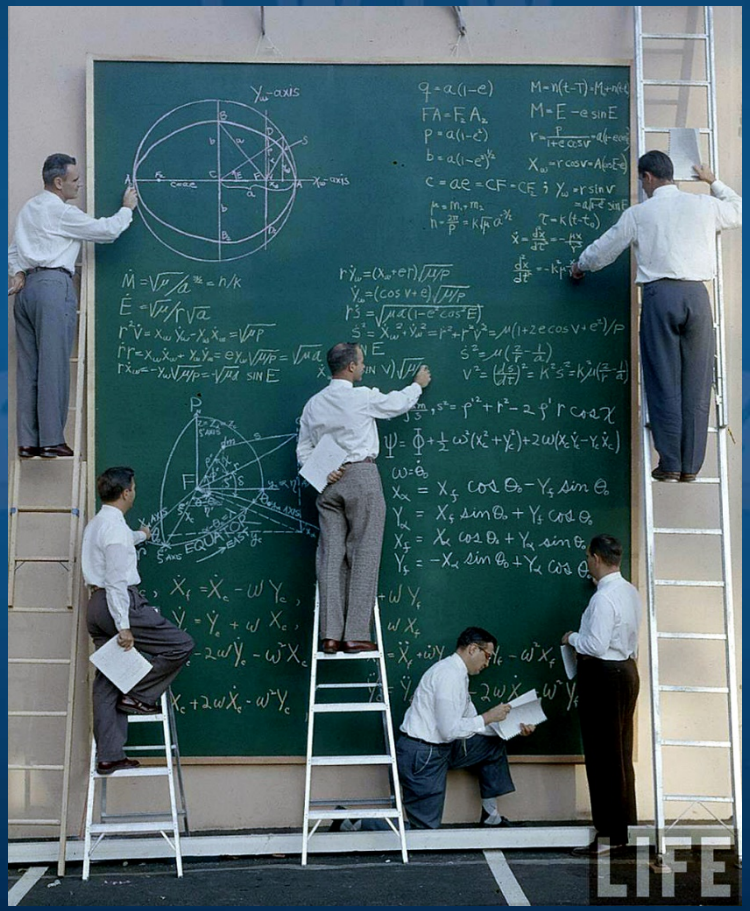
andre.stoelwinder@oranggo.com

Overview

- Introduction
- Objectives / Goals
- Background
- Traditional touch down optimization
- Tool Requirements
- Use Cases
- Achieved optimization results
- Talking about cost and savings
- Summary / Conclusion

This paper is not about

complicating stuff…



It's a pragmatic approach

The issue

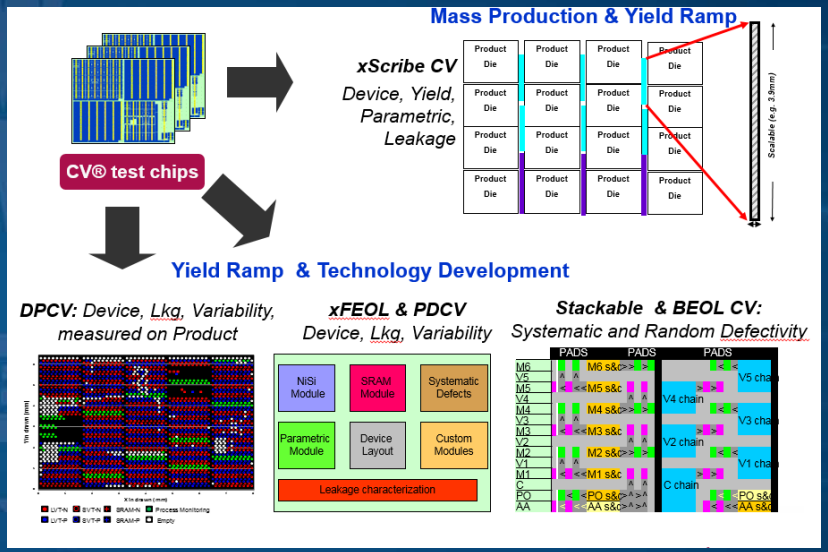
- **Cost of test is under pressure**
- **Quality should be as high as possible**
  - Post processing, outlier detection, test time optimization
- **Probe card shapes dictated by product requirements**
- **Limitations of equipment**
- **Speed of change**
- **Need to have shortest wafer test time as possible**
  - Without compromising on quality

Objectives

- **Test as efficient as possible**
  - Least amount of touchdowns
  - Only where it is needed
- **Overcome limitations of prober**
  - Supported patterns
- **Industry requirements**
  - RF requirements
  - Higher demands of parallelism
  - Elevated temperature testing

PDF Solutions

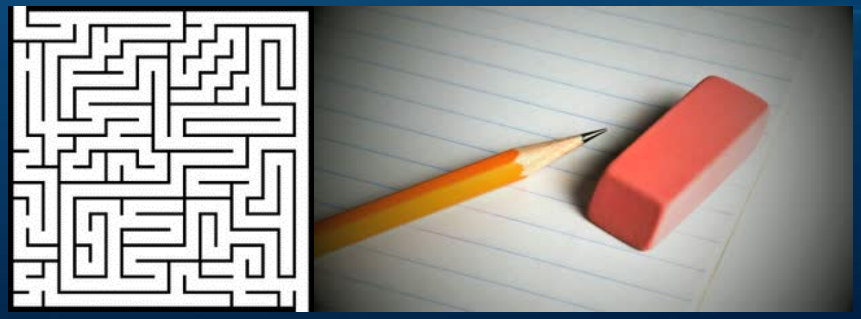
- **Product lines**
  - Char
    - PDF CV Test chip characterization. PB+ data analyzed.
  - Control
    - Also known as Maestria: Control of process tools (FDC), and leveraging this data with other data types.
  - Yield
    - Also known as dataPOWER VSF: Ad-hoc engineering analysis, focused on both casual user and engineering users.
  - Test
    - Control of test cells, test optimization, efficiency, adaptive test. Leveraging with other data types.



More info at www.pdf.com

Traditional

- **Manual labor**
  - Looking at shape of probe card.
  - Determining based on experience what might work or not.
  - Trying to optimize manually by adding touch down positions.
  - Finding out after one hour that maybe should have started differently.
  - It's a puzzle.
  - Time or TIME.



Traditional results

- **Good achievement**
  - Saved 5% -> Happy

BUT……

What if…

- What

9

Time… Precious

Need a tool that is…

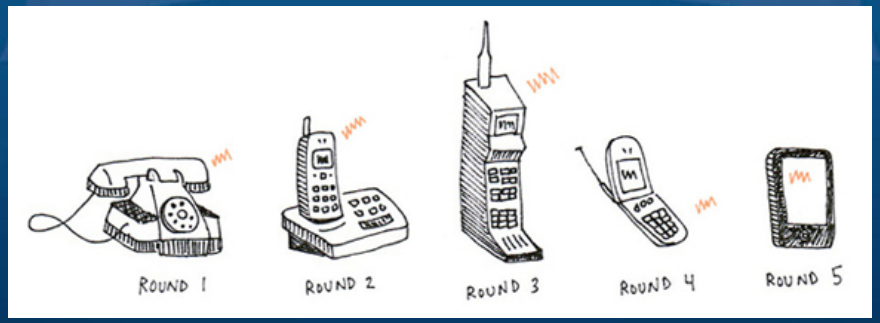
- **The right balance between features and usability…**

Tool requirements

- **Ease of use & Fast**
- **Rule set**
  - On wafer, off wafer, or…
  - Multiple touch downs, yes / no, or…
  - Process step support
  - Routing
- **Debug capabilities**
- **Fine tune capabilities**

Tool requirements

- Needs to support standard probers
- Needs to integrated solution in Exensio-Test
- Needs to support customer automation
- “Trial and Error” friendly



Tool History

- **The Tool**
  - Initially released in 2004 in Cell Controller
  - Improved over time
- **Customer feedback**
  - Standalone solution
  - More complex probe card layout requirement
- **2014**
  - Made available as separate tool
  - Re-designed architecture to support changing requirements
  - Dramatic speed increase and feature improvements

Use Cases

1. **Generic optimization**
   - No specific rules. How to determine best probe card layout?
2. **Odd shaped probe card**
   - What if probe card size gets too big? Alternative shape.
3. **Determine best number of sites**
   - Evaluate number of sites against touchdowns.
4. **Fine tuning strategies**
   - Specific tester requirements handling.

Bench mark results

Actual results achieved

Product	No Die	Sites	Non optimized		Optimized		Touch down reduction	**Test time reduction**	Comments
			TD	Wafer test time	TD	Wafer test time			
A	2483	8	351	0:38:59	329	0:37:03	22	**5.0%**	Optimal layout
B	554	4	156	0:41:29	149	0:39:43	7	**4.3%**	Same layout
C	33239	16	2331	5:14:45	2217	5:04:47	114	**3.2%**	Same layout
					2120	4:56:17	211	**5.9%**	Optimal layout
D	2269	16	210	0:25:56	184	0:23:39	26	**8.8%**	Same layout
					158	0:21:23	52	**17.5%**	Optimal layout
E	6074	32	228	0:40:12	209	0:38:32	19	**4.1%**	Optimal layout
F	246178	32	8426	7:48:57	8110	7:08:08	316	**8.7%**	Same layout
					7809	6:29:15	617	**17.0%**	Optimal layout
G	2483	16	179	0:23:56	171	0:23:14	8	**2.9%**	Optimal layout

Return Of Investment

- **Based on**
  - 15 wafer sort Cells, 5 Products / Cell
  - 5% on Touch Down reduction
  - 0.5% on index time reduction

Investment
Running Cost
Etc…

Benefits
Return of
investment

ROI Calculation

Use Cases Capex,Opex,Quality (Custome	
Opex/year	**Input selection**
Software tools	$5.000
Training	$1.000
Utilities (power cooling)	
Maintenance/y	1,5%
Process cost (testting,scanning,probing,inking)	
Respider cost	$12
number of touchdown before respiders	500.000
probecard spending per year -->device sp hw	1

Resources/year	Input selection
Operator hr cost	
Number of cells/operator	7
Operator hrs/incident (rework-support)	10
Engineering hr cost	
Average probecard inspection/repair time (hrs) /lot	2
Engineering/technician allocation+overhead /cell	10,00%

Process specific (customer input	
Device Specific Average numbers	**I sel**
Product Test time (nett) (s) WS	
Index time (s) WS	
Average spare probecard factor	
WS yield	
calculated tester hr rate (capex only)	$
Hardware margin	
calculated tester hr rate (capex+opex)	$
Hardware margin tester rate	
parallel sites ws	
Back grinding cost/wafer	
working days (7 d 24 hr shift)	
cell efficiency (including retest ,setuptimes,waittimes,...)	
Wafer cost	
Device specific hardware cost	$
Average product cost (after wafersort)	
Wafer lot size	2
GDW	
waferloading/unloading sec/wafer	
Cleaning/PMI sec/wafer	
Number of touched pads per device	

PDF Solutions proposed inputs.	
Tool opportunities	**Input selection**
Process Efficency improvement %	5,50%
Optimised (shorter) probe route % of test time	0,50%

Business opportunities	Input selection
New business	0%

Probecard related	Input
# touchdowns reduction %	5%
probecard lifetime extesion	5%
Probe card balancing lifetime effect - (catastrophic failures)	2%

Optimization	Input selection
wafer recipe generation engineering hrs	40
optimal # sites calculation engineering hrs	8

Quality improvement	
Yield improvement	0,50%
1,2,3, crash site optimizer	n.a

Salaries & Utilities

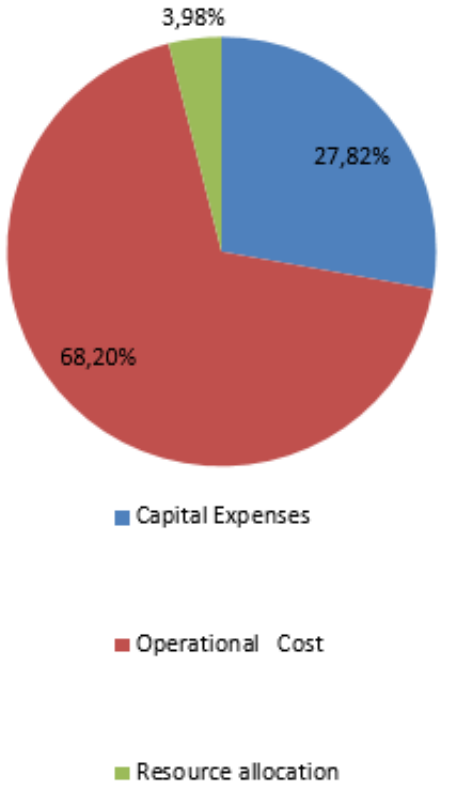
Asian Region Cost source JETRO (Japan external Trade organization)					
Region		Worker/hr	E	Industrial Estate sqm/year	Elec kwh
Shanghai		$2,81		$540,00	$0,13
Guangzhou		$2,47		$324,00	$0,12
Shenzhen		$2,05		$324,00	$0,12
Hong Kong		$10,12		$1.884,00	$0,19
Taipei		$7,14		$216,00	$0,13
Singapore		$7,68		$916,00	$0,23
Bangkok		$2,15		$252,00	$0,11
KL		$2,15		$288,00	$0,11
Batam		$1,11		$144,00	$0,06
Manila		$1,88		$240,00	$0,27
Cebu		$1,36		$132,00	$0,24
Average 2012		$3,72		$478,18	$0,16
Indexed	**20,00%**	**$4,46**		**$573,82**	**$0,19**
Engineering US/Europe					

Cell utilities		KWh	Energy Cost/hr	$11,64
Tester KWh		28		
Handler/prober/probecard repair/other equipement Kwh		10		
Cooling cap 1kBTU~0.3KWh		22		
Other facilities (ligth , compressed air , vacuum , etc , etc)		2		
Total Power		62		

	year 2	year 3	a	year 5
Power cost increase (estimated)	**5,00%**	**10,00%**		**10,00%**
Resource cost increase (estimated)	**8,00%**	**9,00%**		**12,00%**

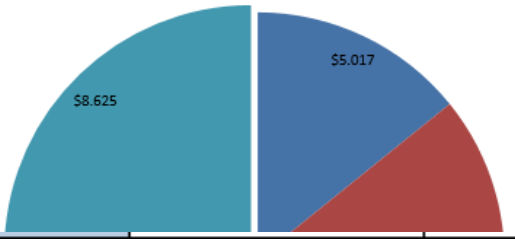
Process Cost Cell / Year

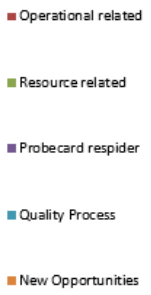
Process cost Parameters cell/year				
Parameters		Optimizer <-->Testcell	Value/year	Relative
Capital Expenses	Equipment	Tester , prober(depriciated)	$83.333	
	Infrastructure	Building/facilities (depriciated)	$7.886	
		Total	$91.219	27,82%
Operational Cost				
	Hardware	Probecards ,etc,etc (depriciated) investments	$60.450	
	Software	License	$5.000	
	Training	Machine/handling/software	$1.000	
	Utillities	Power /cooling	$97.780	
	Maintenance	Repair/tooling/contracts (ex respider probecards)	$7.500	
	Process cost (probe specific)	Total Probecard respider cost	$51.903	
		Total	$223.633	68,20%
Resource allocation	Resources/staf	Operators / Engineers Line/Prod/Test/QA/IT	$11.636	
	Resource cost (probe repair specific)	Probecard maintenance/inspection	$1.413	
		Total	$13.049	3,98%
		Grand Total	$327.900	



Optimization Cost Saving / Cell

Optimizer cost saving opportunities / Cell						
Potential Cost Reduction Parameters						year1
Parameters		Optimization cost saving opportunities		%	% of	Value
			Efficiency improvement			
Investment related	Efficiency improvement	Reduced investments due to increased UPH.	ATE testers and handlers needed for the same capacity, equivalent for depriciation and facilities needed	5,50%	Total testcell CAPEX/year	$5.017
Operational related	Hardware	Reduced Operational cost	Less Loadboard/spiders for the same capicity, including repair/maintenance cost	5,50%	Total specific hw+maintenance	$6.922
		Reduced Operational			Rest of operational	
	Staff cost		recipe		resources (manufacturing)	40		engineering staff	$1.495
		balancing/overhang control	damage (membrane/pyramid types)	2,00%	cost	$1.209
			Process quality improvement			
Quality Process	Potential yield immprovement	Due to better process (probecard) control potential higher yield possible.		0,50%	Real product cost after test	$8.625
			Product quality improvement			
New Opportunities	Business	New products enquiries	New business opportunities due higher capacity and higher outgoeinging quality level.	0,00%	Percentage of total test cell revenue/year	$0
					Grand Total	$35.359

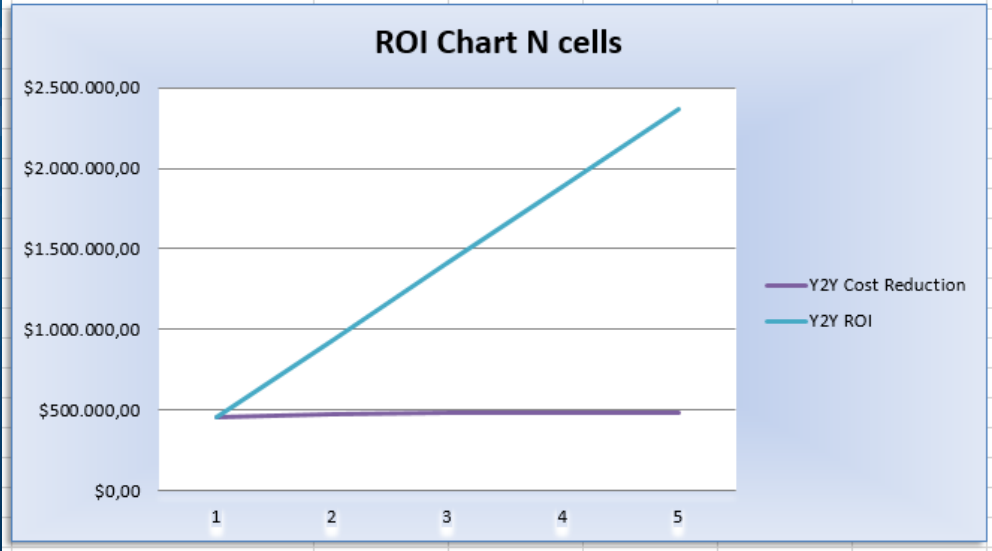




Return Of Investment

- **Based on**
  - 15 wafer sort Cells
  - 5 Products / Cell
  - Saving
    - 5% on Touch downs
    - 0.5% on index
- **Break-even**
  - 3 cells / 1 product
  - Positive within 1 year

Return of investment					
Year	1	2	3	4	5
Total cost of process	$327.900	$327.900	$327.900	$327.900	$327.900
Total cost reduction	$35.359	$36.077	$36.402	$36.458	$36.570
Exensiko-Test PO product cost	$75.280	$67.000	$67.000	$67.000	$67.000
	One Cell operation				
Year to year cost reduction	-$39.921	-$30.923	-$30.598	-$30.542	-$30.430
Cumulative year to year ROI	-$39.921	-$70.844	-$101.442	-$131.984	-$162.414
	Multiple Cell operation				
Year to year cost reduction	$455.104	$474.153	$479.028	$479.870	$481.554
Cumulative year to year ROI	$455.104	$929.257	$1.408.285	$1.888.154	$2.369.708



Conclusion

- Achieve better optimization strategies.
- Savings are in OPEX and less in CAPEX or resources.
- Touchdown reduction between 3% - 10% with outliers above and below.
- Independent of prober software releases.
- Short ROI, depending on number of systems and products, but easily within 1st year.

TI Paper

8:00 AM – 10:00 AM	SESSION 8: Moving from x1 to x123 SOIC Probe Efficiency Improvements
8:00 – 8:30	***Leveraging Multiprobe Probe Card learnings to help Standardize and Improve parametric and WLR Testing*** Brandon Mair (Texas Instruments – Dallas, TX, USA) Presenter: Brandon Mair (Texas Instruments – Dallas, TX, USA)
8:30 – 9:00	***Probe Route Optimization and its effects on the efficiency of test*** Daniel Fresquez and Ms. Rachel Koski (Texas Instruments – Dallas, TX, USA) Presenter: Rachel Koski (Texas Instruments – Dallas, TX, USA)
9:00 – 9:30	***New prober interface docking evaluation*** Daniel Stillman (TI – Dallas, TX, USA) Presenter: Daniel Stillman (TI – Dallas, TX, USA)
9:30 – 10:00	***Review of New, Flexible MEMS Technology to Reduce Cost of Test for Multi-site Wire Bond Applications*** Daniel Stillman (TI – Dallas, TX, USA) Cameron Harker, Tin Nguyen, Doug Shuey, and Frank Meza (FormFactor – Dallas, TX, USA) Presenter: Daniel Stillman (TI – Dallas, TX, USA)

Thank you

- **Users of the tool**
  - For providing actual results.
  - Providing actual use cases.
- **You the audience**
  - For spending this Sunday afternoon.
- **SW Test Workshop**
  - For setting up this 25th conference.