SW Test Workshop

Semiconductor Wafer Test Workshop

Automated Testing of Bare Die-to-Die Stacks

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Presentation Outline

1. Introduction
2. Experimental Set-Up
   - Test Equipment
   - Misalignment Correction Algorithm
   - Test Algorithm
   - Stacked Test Chips
   - Types of Carriers
   - Automatic Re-Align in Action
3. Experimental Results
   - Results on Dicing Tape on Tape Frames for Ø100mm Wafers
   - Results on Sheets of Single-Sided Thermal-Release Tape
   - Results on Double-Sided Thermal-Release Tape of Ø300mm Carrier Wafers
4. Conclusion

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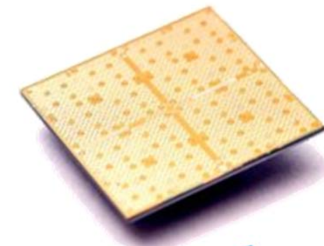
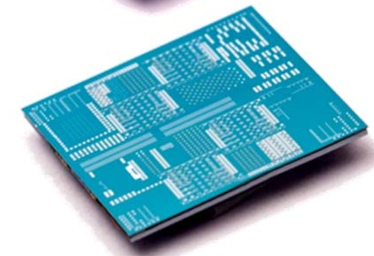
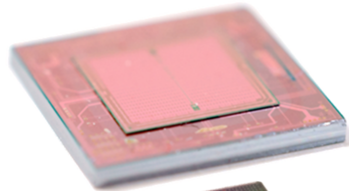
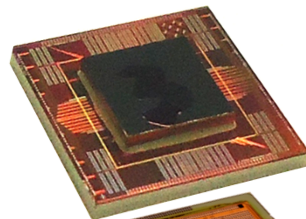
Die-to-Die (D2D) Stacking

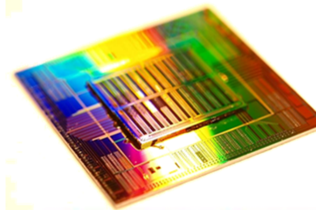
- D2D stacking is an efficient way to generate stacks
  - Allows to
    - Stack dies of different sizes
    - Stack pass-tested dies on pass-tested dies
  - Often utilized for research test chips at IMEC
    - Small and medium quantities
- Transport of D2D stacks in waffle packs

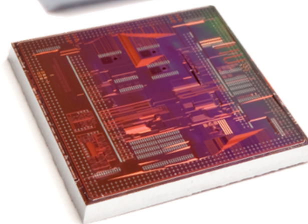


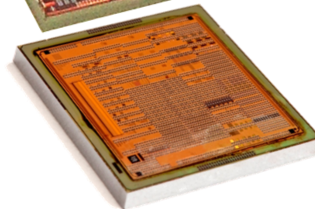


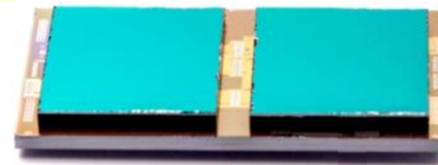












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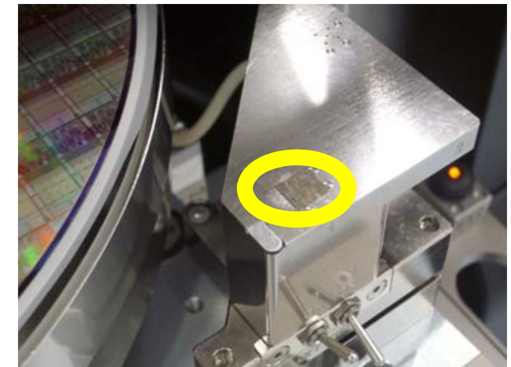
Options for Post-Bond D2D Stack Testing

1. **Per-Stack Placement on Prober**
   - Risk of falling out of waffle pack
   - Risk of loosing stack tracking
   - Manual lifting, placement on chuck
   - Per-stack probe-to-pad alignment
   - Requires engineering presence
   - Bottle-neck in test throughput



2. **Stacks in Bare-Die Tray**
   - Need to hold dies in tray during probing, e.g. through vacuum
     - Custom-made trays with vacuum distribution
       - Expensive, need one per die size
     - Cheaper alternative: drill holes in waffle pack
   - Requires transfer from original waffle pack into tray and vice versa – so far, manual
   - Requires per-stack probe-to-pad alignment

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Concept: Pick-n-Place Array on Carrier Substrate

- Pick-n-place D2D stacks in matrix structure on wafer(-like) carrier substrate
  - **Allows for**
    - Loading a single substrate implies
      loading many D2D stacks in parallel in probe station
    - Automatic index stepping over D2D array by probe station
    - Possible reuse of substrate form factor by OSAT
  - **Requires**
    - Temporary bonding of D2D stacks to carrier substrate
    - Rather accurate pick-n-place (PnP) operation
    - Ability to still correct small PnP mis-alignments on probe station
    - Marking of bad dies: physical (inking) or electronic (wafer map)
- **Substrate Options**
  1. Tape on tape frame
  2. Tape sheets
  3. Carrier wafer

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Test Equipment – CM300 Probe Station

Specification

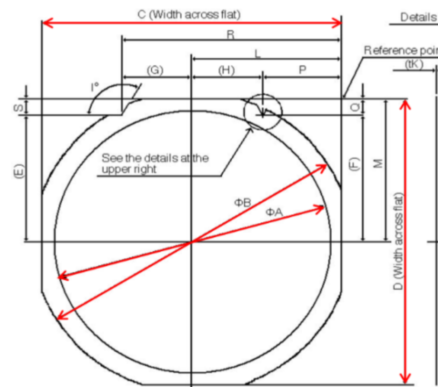
- Cluster configuration
  - Two probers: left/right
  - Shared MHU auto-loader
- Thermo chucks

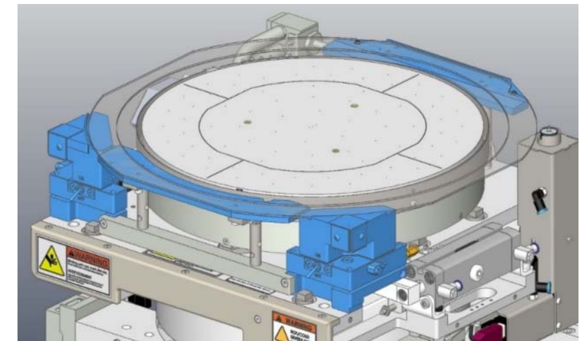
Substrate Loading

- Via auto-loader
  - Ø300mm wafers
- Via front-side load port
  - Wafers up to Ø300mm
  - Tape frames for wafers up to Ø300mm

Location

- IMEC's 300mm fab (in-line)





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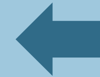
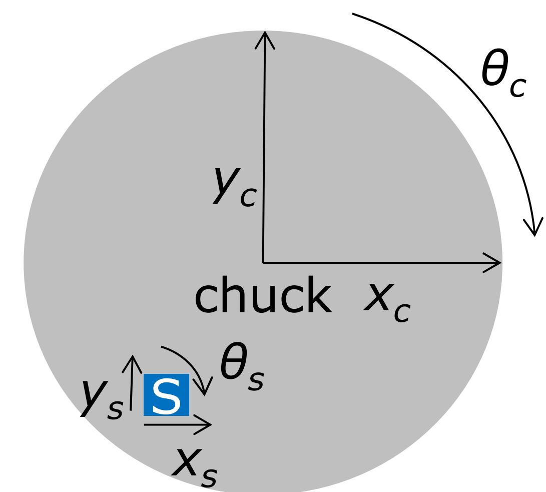
Misalignment Correction Algorithm

Software Functions in Velox

- `ReAlign 2 H` : wafer; x, y, z, and θ;
  after loading new wafer or temperature changes
- `ReAlign 2 C` : n^{th} die; x, y, z;
  accuracy improvement on small pads
- `AlignChip` : single die; x, y, z, and θ;
  for singulated dies and positioners





Correction with AlignChip

- Use with Platen Camera: field-of-view 1.50 mm×1.10 mm
- Correction possible as long as alignment pattern is in FoV
- Constrained capability to resolve rotational misalignments
  - θ_{stack}: rotation around center of die stack (ideally to be applied)
  - θ_{chuck}: rotation around center of chuck (installed mechanism)
- Search area can be enlarged by stepping around
- Can use alternative (back-up) alignment pattern

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Test Algorithm

Algorithm:

Step 1: SetUpProject

<u>for</u> <u>all</u> tape frames **<u>do</u> {**

Step 2: ManualOperation

Step 3: AutomatedOperation

}

Step 1: SetUpProject

```
1: Measure x,y StepNextDie index
2: Training of AlignChip plug-in: pattern recognition and Home setting
3: Training of DetectWaferHeight plug-in
4: Create "wafer" map:
5:    Maximum number of die stacks in x and y (e.g., 7×7)
6:    Input x,y StepNextDie index as measured in Step 1.1
7:    Define coordinate system (e.g. origin (0,0) is SW die stack)
8:    Define probe route (e.g., snake bottom-up)
9: Load probe-card training model (or re-train probe card)
```

Step 2: ManualOperation

```
1: Place tape frame on chuck with center die on center of chuck
2: Indicate in wafer map dies stacks to-be-probed/skipped
3: Move chuck to Platen Camera
4: Move manually to (nearby) dicing street of center bottom die
5: Align2Point for first coarse alignment of tape frame
6: Move manually to Home position on center die stack
```

Step 3: AutomatedOperation

```
1:  Perform AlignChip on center die stack
2:  Perform DetectWaferHeight
    % SynchronPosition is defined (by means of pattern recognition of cross
    % on chuck) and wafer height detection is performed on center die
3:  for all dies stacks do {
4:      StepNextDie % first sub-die (0,0) is base to start AlignChip
5:      Move under Platen Camera
6:      AlignChip
7:      FindFocus: invokes LabVIEW algorithm for calculation ContactHeight
8:      AlignChip % Second time, just to be sure
9:      Move to ProbePosition % Now perfectly aligned
10:     Set Home
11:     Prepare test: datafile headers, light off, init contact counter, etc.
12:     for all sub-dies do {
13:         Contact; measure; Separate; write data to file
14:         StepNextSubdie
15:     }
16: }
```

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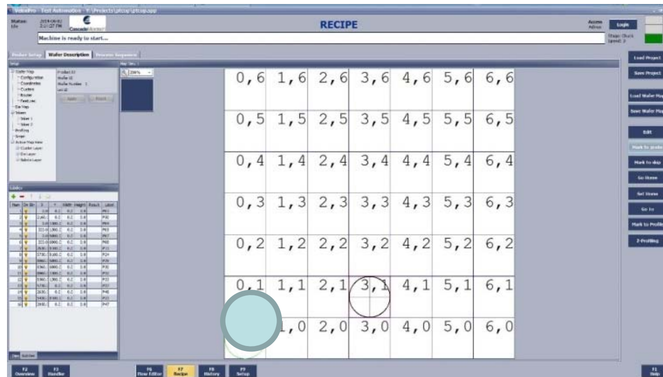
Rectangular “Wafer” Maps with Skip Option

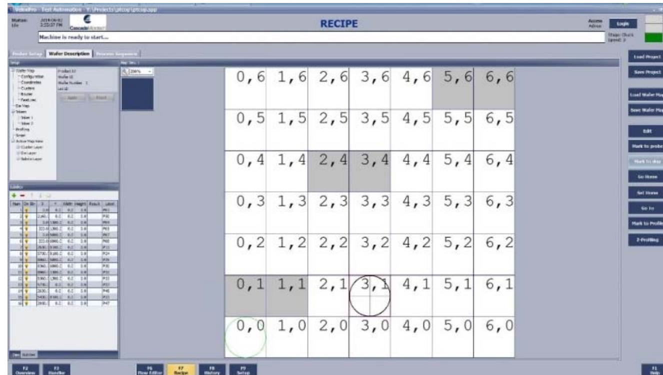


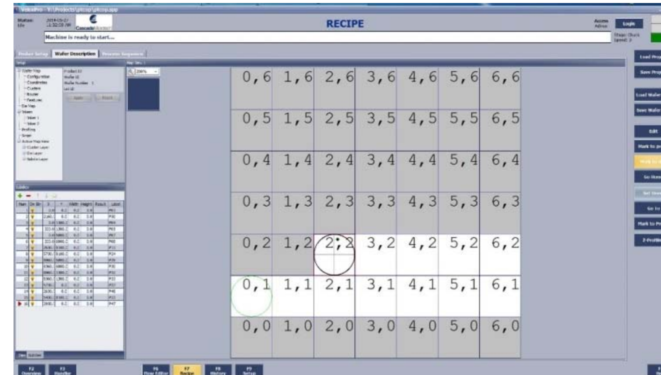
In Step 1 (for all substrates)

- Maximum number of dies stacks in *x* and *y*
- Input *x*,*y* StepNextDie index measured in Step 1.1
- Define coordinate system (e.g., SW stack is origin)
- Define probe route (e.g., snake bottom-up)

In Step 2 (individually for each substrate)

- Indicate in wafer map dies stacks to-be-probed/skipped





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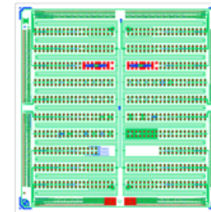
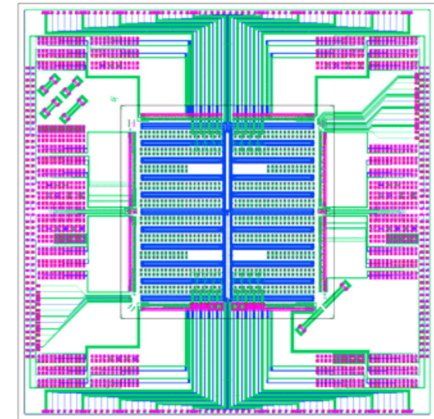
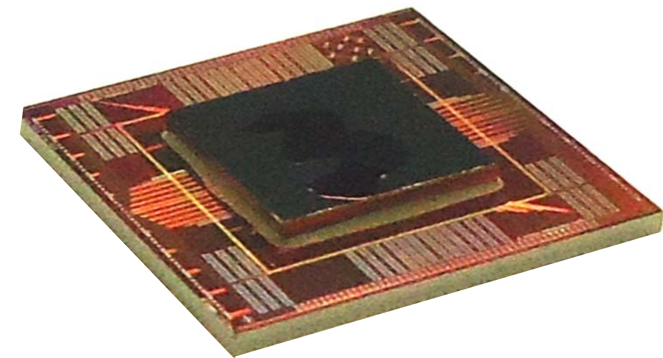
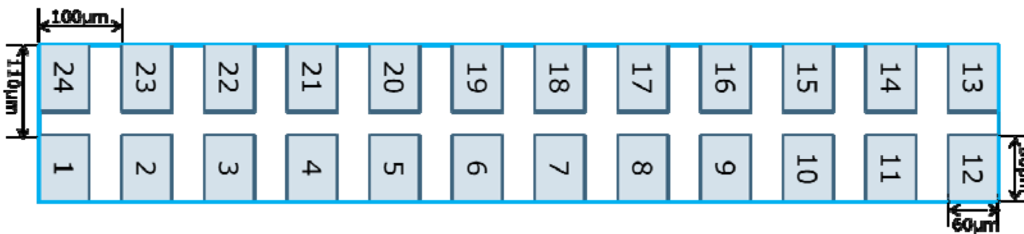
Stacked Test Chips

- Two-die test-chip stacks
  - PTCO: 5.2× 5.2mm^2
  - PTCP: 10.2×10.2mm^2
- Post-bond testing on bare PTCO/P stacks
  - Probing on multiple probe-pad modules
  - All probe-pad modules are located on the front-side (= top-side) of the bottom die
  - Each probe-pad module is IMEC's standard 2×12 module









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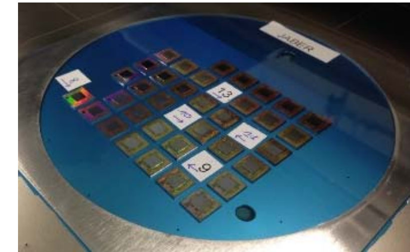
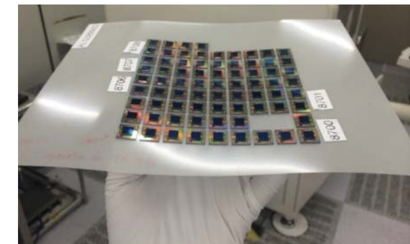
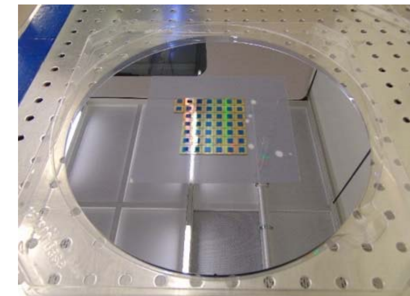
Types of Carriers

1. **Dicing Tape on Tape Frames for Ø100mm Wafers**
   - Blue dicing tape manually laminated on frame
   - PTCO/P D2D stacks in arrays of max. 7×7=49 stacks/frame
   - In total: 372 PTCO/P stacks on 15 frames
2. **Sheets of Single-Sided Thermal-Release Tape**
   - White tape with thick polyester backing layer
   - Can serve as stand-alone carrier
   - PTCO/P D2D stacks in arrays of max. 9×9=81 stacks/sheet
3. **Double-Sided Thermal-Release Tape on Carrier Wafers**
   - Transparent tape affixed to a blank Ø300mm carrier wafer
   - Allows to use the probe station's auto-loader
   - PTCO/P D2D stacks in arrays of 7×7=49 stacks/wafer







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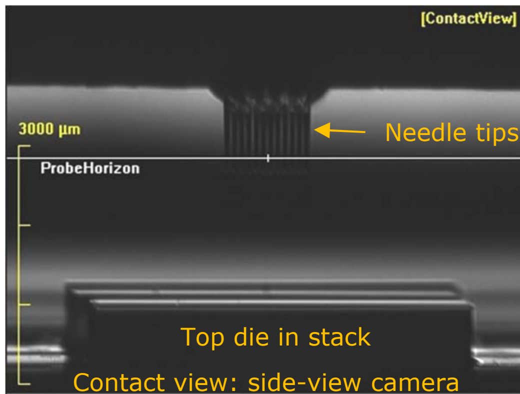
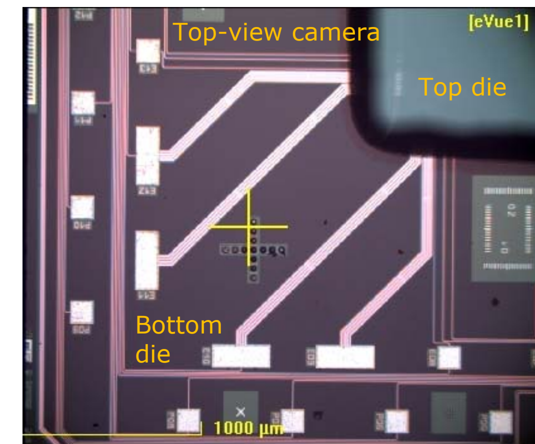
Automatic Re-Align in Action

Extra-long cantilever needles to
↓ compensate for stacked-die height



Validation of correct operation by
↓ checking probe mark locations

Training of alignment pattern
(here: alignment cross on bottom die) ↓



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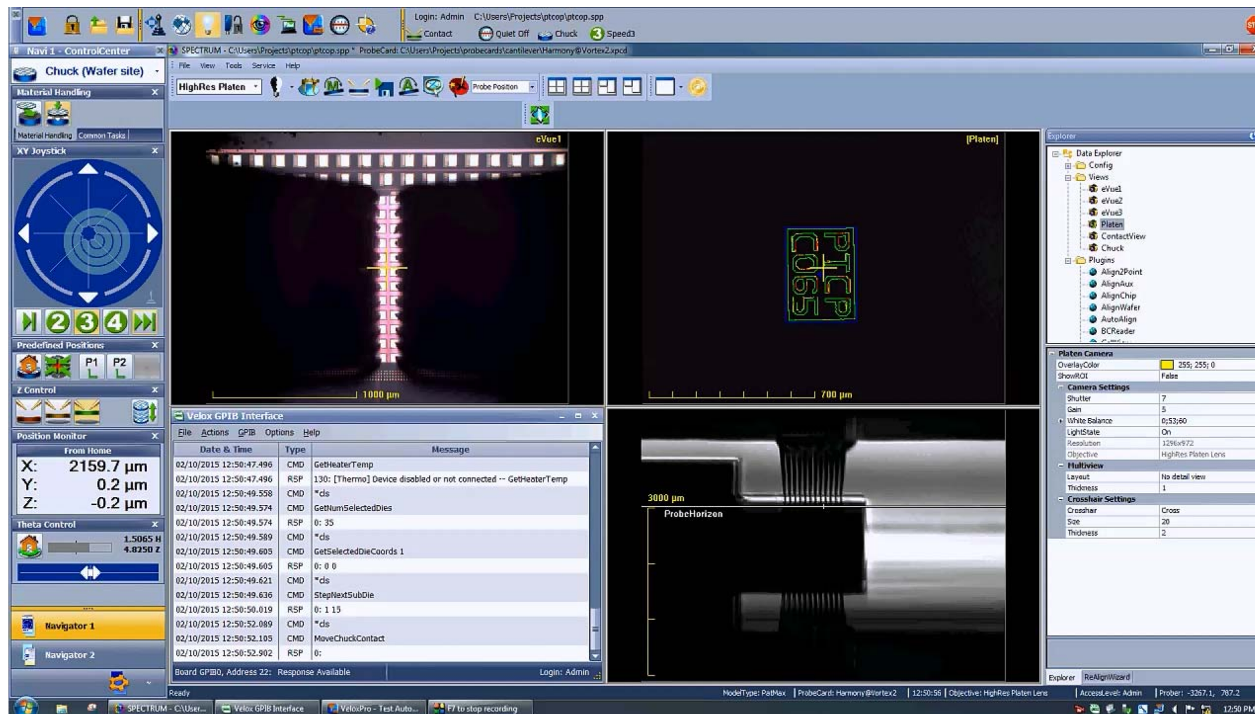
Results on Double-Sided TR Tape – 2/2



Test sequence and video by Bart De Wachter

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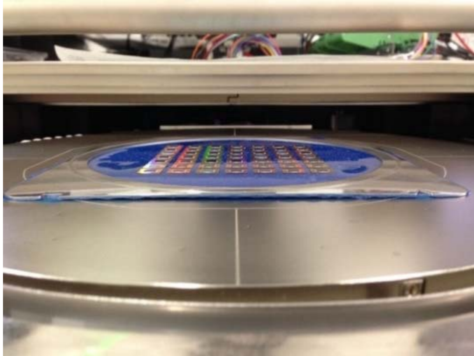
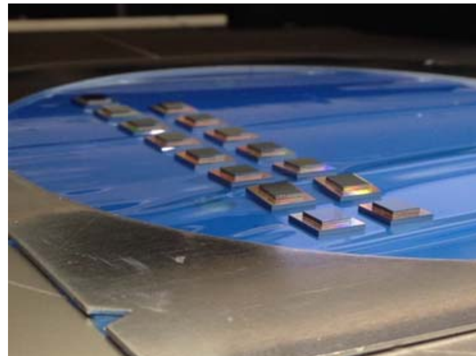
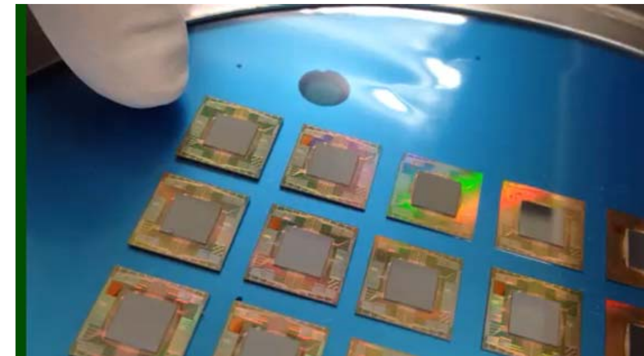
Results on Dicing Tape on Tape Frame – 1/2

- **Tape Frames for Ø100mm Wafers**
  - 100mm used due to pick and place compatability
  - Manual loading via front port chuck pull-out
  - Reused tape frames sometimes bent: difficult for chuck's vacuum
  - Tape wrinkles due to manual lamination; most of them disappeared over time







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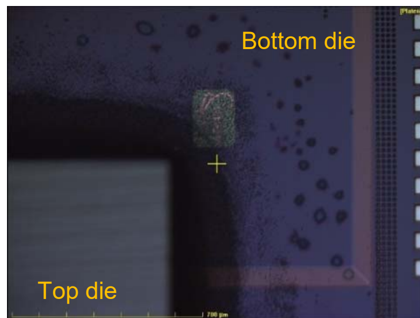
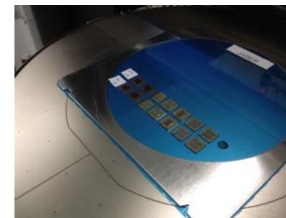
Results on Dicing Tape on Tape Frame – 2/2

- **Re-Align Operation Largely Successful**
  - Performance: ~30 seconds/stack
    - Two AlignChip invocations (Step 3.6 + 3.8)
    - Two alignment patterns per AlignChip
- **Re-Align Issues**
  - Two instances 90° rotated: manual mistake in PnP preparation
  - Two instances with obscured alignment patterns due to underfill fillet/out-bleeding

0,0	1,0
0,-1	1,-1
0,-2	1,-2
0,-3	1,-3
0,-4	1,-4
0,-5	1,-5
0,-6	1,-6

Die Stack	Wafer Map Location	x_c (µm)	y_c (µm)	θ_c (°)
1	(0,0)	-110	59	0.065
2	(1,0)	-203	28	-0.079
3	(1,-1)	-86	113	0.177
4	(0,-1)	1	267	0.198
5	(0,-2)	-37	55	-0.275
6	(1,-2)	-39	55	0.069
7	(1,-3)	-20	91	-0.028
8	(0,-3)	0	0	-0.155
9	(0,-4)	-4	91	0.138
10	(1,-4)	8	51	-0.091
11	(1,-5)	-	-	-
12	(0,-5)	-127	245	0.371
13	(0,-6)	-111	184	-0.079
14	(1,-6)	133	6	-0.388
Minimum		-203	0	-0.388
Maximum		133	267	0.371
Average(abs)		67.6	95.8	0.163
Std.dev(abs)		62.5	82.4	0.112





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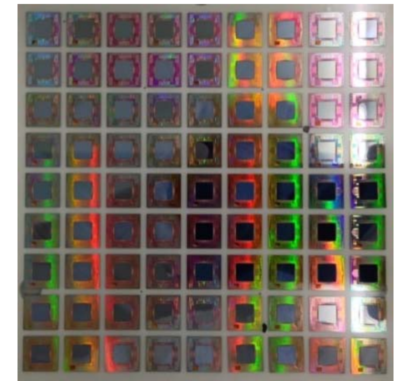
Results on Single-Sided TR Tape – 1/2

- **Sheets of Thermal-Release Tape**
  - Stand-alone tape sheets, no frame necessary
  - No bent frames, no tape wrinkling
  - Better PnP accuracy, narrower 'streets'
  - Manual loading via front port
- **Re-Align Operation Largely Successful**
  - Performance: avg. 13.1 seconds/stack
    - One AlignChip invocation (Step 3.6; skipped Step 3.8)
    - Two alignment patterns
- **Re-Align Learnings**
  - Stacks 6+7: too large θ_{stack}, skipped in wafer map
  - Stack 45: large θ_{stack}, missed alignment for Stacks 46+47

0,8	1,8	2,8	3,8	4,8	5,8	6,8	7,8	8,8
0,7	1,7	2,7	3,7	4,7	5,7	6,7	7,7	8,7
0,6	1,6	2,6	3,6	4,6	5,6	6,6	7,6	8,6
0,5	1,5	2,5	3,5	4,5	5,5	6,5	7,5	8,5
0,4	1,4	2,4	3,4	4,4	5,4	6,4	7,4	8,4
0,3	1,3	2,3	3,3	4,3	5,3	6,3	7,3	8,3
0,2	1,2	2,2	3,2	4,2	5,2	6,2	7,2	8,2
0,1	1,1	2,1	3,1	4,1	5,1	6,1	7,1	8,1
0,0	1,0	2,0	3,0	4,0	5,0	6,0	7,0	8,0



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Results on Single-Sided TR Tape – 2/2

Die Stack	Wafer Map Location	x_c (µm)	y_c (µm)	θ_c (°)	t_{AC} (s)	t_{SND} (s)
1	(0,0)	-6.5	-57.0	-0.083	13.3	0.9
2	(1,0)	-66.0	11.0	0.073	14.0	0.9
3	(2,0)	-15.2	-9.4	-0.070	14.2	1.0
4	(3,0)	-12.4	-11.2	-0.051	12.9	1.0
5	(4,0)	-20.0	8.1	-0.001	13.0	1.5
6	(5,0)	-	-	-	-	-
7	(6,0)	-	-	-	-	-
8	(7,0)	49.9	39.3	0.030	13.0	1.0
9	(8,0)	46.5	49.7	0.045	13.1	0.9
10	(8,1)	29.5	47.2	0.030	12.9	0.9
11	(7,1)	34.1	35.5	0.095	12.8	0.9
12	(6,1)	42.1	25.1	0.035	13.1	0.9
13	(5,1)	47.3	20.3	0.091	13.2	1.0
14	(4,1)	53.4	5.9	-0.002	12.9	0.9
15	(3,1)	57.8	-12.5	0.019	12.9	0.9
16	(2,1)	63.4	-28.5	0.039	12.9	0.8
17	(1,1)	69.9	-40.7	-0.029	13.1	1.0
18	(0,1)	3.7	58.2	0.120	14.2	0.9
19	(0,2)	13.5	49.0	-0.042	12.8	0.9
20	(1,2)	56.3	-42.7	-0.131	14.0	0.9
21	(2,2)	52.1	-27.9	-0.003	13.1	0.9
22	(3,2)	48.0	-15.9	0.041	13.0	1.0
23	(4,2)	38.4	0.7	0.070	13.1	0.9
24	(5,2)	34.5	15.9	0.052	13.1	0.9
25	(6,2)	28.3	25.6	0.012	13.0	0.9
26	(7,2)	46.2	77.7	-0.061	14.3	0.9
27	(8,2)	9.3	31.6	0.071	14.0	0.9
28	(8,3)	-21.9	-36.6	0.080	14.3	0.9
29	(7,3)	5.5	29.2	-0.094	14.1	0.9
30	(6,3)	9.3	18.4	0.029	13.0	0.9
31	(5,3)	15.6	12.7	0.056	13.1	0.9
32	(4,3)	17.0	1.4	0.094	12.9	0.9
33	(3,3)	21.4	-15.0	0.092	13.0	0.9
34	(2,3)	31.2	-22.3	-0.005	13.0	0.9
35	(1,3)	36.3	-37.1	-0.005	13.1	0.8
36	(0,3)	41.5	-44.7	0.077	12.7	1.0
37	(0,4)	29.3	-47.5	0.024	12.8	1.0
38	(1,4)	23.5	-37.5	0.054	13.1	1.0
39	(2,4)	15.5	-27.0	0.029	12.7	1.0
40	(3,4)	11.0	-13.6	0.025	13.0	1.0
41	(4,4)	7.4	-5.8	-0.028	12.7	1.0
42	(5,4)	1.8	6.4	-0.090	13.0	1.0
43	(6,4)	-0.1	24.2	0.080	13.1	1.0
44	(7,4)	-4.9	47.6	0.093	12.7	1.0
45	(8,4)	-105.2	1399.3	-1.771	15.3	1.0
46	(8,5)	-	-	-	47.1	0.8
47	(7,5)	-	-	-	47.2	0.8
48	(6,5)	-22.3	24.9	1.748	20.9	0.9
49	(5,5)	-14.8	8.4	0.004	12.7	0.9
50	(4,5)	-13.4	-17.0	-0.085	12.7	0.9
51	(3,5)	-16.2	-14.6	-0.064	13.9	0.9
52	(2,5)	2.1	-30.6	0.074	14.0	0.9
53	(1,5)	16.1	-33.4	0.066	12.7	0.8
54	(0,5)	14.9	-57.0	0.055	12.7	1.0
55	(0,6)	70.1	65.1	0.137	13.9	0.9
56	(1,6)	63.3	48.9	-0.075	12.7	0.9
57	(2,6)	3.2	-17.6	-0.116	13.9	0.9
58	(3,6)	-0.8	-15.2	-0.040	13.1	1.0
59	(4,6)	-6.2	-5.0	-0.026	13.0	1.0
60	(5,6)	-15.8	-3.0	-0.003	13.1	0.9
61	(6,6)	-20.6	-1.6	-0.055	12.6	0.9
62	(7,6)	-25.6	6.3	-0.002	13.0	0.9
63	(8,6)	-31.4	14.5	0.001	12.7	1.0
64	(8,7)	-36.6	10.5	-0.072	12.7	0.9
65	(7,7)	-32.0	5.9	-0.046	12.7	0.9
66	(6,7)	-28.0	0.5	-0.012	12.7	0.9
67	(5,7)	-23.0	-7.0	0.003	13.0	0.9
68	(4,7)	-16.6	-8.6	0.022	12.7	0.9
69	(3,7)	-8.8	-20.0	-0.005	12.8	0.9
70	(2,7)	-4.0	-22.0	0.065	13.1	0.9
71	(1,7)	2.5	-32.6	0.001	12.9	0.9
72	(0,7)	9.3	-40.6	-0.014	13.0	0.8
73	(0,8)	1.3	-42.2	-0.024	12.8	1.0
74	(1,8)	-6.1	-35.8	0.003	12.7	0.9
75	(2,8)	-11.3	-25.8	0.006	12.9	0.9
76	(3,8)	-15.5	-21.6	-0.029	13.0	0.9
77	(4,8)	-23.8	-17.0	-0.038	13.1	1.0
78	(5,8)	-30.6	-8.1	0.005	13.0	1.0
79	(6,8)	-34.2	-2.1	-0.013	12.7	1.0
80	(7,8)	-40.2	3.1	-0.053	12.7	1.0
81	(8,8)	-50.6	8.5	0.045	12.9	
Minimum		-66.0	-57.0	-0.131	12.6	0.8
Maximum		70.1	77.7	0.137	14.3	1.5
Average(abs)		25.7	24.3	0.047	13.1	0.9
Std.dev(abs)		18.9	17.6	0.035	0.5	0.1

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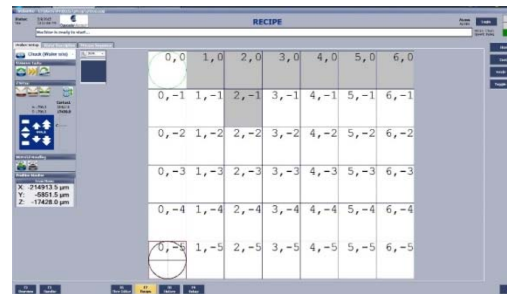
Results on Double-Sided TR Tape – 1/2

- **Thermal-Release Tape on Ø300mm Carrier Wafer**
  - Enable loading with auto-loader

- **Re-Align Operation Successful**
  - Performance: avg. 5.9 seconds/stack
    - One AlignChip invocation
    - One alignment pattern
  - Long compared to StepNextDie (= 0.9 s), but a lot faster than manual alignment!



Die Stack	Wafer Map Location	x_c (µm)	y_c (µm)	θ_c (°)	t_{AC} (s)	t_{SND} (s)
1	(0,0)	-0.2	-0.2	-0.004	5.4	2.1
2	(6,-1)	21.3	47.2	-0.035	5.6	1.1
3	(5,-1)	21.3	61.1	-0.035	5.5	0.8
4	(4,-1)	17.0	70.0	-0.045	5.6	0.9
5	(3,-1)	12.4	74.9	0.013	5.5	1.1
6	(1,-1)	-16.1	66.4	-0.062	6.5	0.9
7	(0,-1)	-19.3	64.2	0.048	5.5	1.0
8	(0,-2)	-10.0	160.1	0.040	5.5	0.9
9	(1,-2)	-5.7	160.0	0.014	5.5	0.9
10	(2,-2)	-8.8	162.7	0.012	5.5	0.8
11	(3,-2)	-4.6	167.2	-0.003	5.5	0.9
12	(4,-2)	2.9	176.2	0.036	5.7	0.9
13	(5,-2)	-1.3	177.0	0.039	5.5	0.9
14	(6,-2)	6.4	180.3	0.019	5.6	0.9
15	(6,-3)	10.4	293.2	0.060	6.7	0.8
16	(5,-3)	8.6	297.2	-0.042	5.4	0.8
17	(4,-3)	8.8	313.8	0.004	5.6	0.9
18	(3,-3)	4.6	312.3	0.022	5.4	0.8
19	(2,-3)	-0.6	310.4	-0.012	5.5	0.9
20	(1,-3)	-3.3	319.2	-0.020	5.6	0.8
21	(0,-3)	-5.5	286.4	-0.045	5.5	0.9
22	(0,-4)	-8.2	330.0	-0.043	5.5	0.9
23	(1,-4)	9.2	293.2	-0.072	6.7	0.9
24	(2,-4)	0.7	302.1	0.062	6.7	0.9
25	(3,-4)	3.2	298.1	0.014	5.5	0.8
26	(4,-4)	3.3	282.9	-0.016	5.4	0.9
27	(5,-4)	28.3	305.2	-0.064	6.7	0.8
28	(6,-4)	-0.3	229.6	0.113	6.8	0.9
29	(6,-5)	18.8	369.5	-0.071	6.8	0.9
30	(5,-5)	11.4	373.8	-0.029	5.5	0.9
31	(4,-5)	8.6	389.0	0.045	5.6	0.9
32	(3,-5)	7.0	387.8	-0.028	5.6	0.8
33	(2,-5)	-2.3	397.4	0.027	5.4	0.9
34	(1,-5)	23.6	386.3	-0.055	12.1	0.8
35	(0,-5)	16.9	378.5	0.002	5.5	
Minimum		-19.3	-0.2	-0.072	5.4	0.8
Maximum		28.3	397.4	0.113	12.1	2.1
Average(abs)		9.5	240.7	0.036	5.9	0.9
Std.dev(abs)		7.3	116.9	0.024	1.2	0.2

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Presentation Outline

1. Introduction
2. Experimental Set-Up
   - Test Equipment
   - Misalignment Correction Algorithm
   - Test Algorithm
   - Stacked Test Chips
   - Types of Carriers
   - Automatic Re-Align in Action
3. Experimental Results
   - Results on Dicing Tape on Tape Frames for Ø100mm Wafers
   - Results on Sheets of Single-Sided Thermal-Release Tape
   - Results on Double-Sided Thermal-Release Tape of Ø300mm Carrier Wafers
4. Conclusion

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Comparison Experimental Results

- **Dicing Tape on Tape Frame**
  Re-align works, but...
  - Bent frames, wrinkled tape
  - Less accurate PnP

	x_c	y_c	Θ_c	t_{AC}*	t_{SND}
Minimum	-203µm	0µm	-0.388°	~30s	~0.9s
Maximum	+133µm	+267µm	+0.371°		
Average(abs)	±68µm	±96µm	±0.163°		
Std.dev(abs)	±62µm	±82µm	±0.112°		

* Two times AlignChip, two patterns each

- **Single-Sided TR Tape**
  Re-align works

	x_c	y_c	Θ_c	t_{AC}*	t_{SND}
Minimum	-66.0µm	-57.0µm	-0.131°	12.6s	0.8s
Maximum	+70.1µm	+77.7µm	+0.137°	14.3s	1.5s
Average(abs)	±25.7µm	±24.3µm	±0.047°	13.1s	0.9s
Std.dev(abs)	±18.9µm	±17.6µm	±0.035°	0.5s	0.1s

* One time AlignChip, two patterns each

- **Double-Sided TR Tape**
  Re-align works
  - Carrier wafer enables auto-loader

	x_c	y_c	Θ_c	t_{AC}*	t_{SND}
Minimum	-19.3µm	-0.2µm	-0.072°	5.4s	0.8s
Maximum	+28.3µm	+397.4µm	+0.113°	12.1s	2.1s
Average(abs)	±9.5µm	±240.7µm	±0.036°	5.9s	0.9s
Std.dev(abs)	±7.3µm	±116.9µm	±0.024°	1.2s	0.2s

* One time AlignChip, one pattern

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Summary

- Demonstrated feasibility of automated index stepping and re-align on arrays of pick-n-placed bare D2D stacks on substrate carriers
  1. Blue dicing tape on tape frames (for Ø100mm wafers)
  2. Sheets of white single-sided thermal-release tape
  3. Sheets of transparent double-sided thermal-release tape on Ø300mm wafers
- AlignChip of CM300's Velox
  - Features: back-up alignment patterns; stepping to increase search area
  - One invocation for one alignment pattern is mostly sufficient
  - Execution time: AlignChip = 5.9s; StepNextDie = 0.9s; test time = XX s
- Upside potential with exceeded θ_{stack}
  - $\theta_{stack} \geq 1.7°$: AlignChip might lose its way, especially out of chuck center
  - Further improvement: AlignChip; Probe; *Undo AlignChip;* StepNextDie
- Significant test throughput improvement for IMEC
  - An option for industrial small/medium-volume production testing

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Thank you for your attention