SW Test Workshop
Semiconductor Wafer Test Workshop

Inter-changeable Pre-bump Probe Solution & Challenges

Author: Yang Qu

Presenter: Wei Liang Sio

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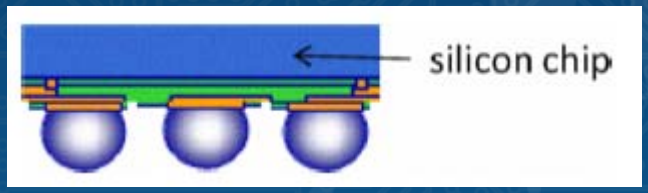
Overview

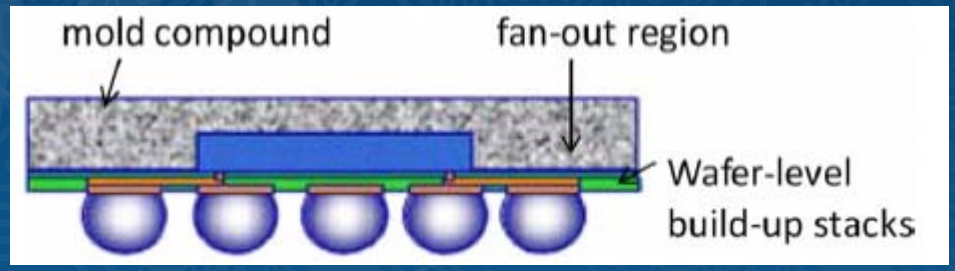
- Background
- Challenges brought by WLP
- Inter-changeable solution
- Experimental data
- Challenges
- Conclusion and further works

WLP Introduction

- **WLP = Wafer Level packaging**
- **Fan-In WLP and Fan-Out WLP**



Fan-In WLP



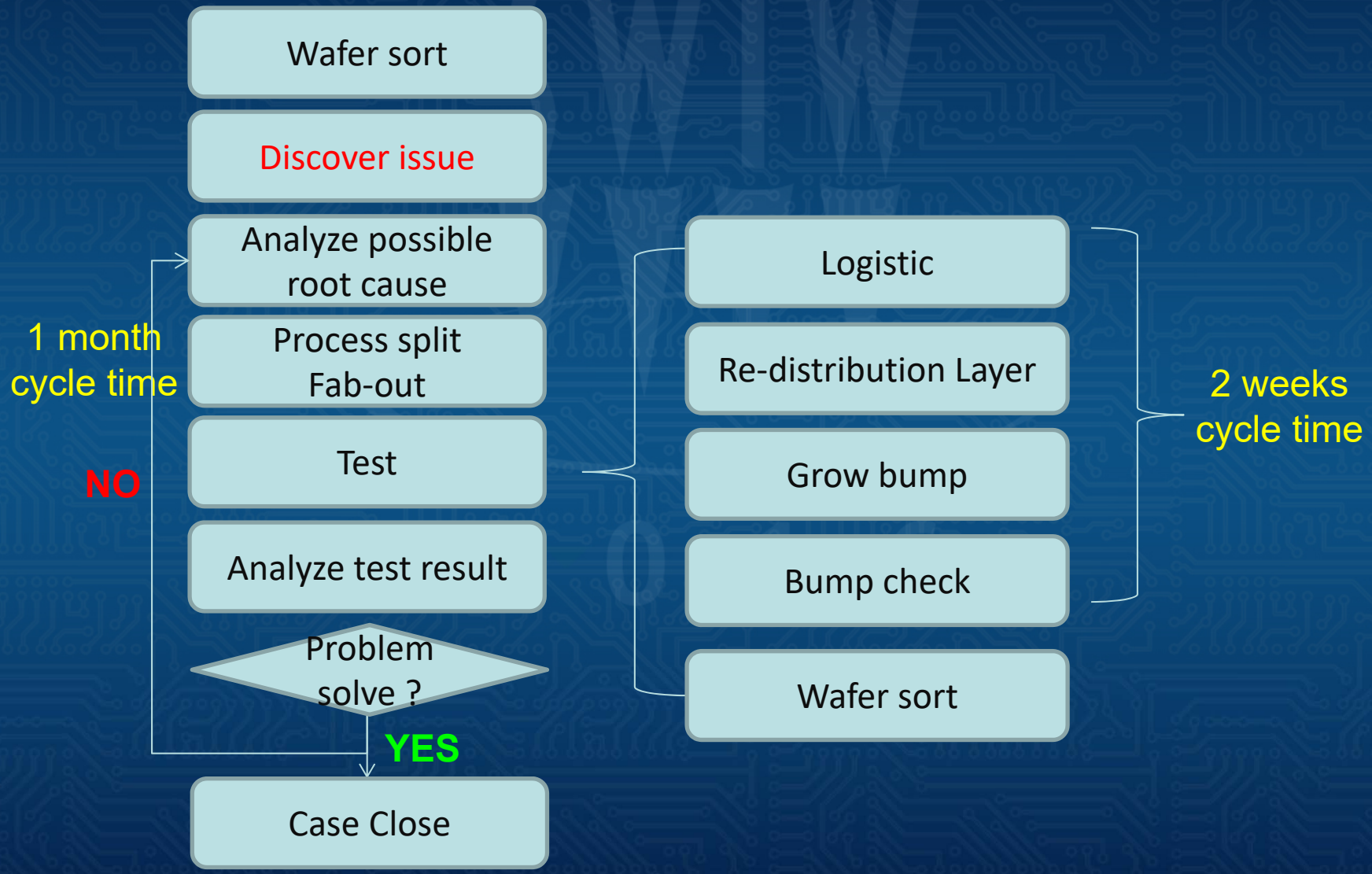
Fan-Out WLP

- **Advantage**
  - Smaller chip size
  - Shorter electrical path
  - Reduced parasitics
  - Lower cost

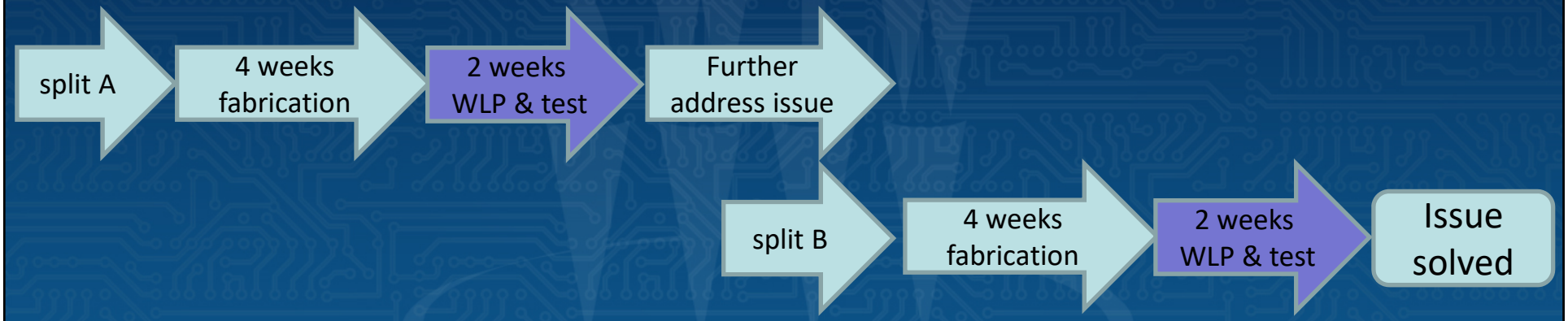
Challenges Brought by WLP

- **Negative impacts**
  - **Prolong process learning cycle**
  - Slow response to line issue
  - Extra cost for engineering debugging

Role of Test in Process Learning Cycle



Role of Test in Process Learning Cycle



To resolve process issues:

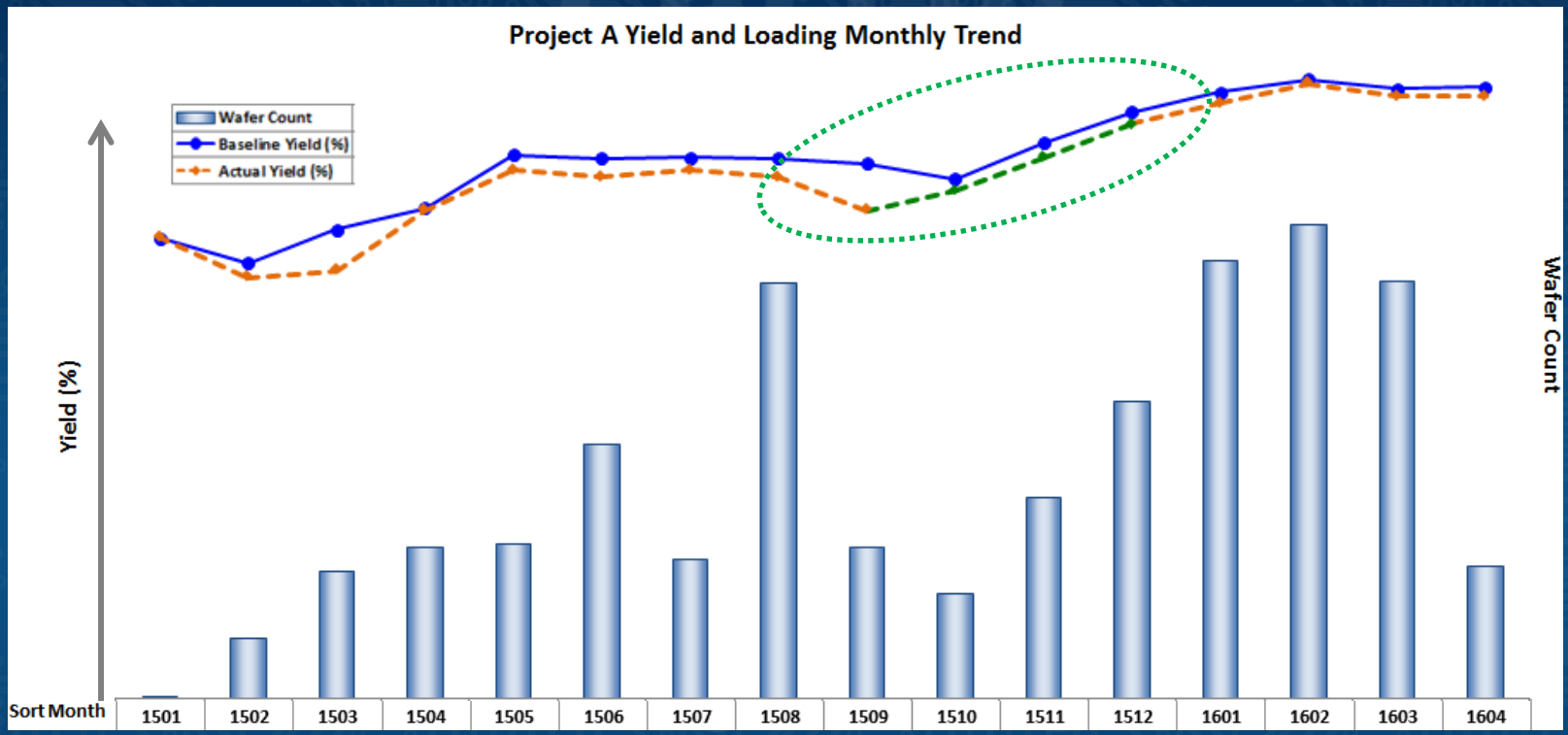
- Multiple learning cycles are required
- Cycle time is impacted by packaging and testing

- **Shorten process learning cycle = faster time to market**

Challenges Brought by WLP

- **Negative impacts**
  - Prolong process learning cycle
  - **Slow response to line issue**
  - Extra cost for engineering debugging

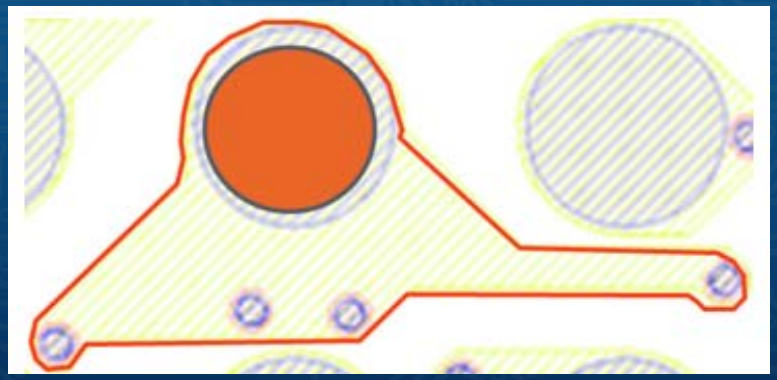
Slow Response to Issue

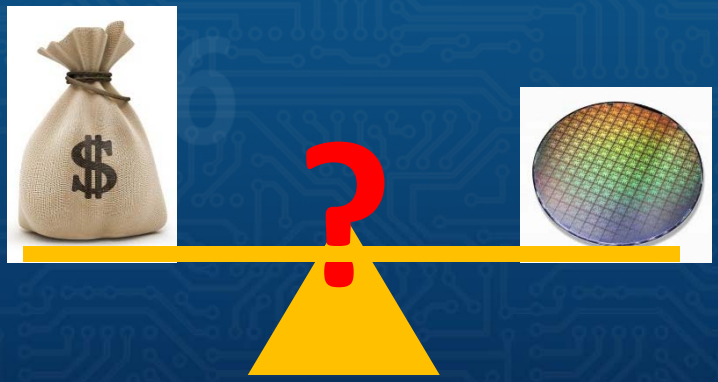


- **Line Excursion**
  - Line excursion: >10% of the monthly loading has been affected.
  - Hit rate 4~10%, yield loss ~5%
- **Shorten response time to line issue = faster yield recovery**

Challenges

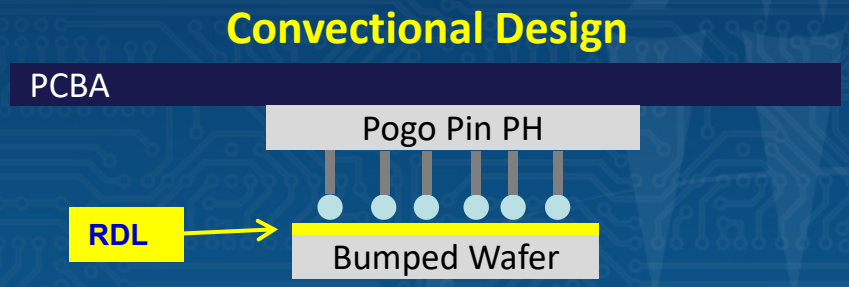
- **Obstacles to perform pre-bump probing**
  - Differences between bumps and pads
  - Extra hardware cost / lead time
  - Additional resources to customize test program
  - Potential damage on underlying structure

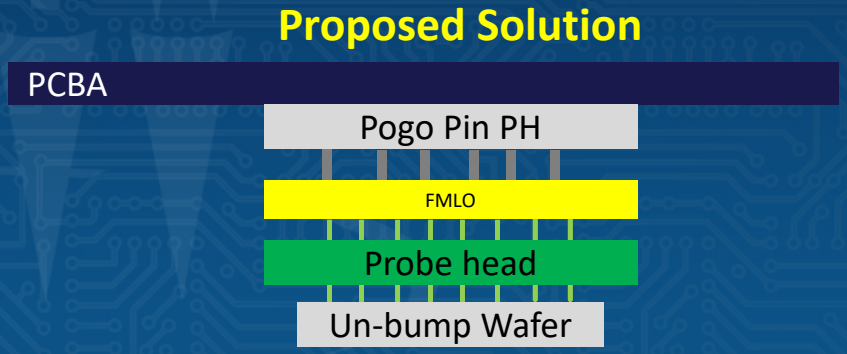


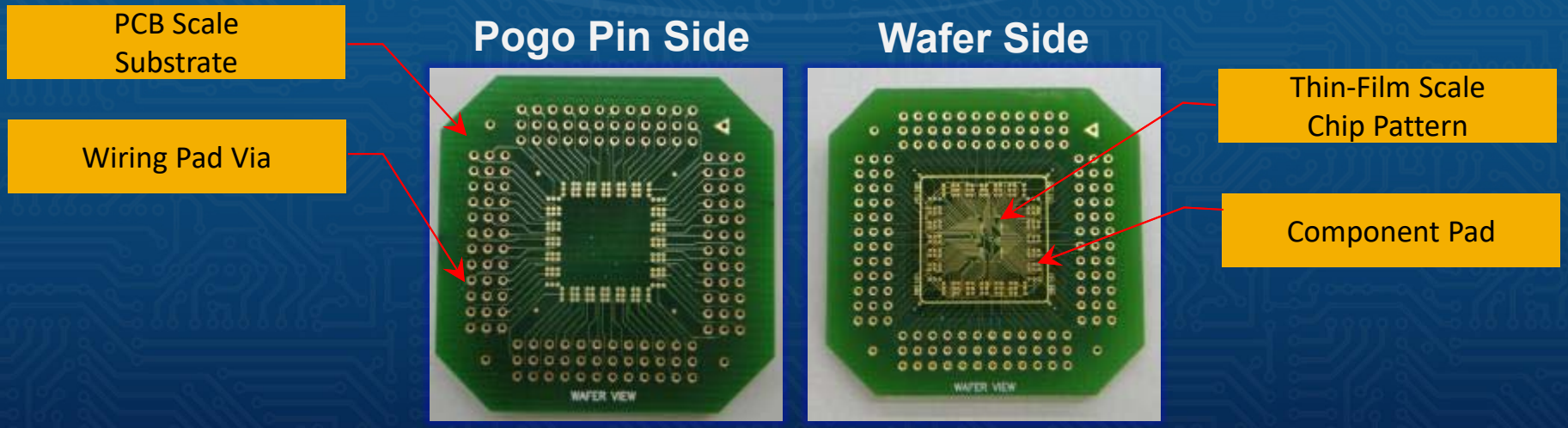


Proposed Solution

Employ customized FLMO to replace RDL, enabling probing of un-bump wafers







Advantages of Proposed Solution

	Inter-changeable Probe head	Customized Pre-bump probe card
Lead-Time	5 weeks	7~8 weeks
Design Change	1 week	7~8 weeks
Cost	FMLO + Pointed PH	100% fresh fabrication

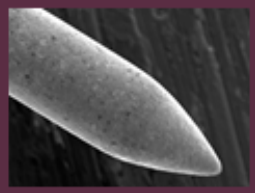
- **Shares same PCB with bump probe card**
- **Uses same test program as production wafer sort**
  - No program modifications needed
  - Full test coverage as production program

Case Study

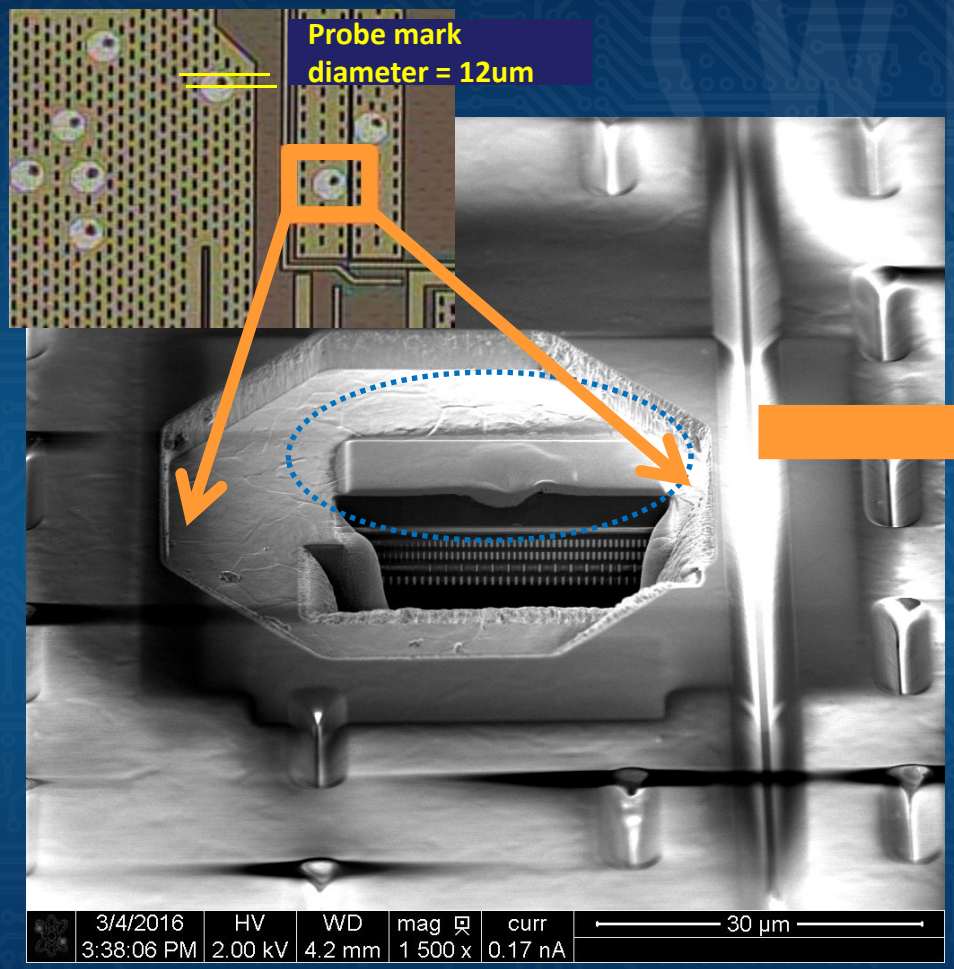
- **Product Specifications**
  - Bumps: 225
  - Al pad: 727
  - Al pad min pitch: 75um
  - Pad size: 50um octagonal
- **Project life cycle**
  - 1.5~2year

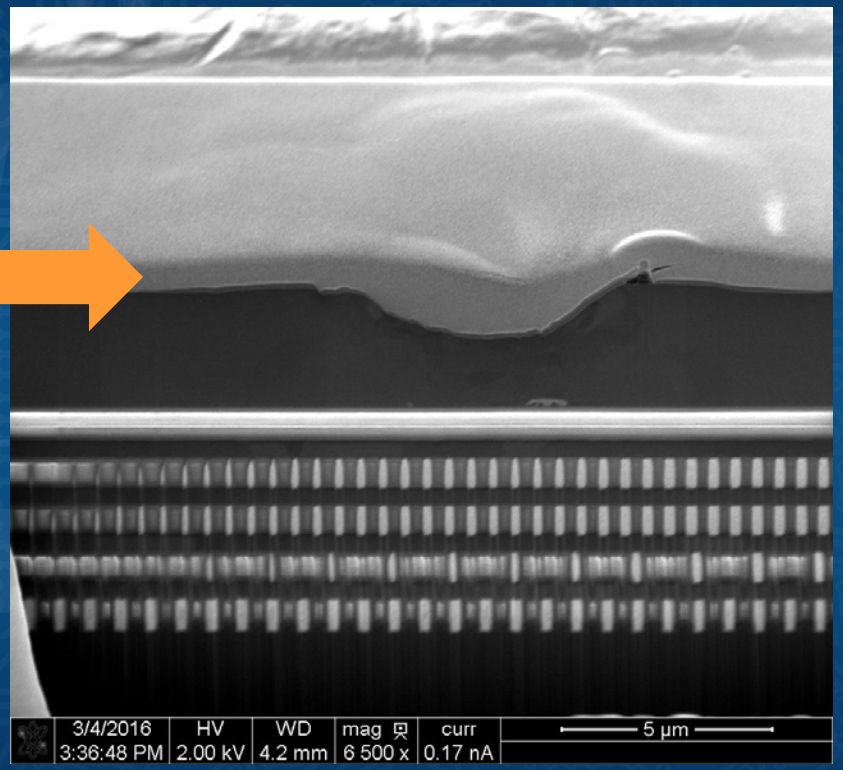
Case Study

- **Needle specification**

Tip Dim. (um)	Flat: ϕ 40um Point: ϕ 8~10um	
Min. Pitch (um)	60	
C.C.C. (mA)	600	350
BCF (gw/mil)	0.5 ~ 0.7	
Max. OD	100 um	
Alignment	±0.4 mil	
Planarity	≦1.6 mil	
Tip shape		

Impact on Underlying Structure

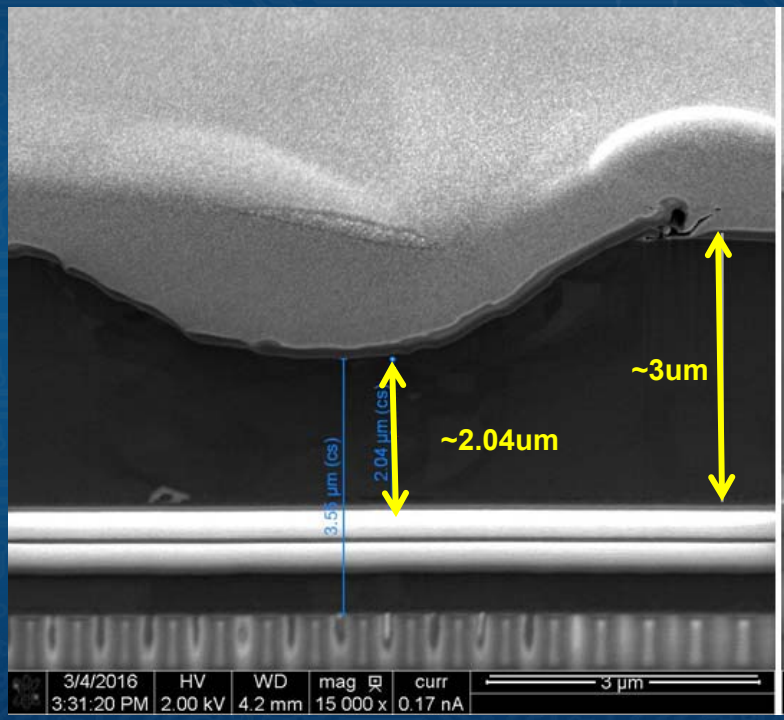




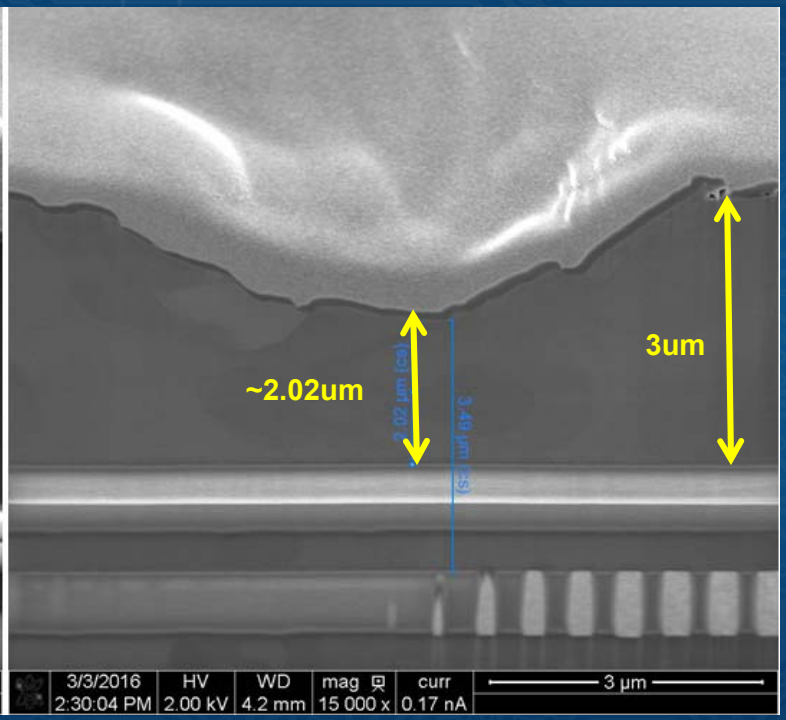
Impact on Underlying Structure

No physical damage is observed on the underlying structure

Single contact



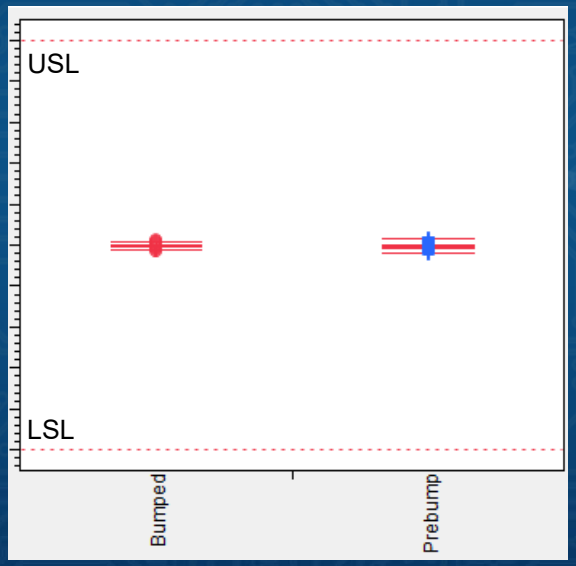
After multiple contacts



Comparison of Results

- Pre-bump wafer vs bumped wafer
- Functional test 100% correlated
- Leakage, IDD off and Bandgap have comparable distribution

Leakage



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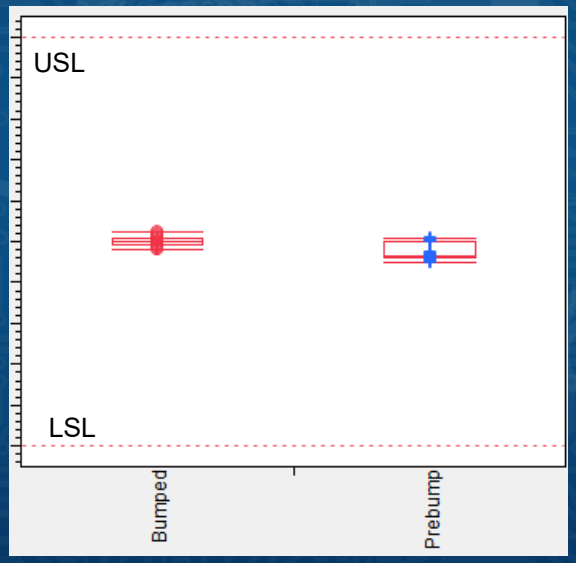
IDD Off



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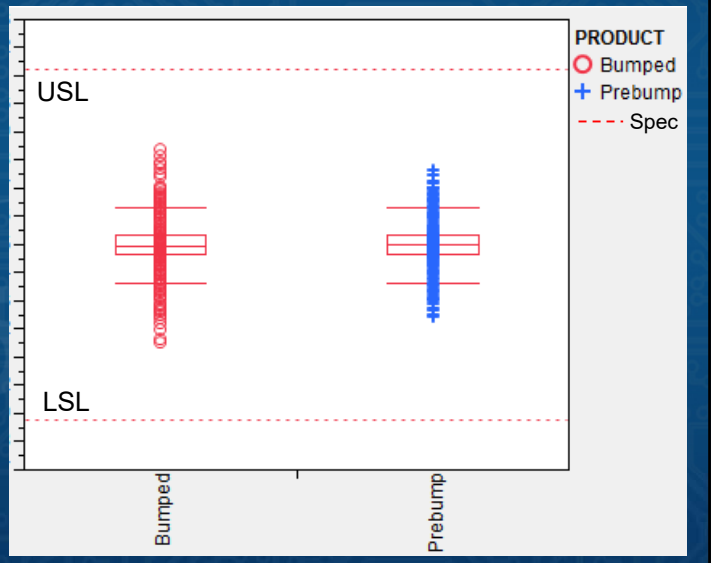
Bandgap



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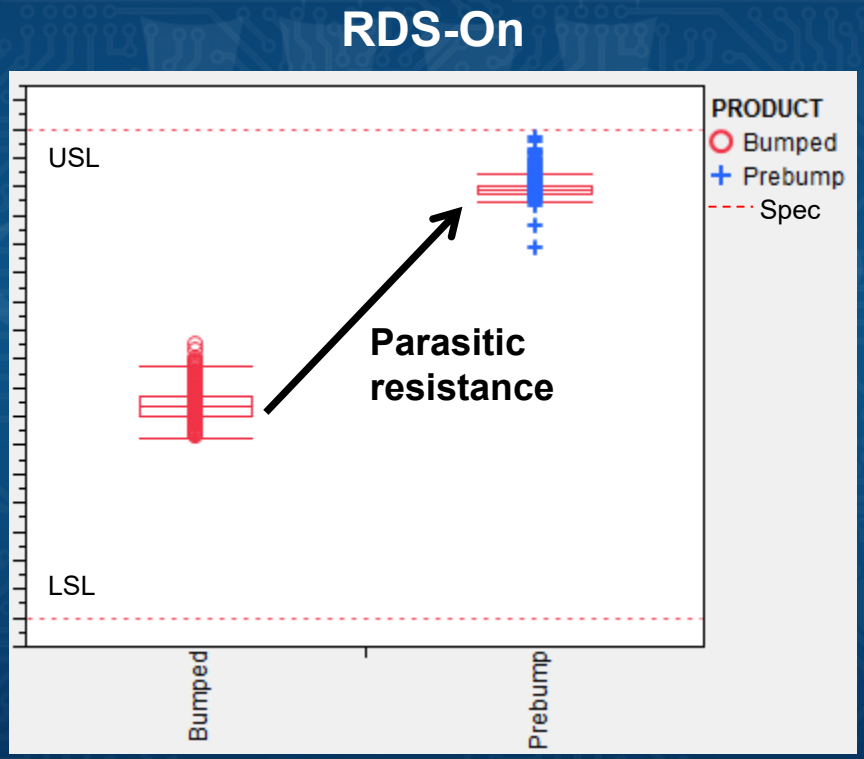
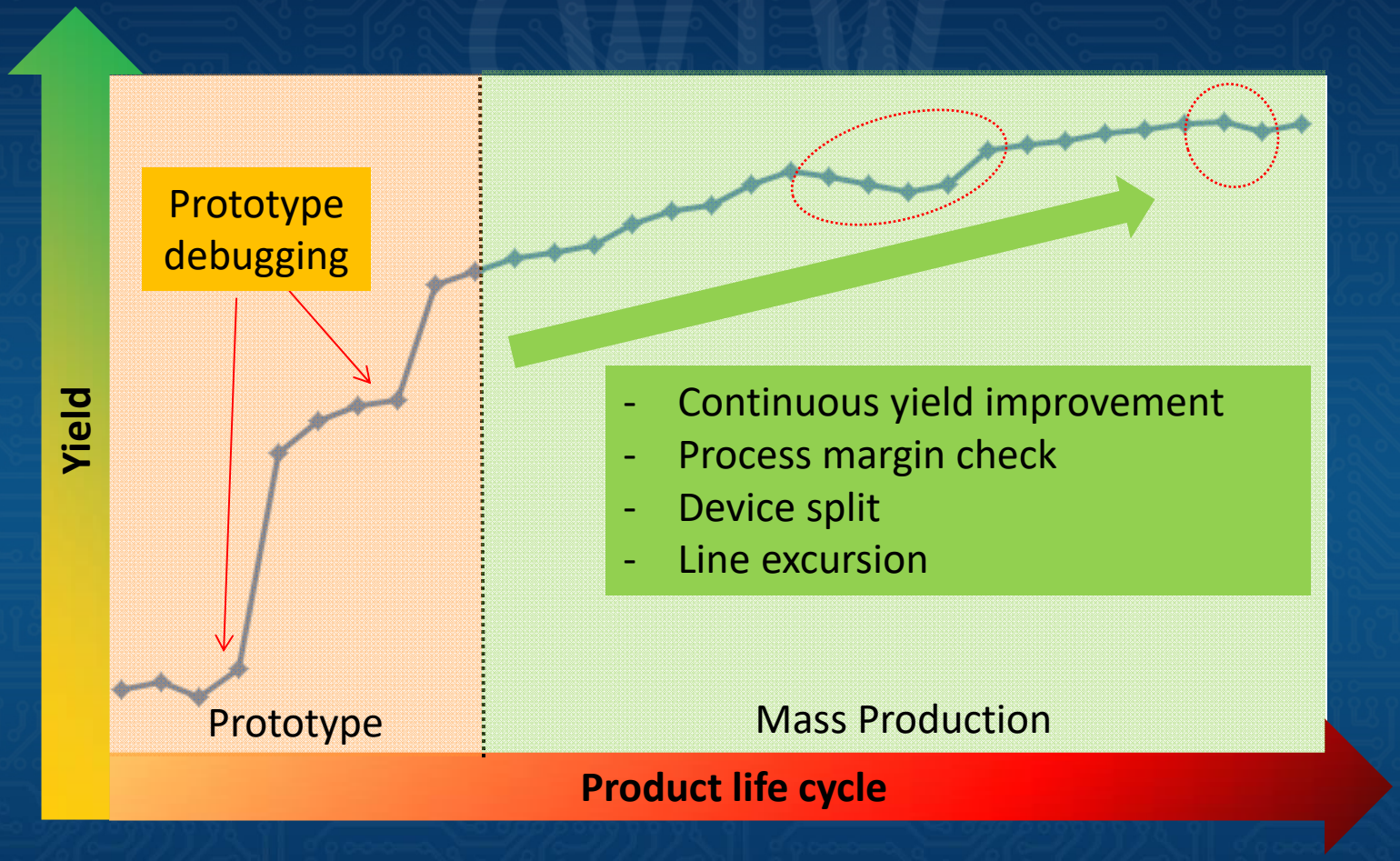
Pre-bump Sorting Challenges

- For example, RDS-on is sensitive to parasitic resistance in the test path.



Benefits



- **Average product life cycle is 2 years**

Conclusion

- Eliminate bump cost for engineering wafers
- Pre-bump testing reduces cycle time and response time to line excursion
- Inter-changeable solution reduce engineering probe hardware costs and lead time
- No physical damage observed on pre-bump pads

Follow-On Work / Q&A

- **Follow-On work**
  - Difference between RDL resistance and FLMO trace resistance could cause resistance mis-match
  - Plan to re-design and fabricate FMLO to match RDL resistance
  - High temperature probe verification

- **Questions ?**

Acknowledgement

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