SW Test Workshop
Semiconductor Wafer Test Workshop

Managing Challenges Associated with Large Area Array C4 Bump/Cu Pillar SOC Applications using Advanced MEMS Technology

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Motivation/Issue

- **As the market appetite for advanced processing power in automotive, mobile, tablet, flat panel, and video game consoles continues to grow:**
  - Complex wafer testing with higher pin counts, large area array, increased parallelism and smaller form factors are required
  - Probe cards requiring 20k, 30k, and > probes resulting in high mechanical force, higher frequency of cleaning, higher probe burn incidence, challenges servicing, and reduced probe lifetime are increasing Cost of Test
- **The market needs a better solution!**

Execution

- In this paper we will discuss the advantages of a new probe style and housing methodology to meet metrics associated with minimizing COO and maximizing ROI as validated through collaboration with a major FAB/Test House.




1st Phase Objective
Identify End User Wish List

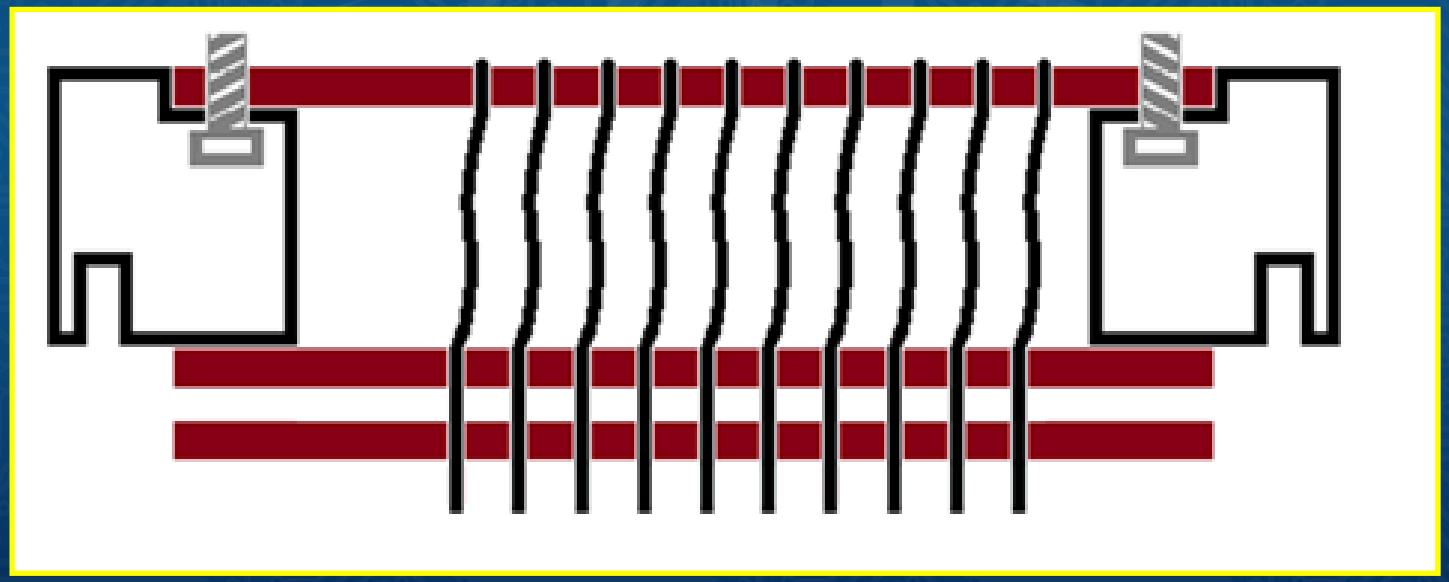
- *Low and consistent Cres performance leading to maximum yields*
- *High current probe material that resists probe burning thereby maximizing tester uptime*
- *Extended probe lifetime to maximize the number of dies tested before probe replacement*
- *Easy and safe repair*
- *Means to Lower Cost of Test*

2nd Phase Objective
Complete Design Meeting Phase 1

- **Must be a MEMS probe**
  - Ability to control shape/spring rate/material composition (high current)
- **Mechanical support to allow easy mfg, assembly, and service**
  - Simple and safe probe replacement
  - Minimal training to perform
- **Extended probe lifetime**
  - Providing means to Lower Cost of Test!

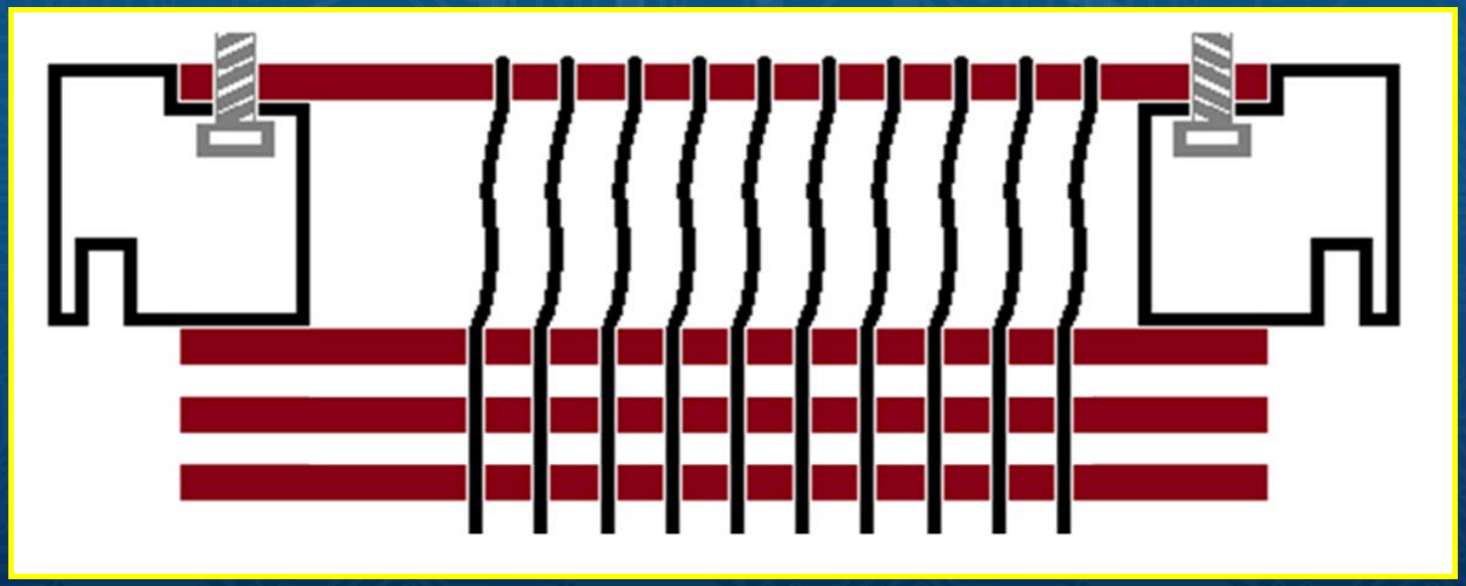
2nd Phase Objective
Complete Design Meeting Phase 1

- Design modeling suggested adding a Patented 2nd LGP to improve probe position and stability lending to placement accuracy and reduced LGP friction



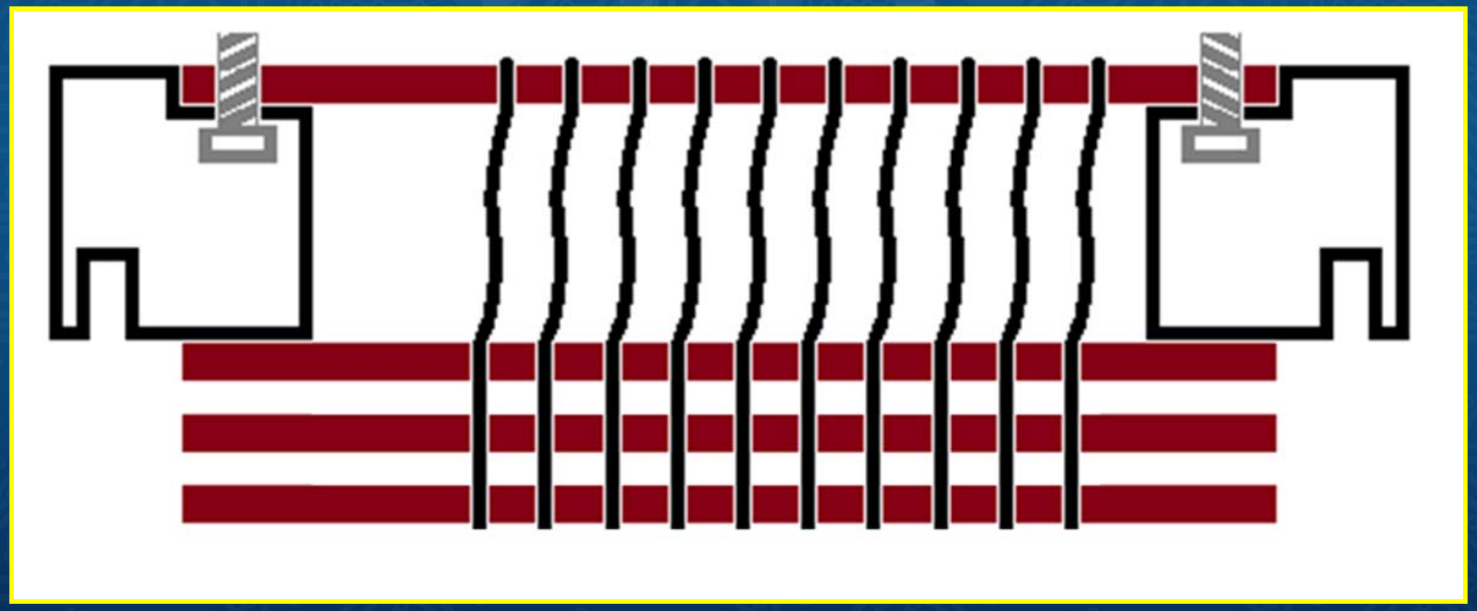
2nd Phase Objective
Complete Design Meeting Phase 1

- Added a Patented sacrificial 3rd LGP increasing total probe length while maintaining identical probe position and stability.



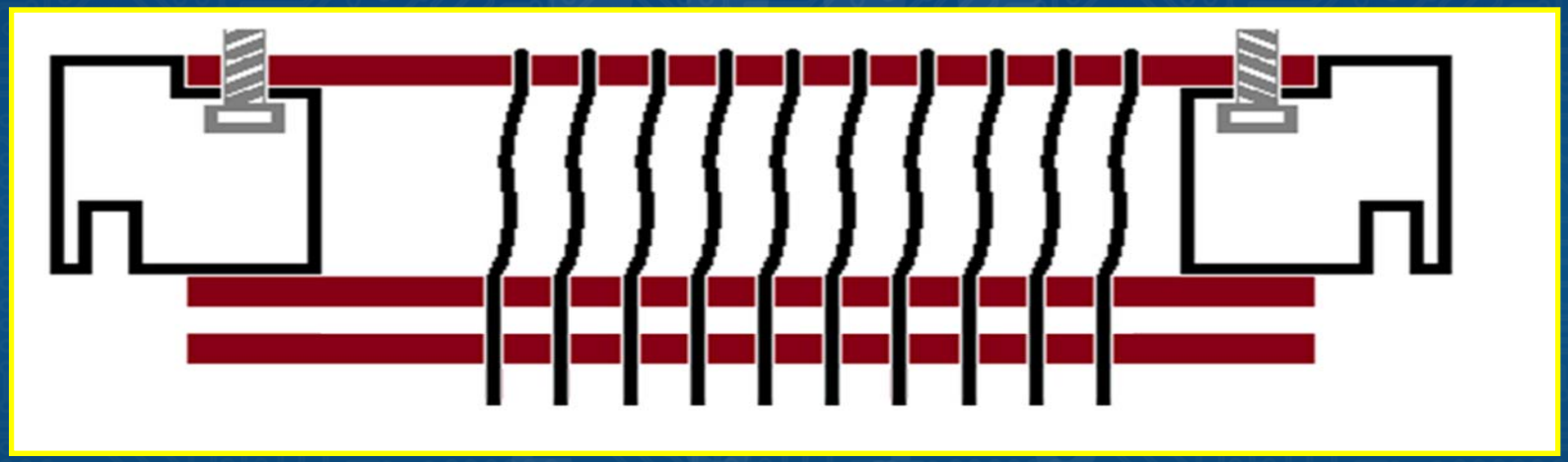
2nd Phase Objective
Complete Design Meeting Phase 1

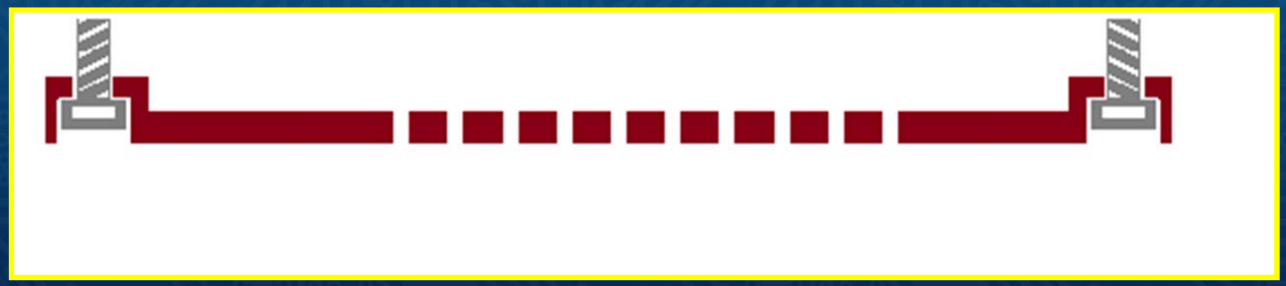
- When probe EOL occurs, simply removing the sacrificial 3rd LGP exposes more probe, thus 2X's lifetime!



2nd Phase Objective
Complete Design Meeting Phase 1

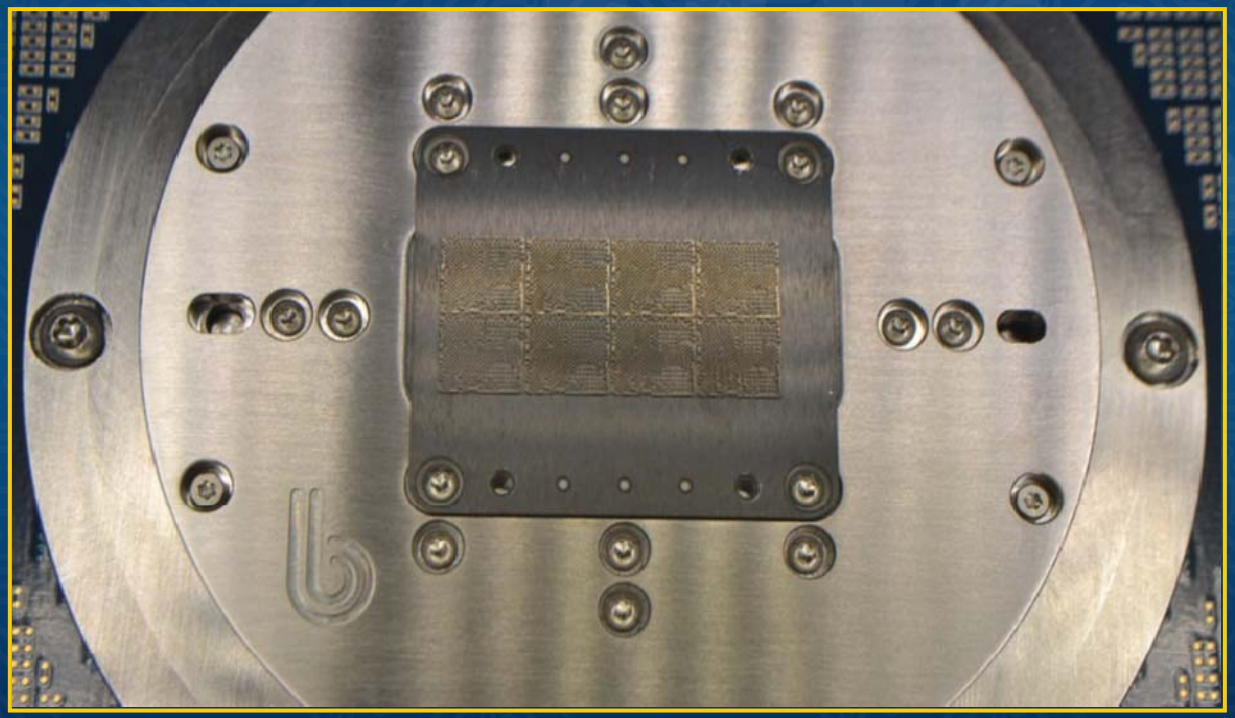
- Patented sacrificial 3rd LGP removed exposing 2X's lifetime!

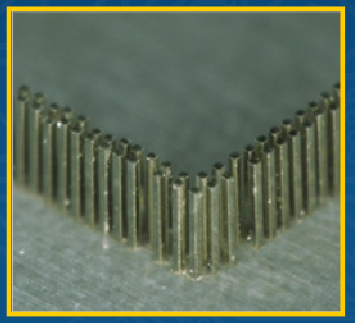




3nd Phase Objective
Manufacture

- **Technology Name - Motus III R**
  - Latin term meaning ‘movement’





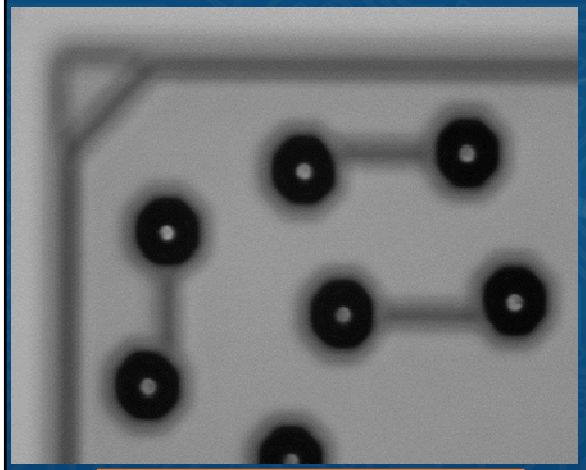
3rd Phase Objective
Manufacture – Motus III R

- **Patented sacrificial 3rd LGP shown in photo**
  - Simple 4 screw end user removal

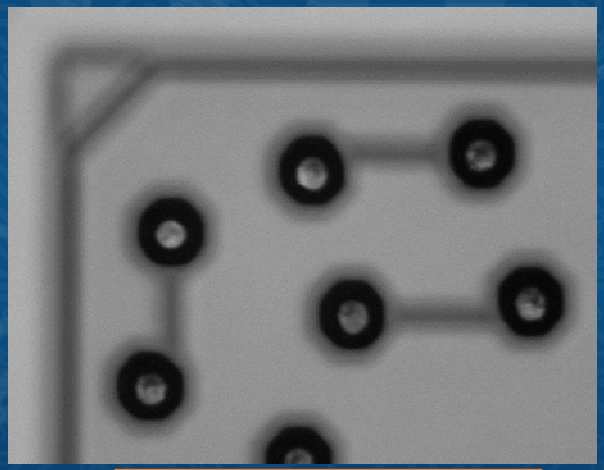
- **Video this slide**

4th Phase Objective
Bump Deformation by 3rd Party – Motus III R

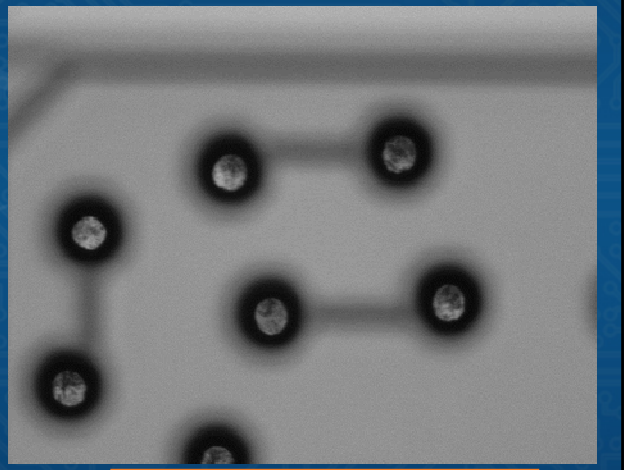
- < 75% bump damage Pb-Free Solder Bump



Probe Marks 5 µm OD



Probe Marks 50 µm OD



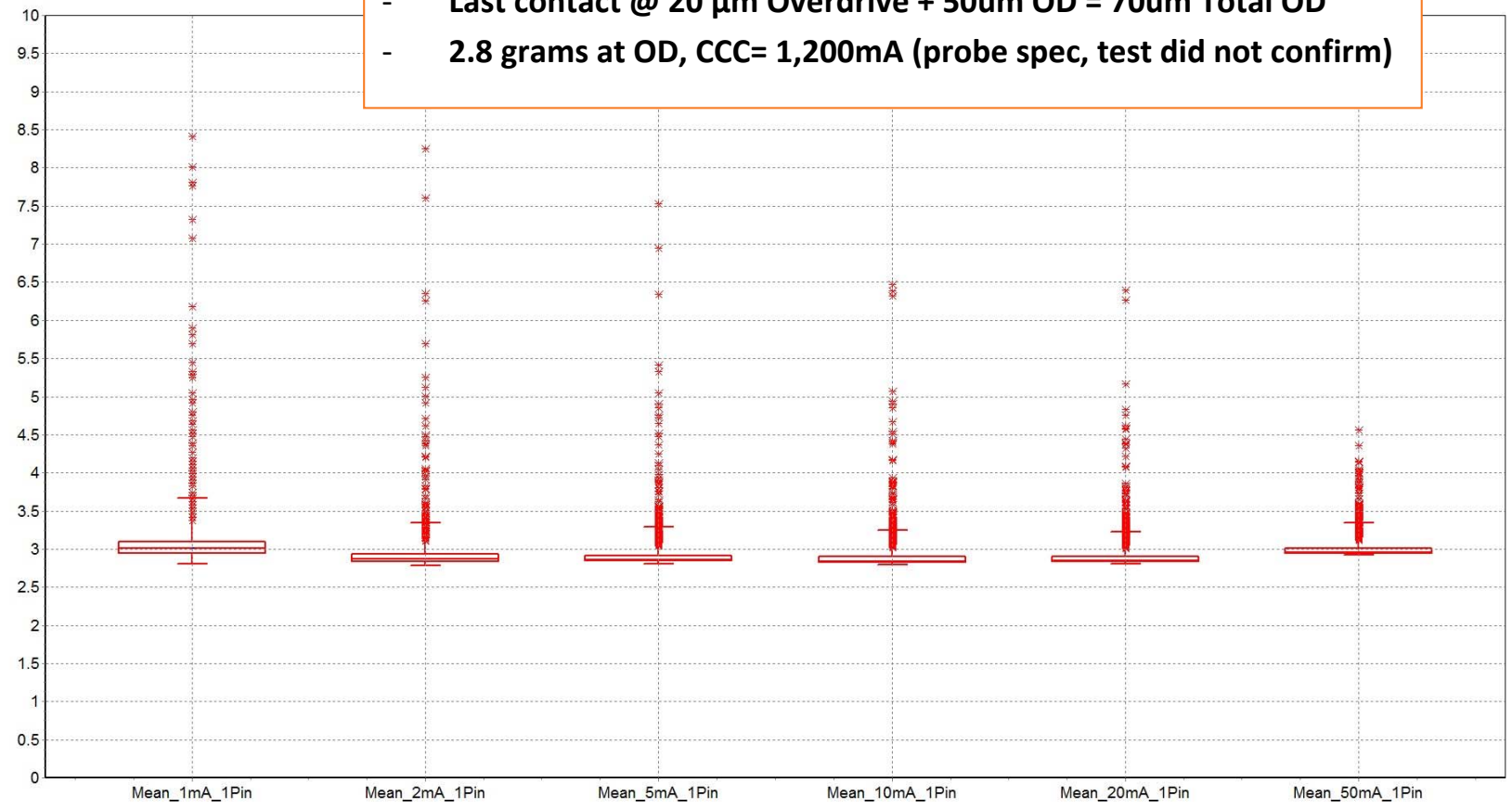
Probe Marks 70 µm OD

4th Phase Objective
Bump Deformation by 3rd Party – Motus III R

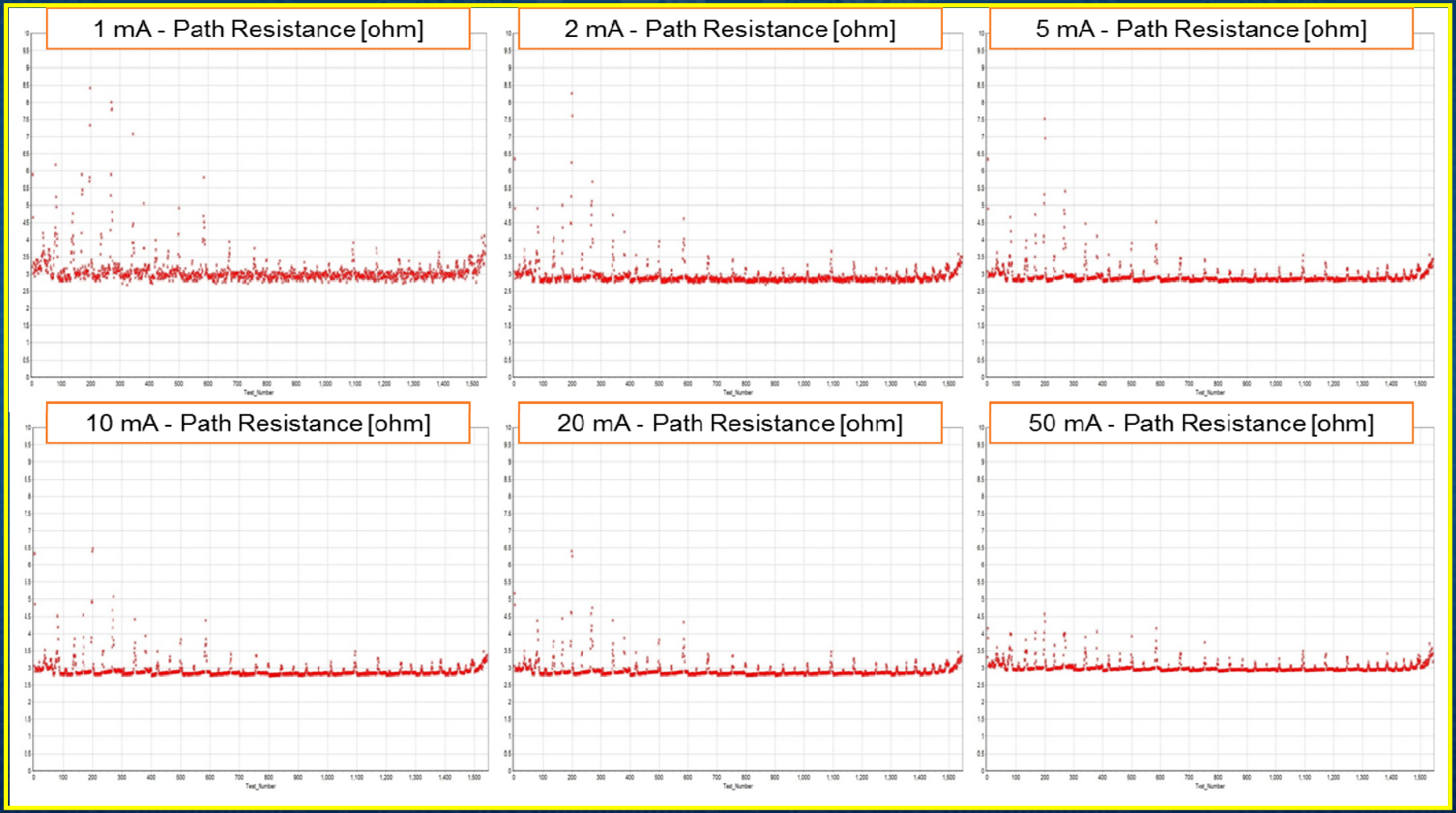
- < 75% bump damage on 40um Cu-Pillar

4th Phase Objective
Cres Testing by 3rd Party – Motus III R

- Last contact @ 20 µm Overdrive + 50um OD = 70um Total OD
- 2.8 grams at OD, CCC= 1,200mA (probe spec, test did not confirm)



4th Phase Objective
Cres Testing by 3rd Party – Motus III R



4th Phase Objective
Cres Testing by 3rd Party – Motus III R

- Cres data test was positive and aligned with a buckling beam Paliney7 Cres, but with much improved probe position, stability and higher lifetime.
- Redesign/manufacturing resulted in changing the Probe-to-ST contact, thereby reducing Cres as witnessed on actual production device. However, insufficient time to re-perform test meeting SWTC deadline.

5th Phase Objective

Easy & Safe Probe Replacement – Motus III R

- Ability for end-user to service PH maximizes uptime and eliminate or reduces need for backup hardware
- Maximum uptime provides Means to Lower Cost of Test

- **Video this slide**

- **Video this slide**

Conclusion

- **Motus III^{R} addresses the market requirement for:**
  - High mechanical performance reliability
  - Consistent Cres supporting high yield
  - Extended lifetime without tradeoffs
  - Higher current probe that resists burning
  - Safe and Easy end user repair
  - Means to Lower Cost of Test

Next Steps

- MAC (maximum allowable current) characterization on Motus IIIs to meet new industry standard testing methodology
- Motus IIIs Alpha test vehicle being delivered June/July to GlobalFoundries with validation target by end of Q3
- Expect Motus IIIs availability in Q4 in limited quantity with high volume availability starting in in Q1 2017
- Need to identify Alpha 60um test vehicle for Lancaster in Q1 2017 as well as 40um

Future Work

	Available Now	*Available Now*	Q3 2016	Q1 2017	Q3 2017
Product/Dev. Code	*Motus II*	*Motus III*	*Motus IIIs*	*Lancaster*	*Piper*
Technology Type	MEMS Offset Probe	MEMS Offset Probe	MEMS Offset Probe	Advanced Vertical TBA	Advanced Vertical TBA
SOC Application	Al Pad	Micro Bump - CuP	Micro Bump - CuP	Micro Bump - CuP	Micro Bump - CuP
Market	1st Gen TSV	SOC	SOC	SOC	SOC
Pitch ums	140um +	100/110	80-90	60-70	40-50

Recognitions

- Jens Kober - GlobalFoundries, Dresden
- Alexander Wittig – GlobalFoundries, Dresden
- Thomas Auxel – GlobalFoundries, Dresden