SW Test Workshop
Semiconductor Wafer Test Workshop

Interlayer Dielectric (ILD) Cracking Mechanisms and their Effects on Probe Processes

Daniel Stillman, Daniel Fresquez

Texas Instruments Inc.

June 5-8, 2016

Outline

- **Probe Optimization – Why is it needed?**
- **Objective and obstacles**
- **Thermal Challenges**
  - Interface movement
  - Affects on Z and pre-set OT
- **Implementing an automated solution**
- **Improvements in Silicon Design**
- **Acknowledgments**

Speed Optimization – Why is it needed?

- **Improve quality for our customers**
  - Extreme temperatures, multiple insertions, and automotive quality requirements make card technology selection critical for the end product.
- **Provide a means for PC design**
  - Complex probe card designs (matrix, skip row / skip column, diagonal) call for more upfront design work to insure optimal efficiency.
- **Provide robust design rules for future technology nodes**
  - How do we design for probe?

Objective

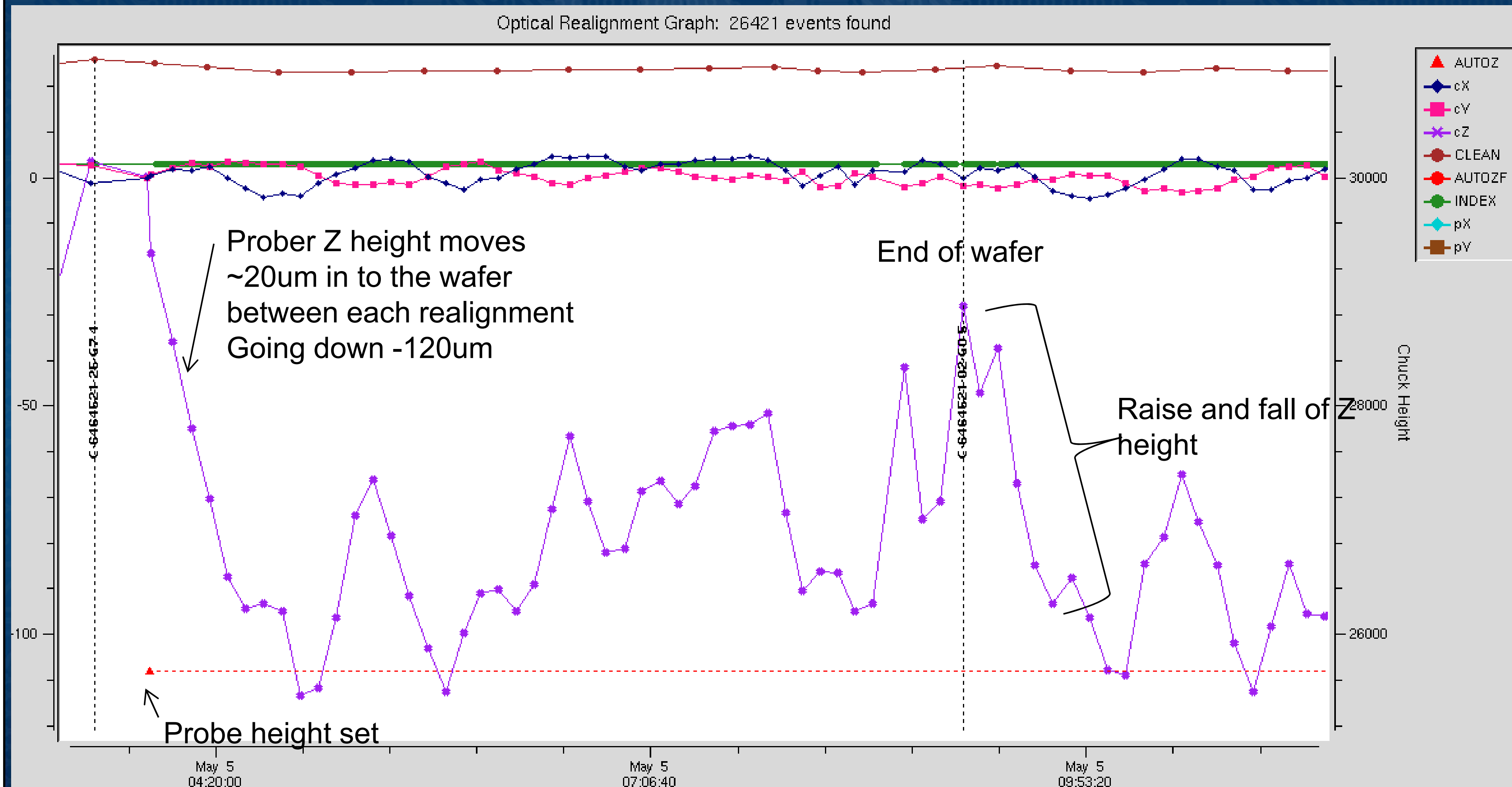
- Challenge: Changes in metal design can results in cracks in barrier metals and insulation layers. These cracks can results in metal migration and functional failures
- Obstacles: Slowing down Z-speed reduces force induced by probe card technology on IC devices, thus preventing di-electric crack fail modes.

Thermal Challenges

Thermal movement During probing

- Thermal movement during probing can result in unexpected added probing over travel
- Contact related issues
- Crashed probe cards

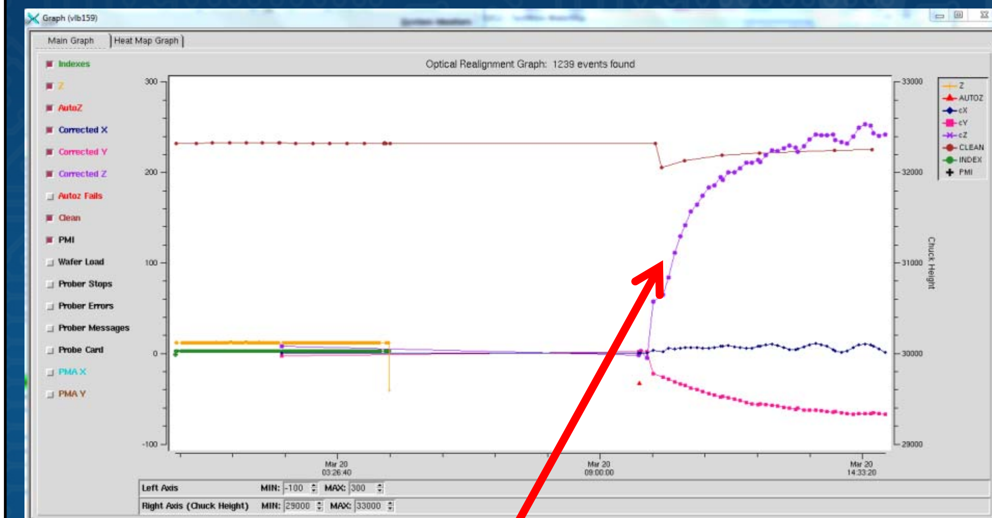
Thermal Movement

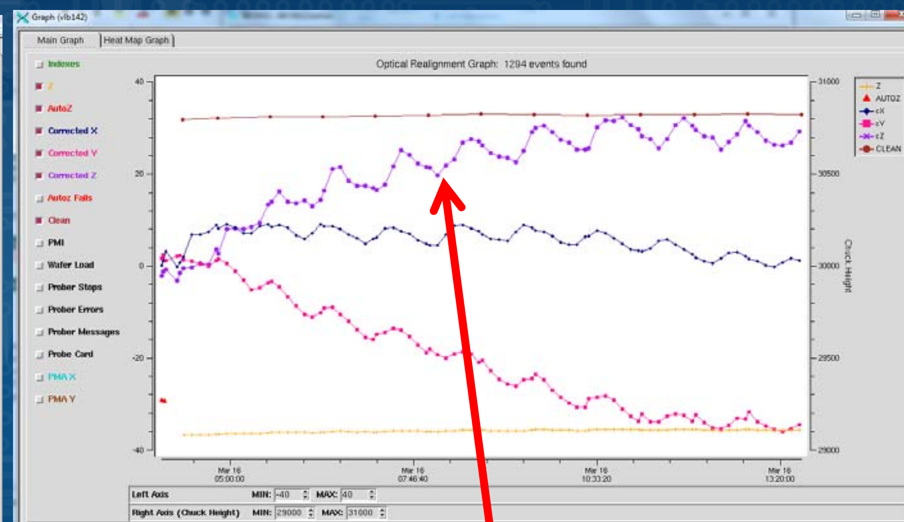


High Temp Evaluations

Problem

Same probe card showed different thermal curves on two different testers



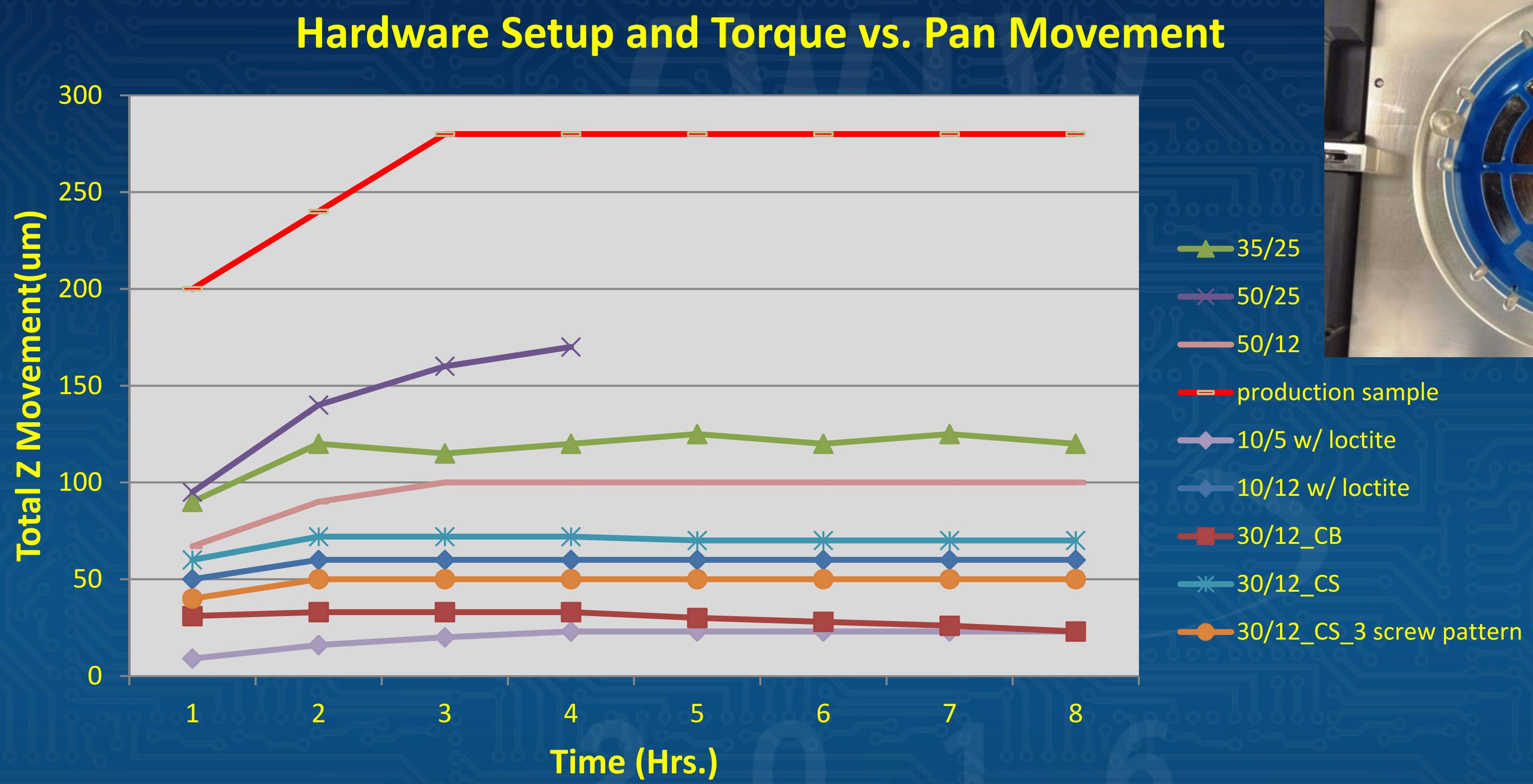


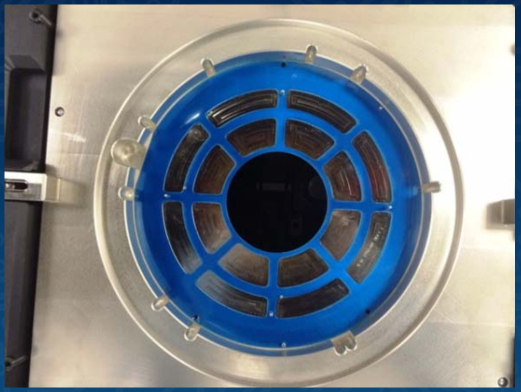
140um Z movement

40um Z movement

Found the probe card pan hardware was causing changes in thermal movement

Hardware Setup Comparisons



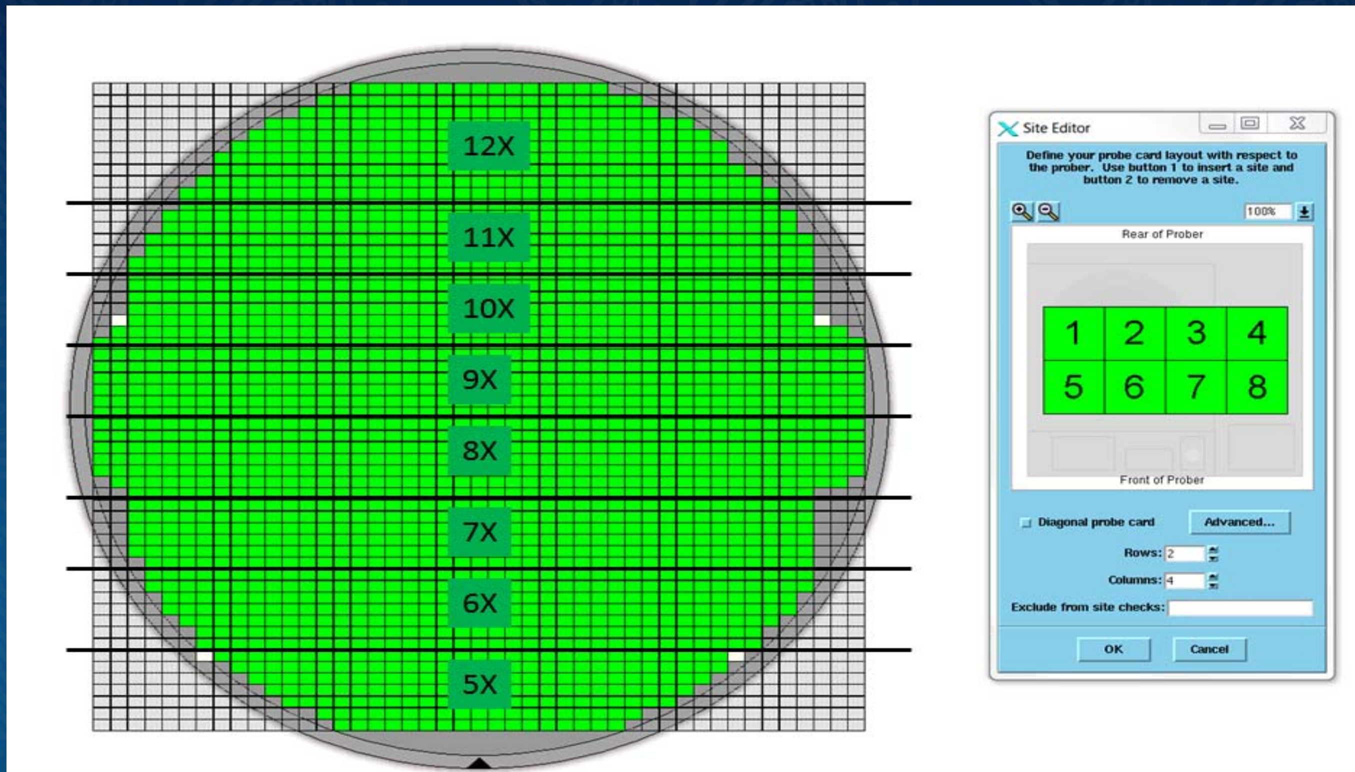


SS and Invar Head Stage Interactions and Optimal Setup Combinations:

- 5 Screws 10 in/lbs torque with Loctite = 25um movement
- 5 Screws, 50 in/lbs torque = 40um – 50um
- 12 screws, 30 in/lbs torque = 50um movement

Top performance with all 25 screws and production acceptable= 100um

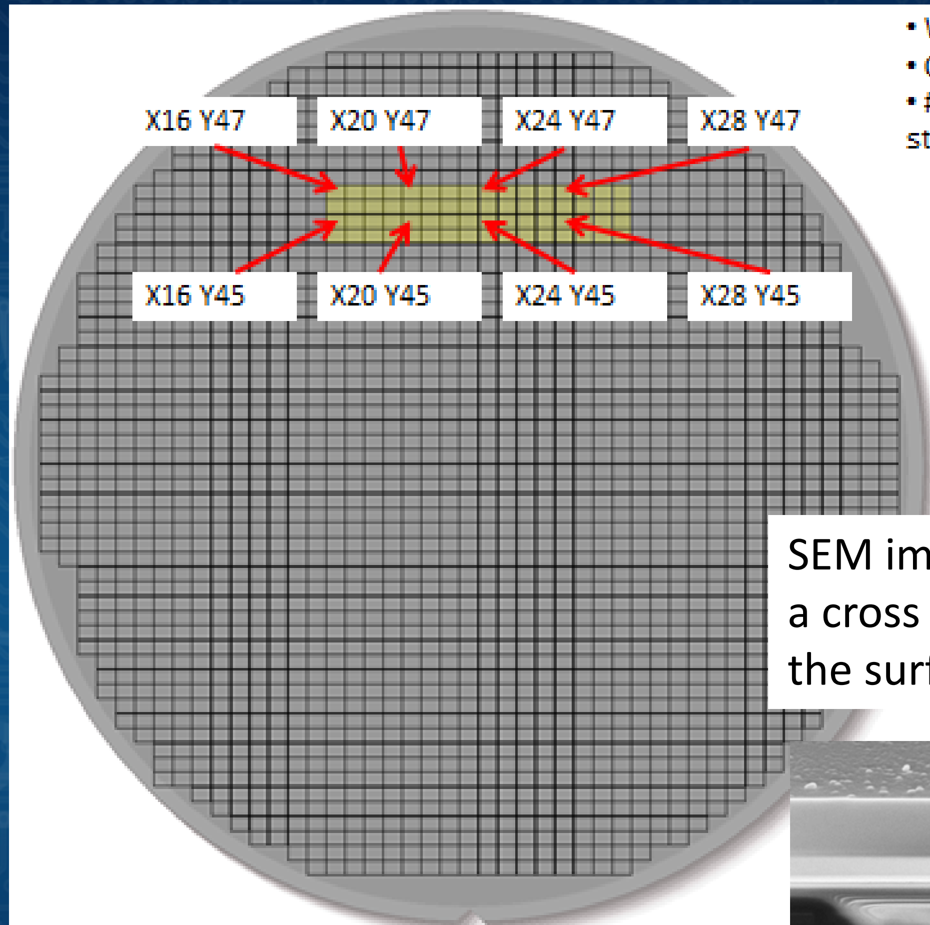
Implications of Stepping Efficiency at Probe



- Background: Material baseline moved from 2 pass probe to 4 pass probe with temperature ranging from 160C to -40C.
- Purpose: The wafer was probed in 8 sections with a various number of touchdowns by the probe card. The objective is to determine probe process margins and what section begins to exhibit probe damage to the under layers. At what level the damage exists and to quantify the amount of damage by means of de-processing.

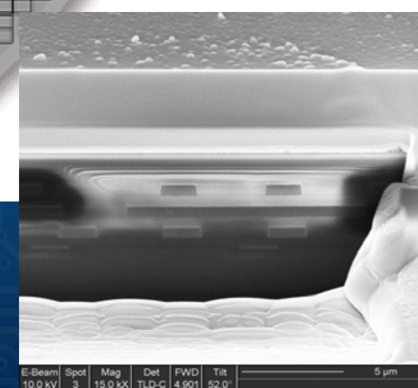
Probe DOE : Results Summary

- A new wafer probed 12x with max over travel was submitted. The locations for inspection (worst case) are highlighted on the wafer map at right.
- After optical inspection, ½ of the available locations were deprocessed while retaining the pad metallization on the remaining locations.
- Optical inspection revealed marks on top of the ILD's corresponding to the probe marks.
- A FIB cross section revealed that the marks on top of the ILD's were only a surface feature, and no cracks were observed propagating downward.



- Wafer: C-3507388-03
- OverTravel used: 100um
- # Touchdowns on each step: 12x

SEM images showing a cross section view of the surface marks.

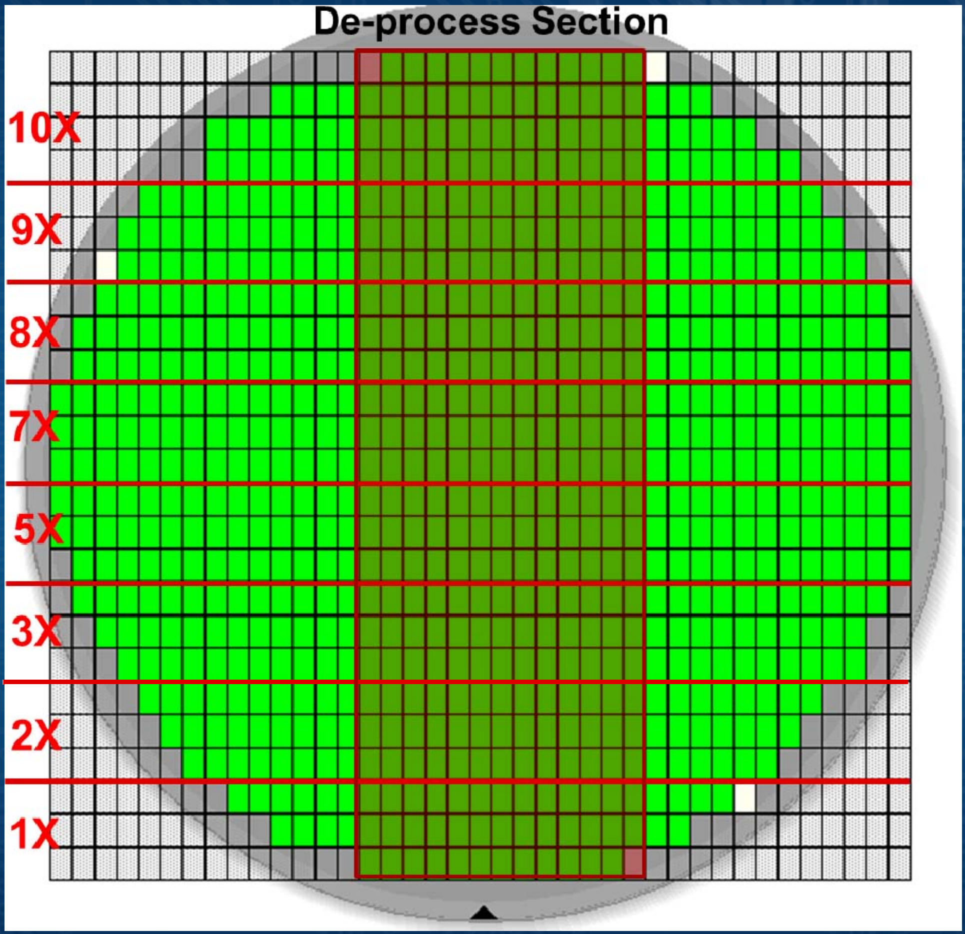


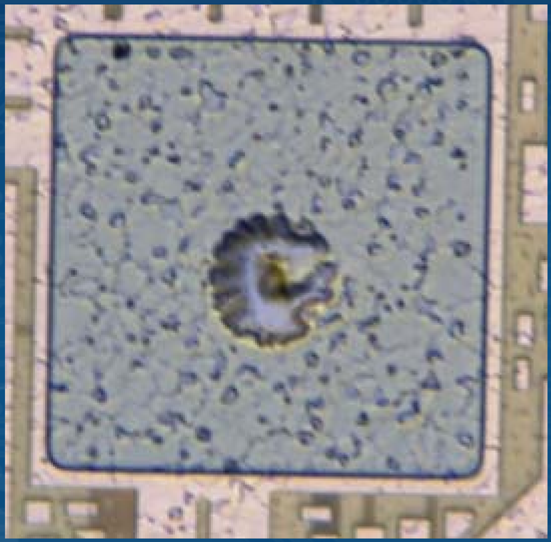
Optimizing Z speed by PC technology

New Technology Development Overview

- **Problem: Base line probing can result in cracks in a new metal stack at low touchdowns.**
- **Objective: Evaluate the effect of probing on top of new stack up with a vertical probe card to reduce cracking at low touchdowns**
  - In this study two speed features were used 5Speed Variable Control.
  - 5SVC: Step one (-500um to -91um 18000um/sec 0.2G) Step two (-90um to 0um 188um/sec 0.01G)
- **Procedure: Initial visual inspection: Several probe marks were optically inspected for the appearance of the scrub marks and for any obvious damage.**
  - De-processing: Remove Pd with 1 part HCl, 10 parts Nitric Acid, 10 parts Acetic Acid (45C, 2 minutes)
  - Inspection Criteria: 16 dies per touchdown section (4 dies per site per touchdown)
- **Conclusions: No Cracks were found at 10x touchdown at 90um probing OT**

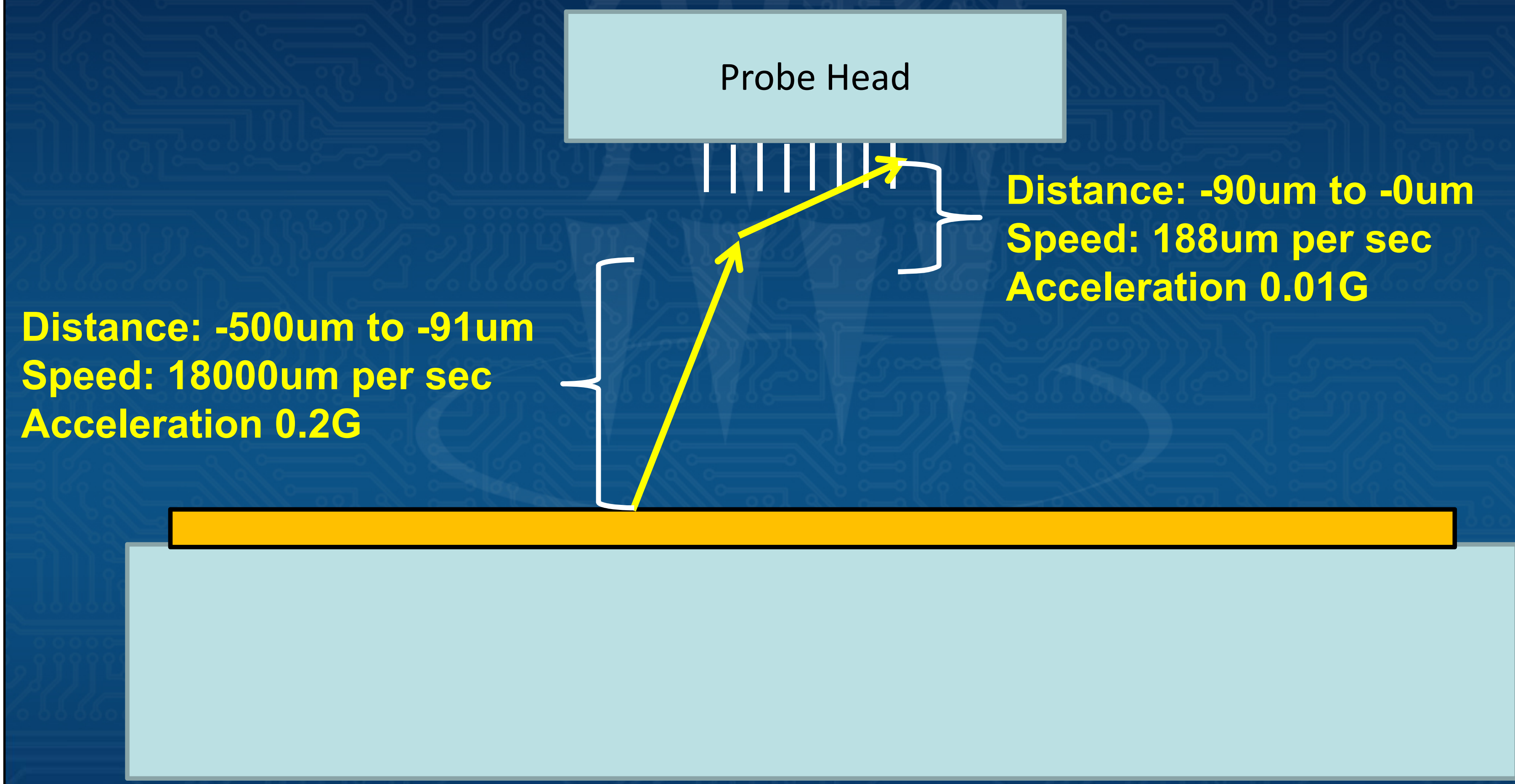
Base line Cracking Results



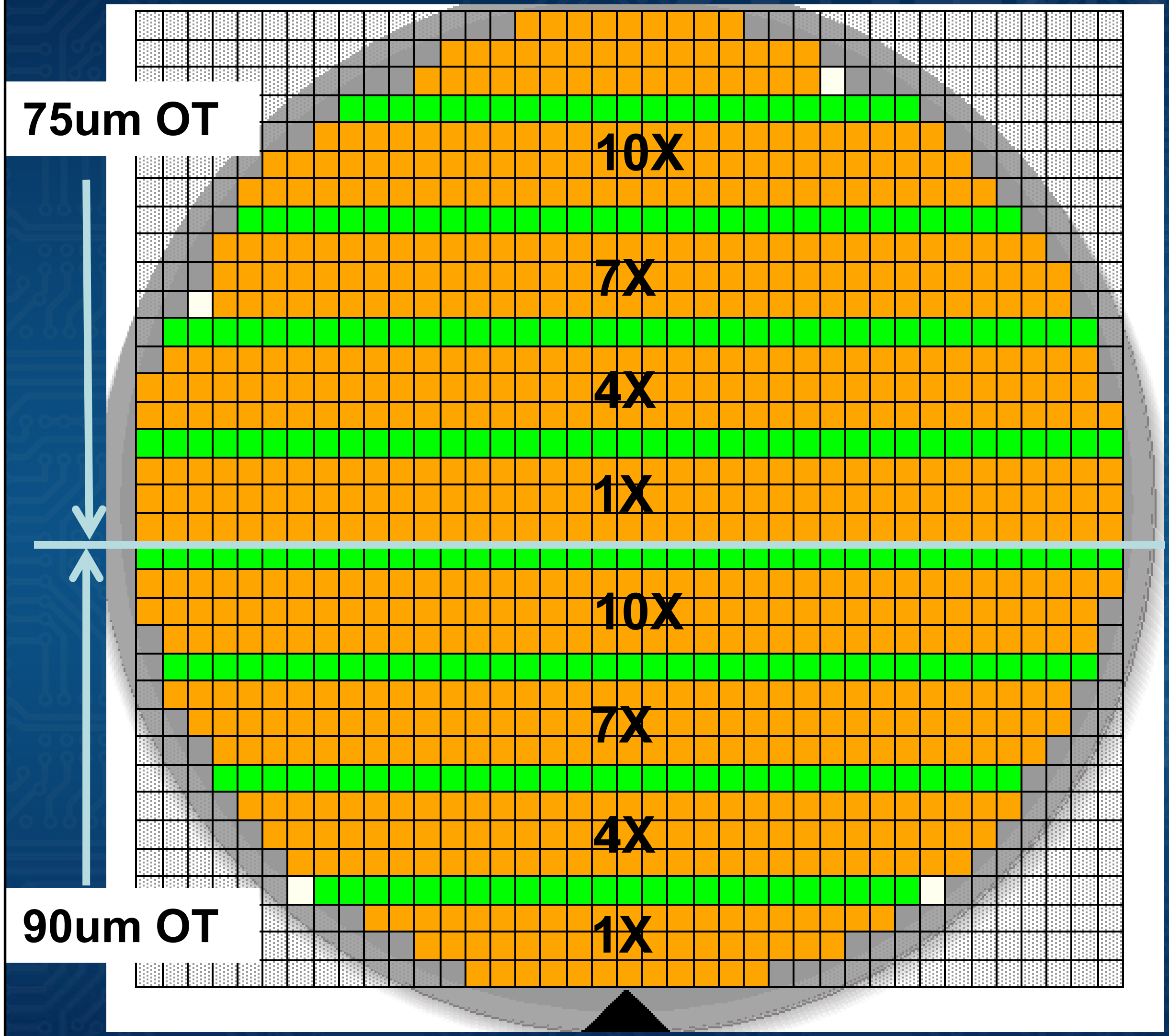


5X Touchdowns

Prober Speed Model



Probe Plan



Probe Study Info:

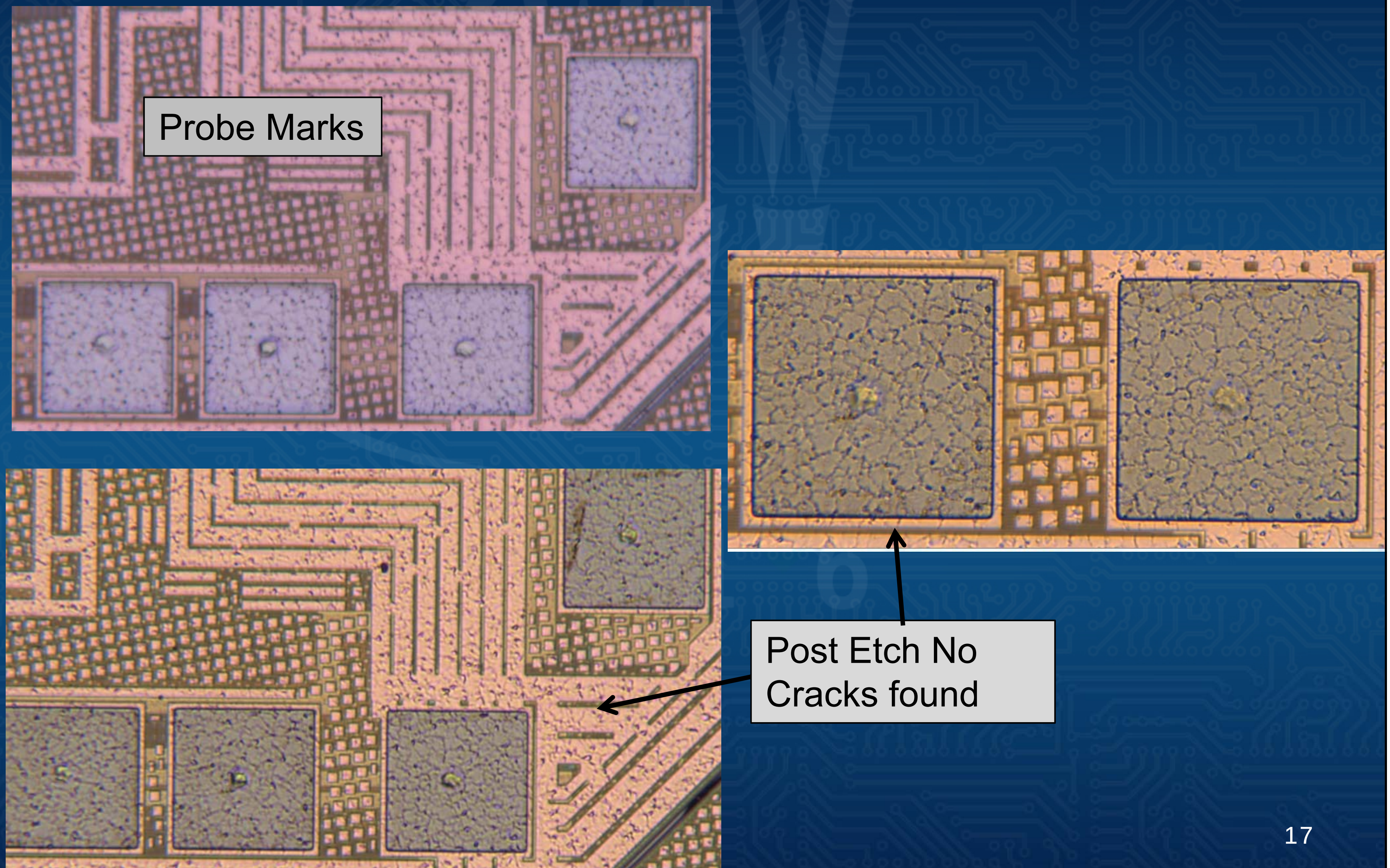
Probe Technology: 3mil
DUT Count: x2
Number or Probes:

Probing Over Travel: 75um and 90um on first touch 5SVC
Planarity: 12um

Cleaning Interval: 40/8
Cleaning Over-travel: 65um on all touch
Cleaning Media: PP150

5SVC Probe Results

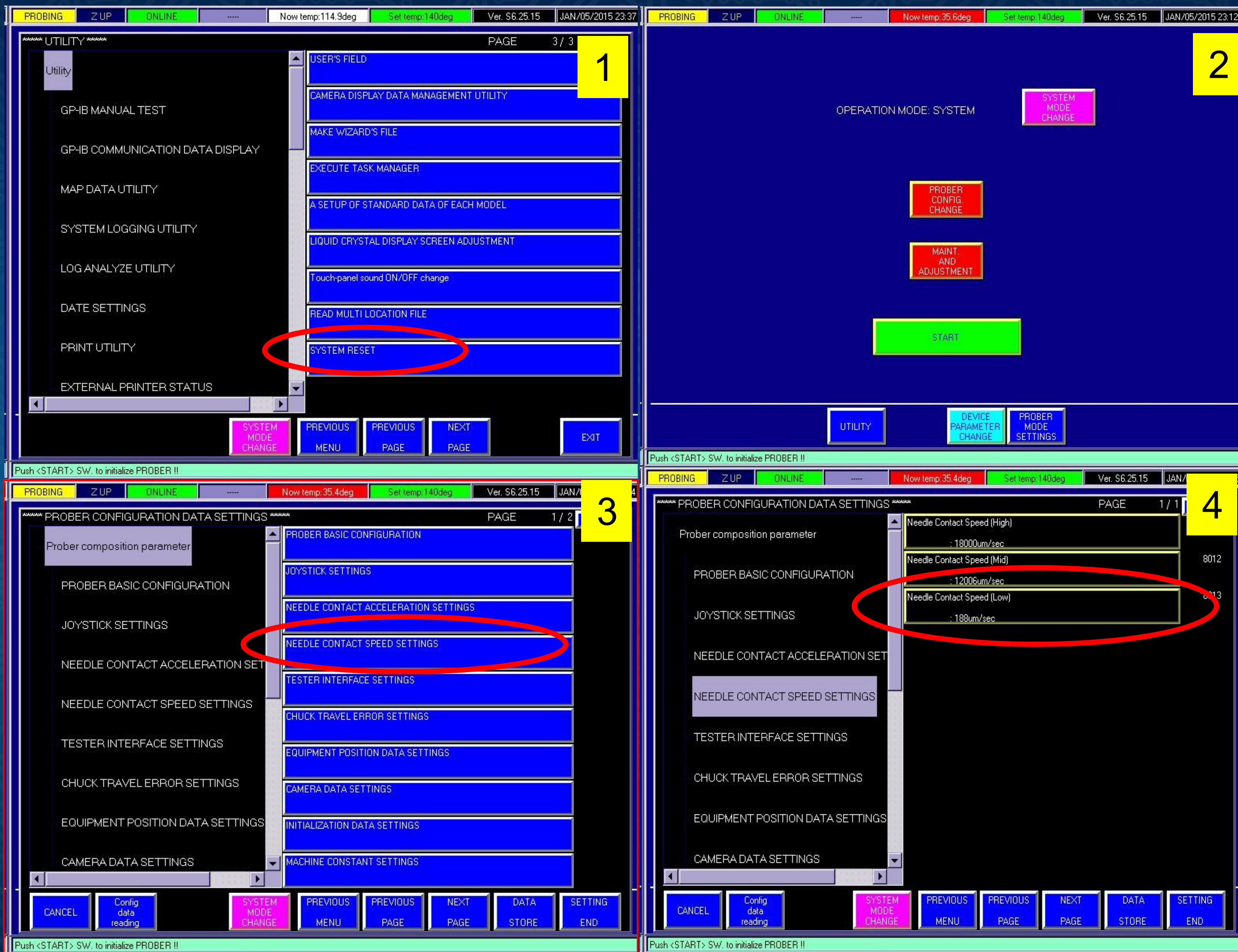
90um OT 10x Touchdowns



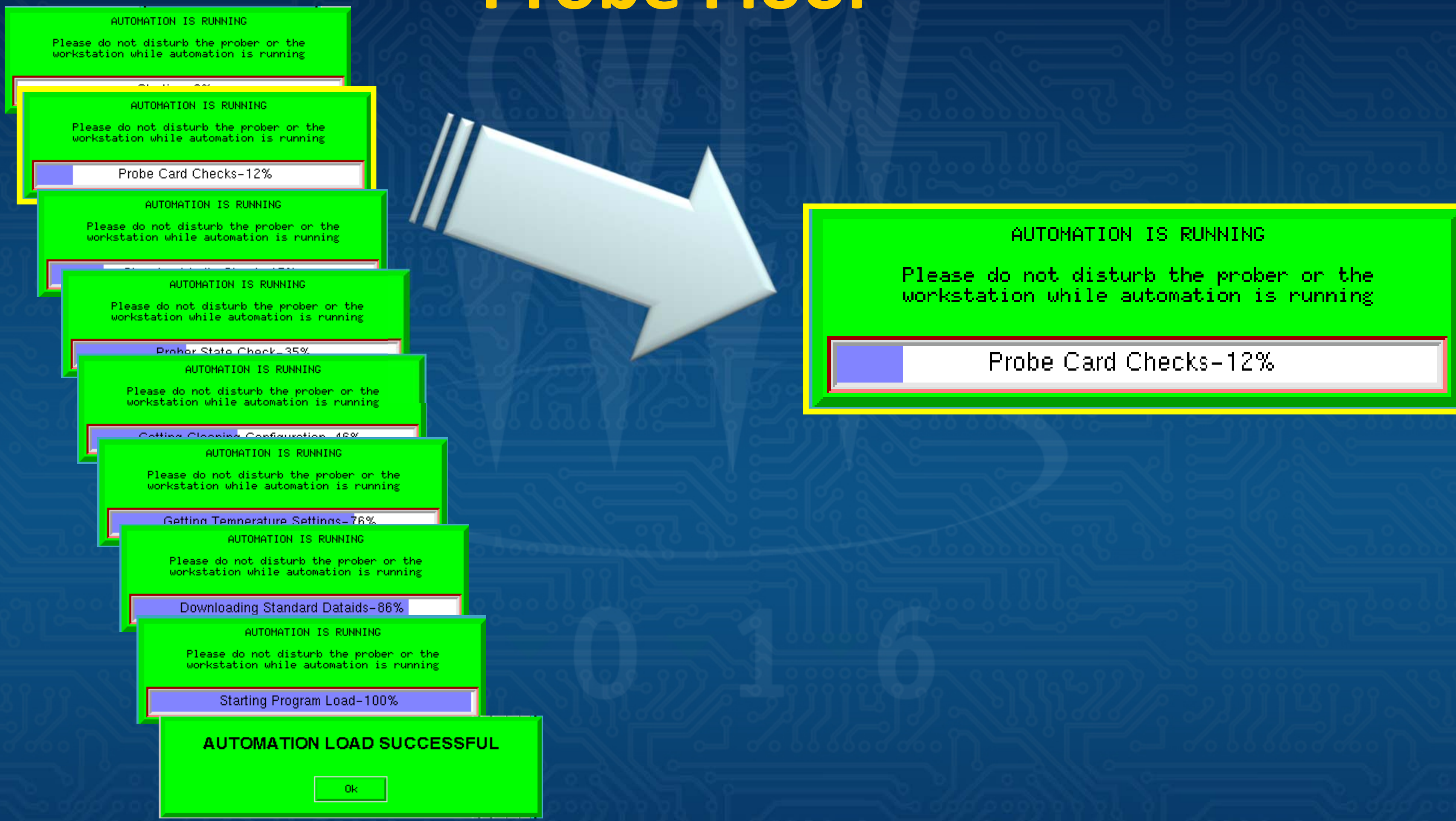
Providing an automated probe solution

June 5-8, 2016

Prober Update Procedure for 5SVC



Automated Solutions for a Production Probe Floor

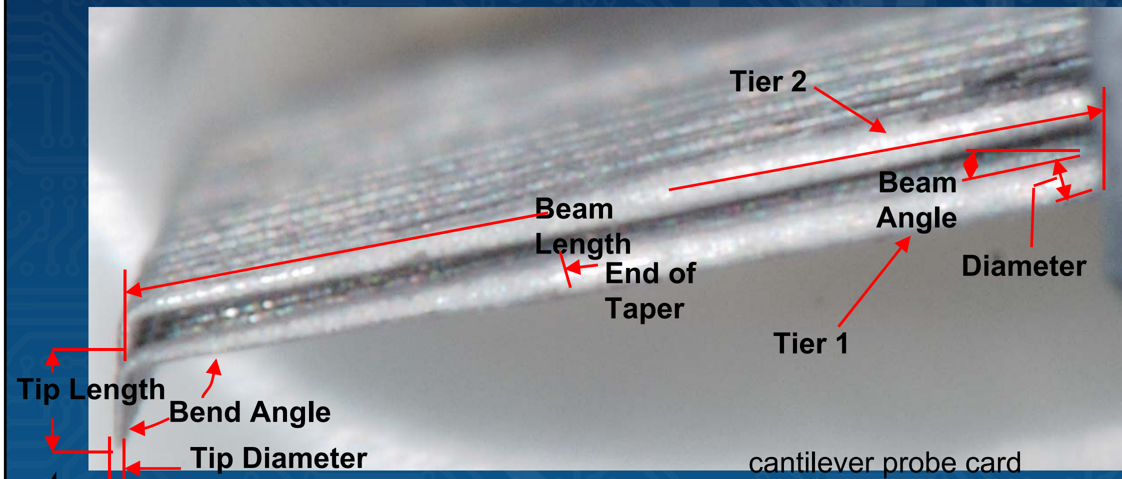


- **By specifying the probe card technology within production automation scripts the prober speed profiles can be optimized for production needs .**

PC Technology Challenges

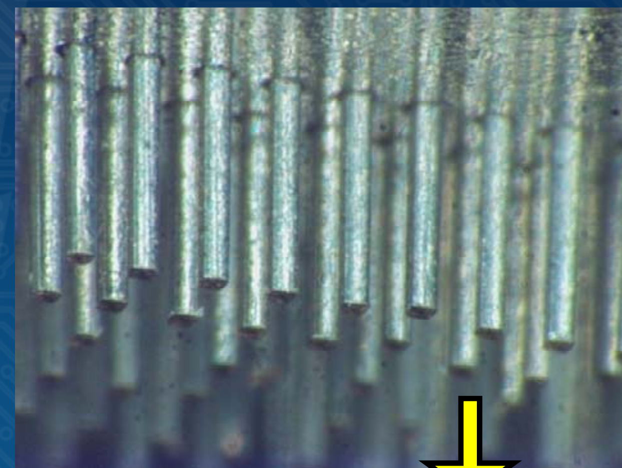
Probe Technology

Cantilever

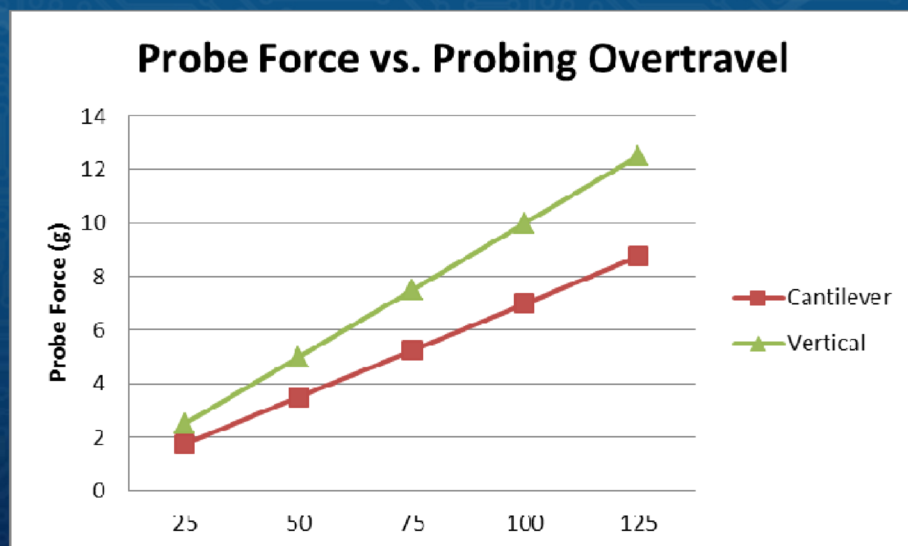


Downward and lateral force

Vertical



Downward force only



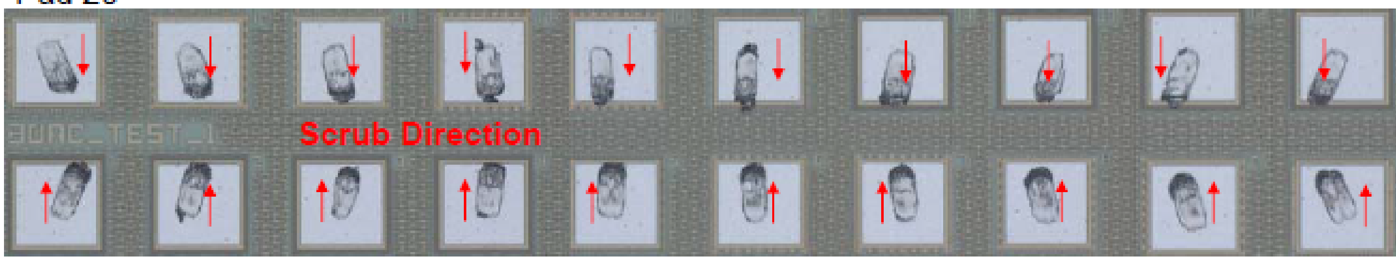
SW Test Workshop
Semiconductor Wafer Test Workshop

Silicon Design Rules for Optimized Probe Performance

June 5-8, 2016

Test Chip Cracking Study

Pad 20 ← Pad 11

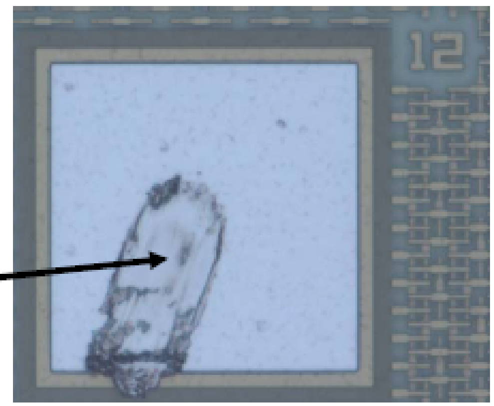


Pad 1 → Pad 10

Probed 6x touchdowns in the same location at 75um of over-travel

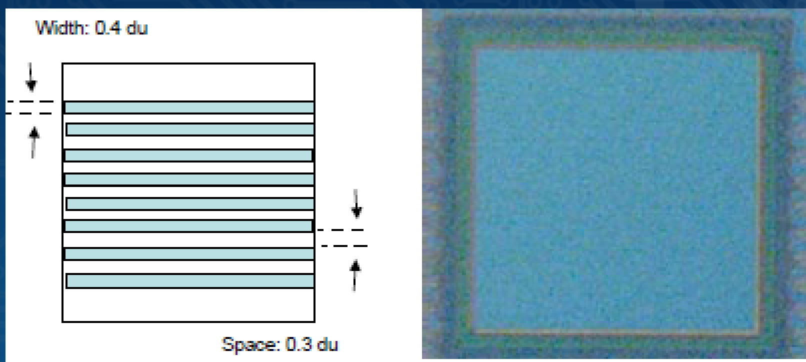
Probe marks sliding off the pad

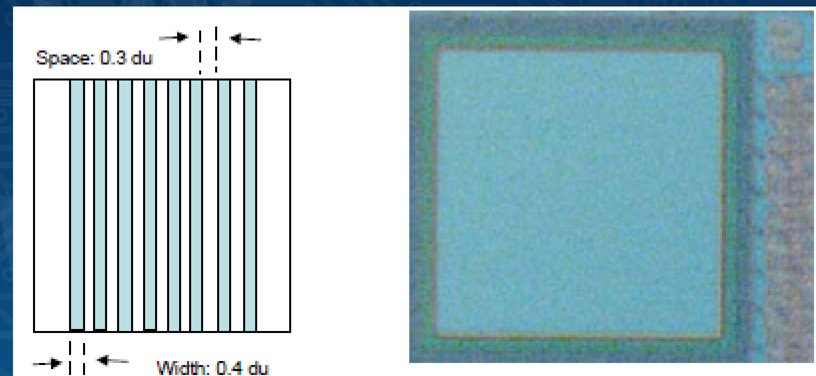
Under layer punch through

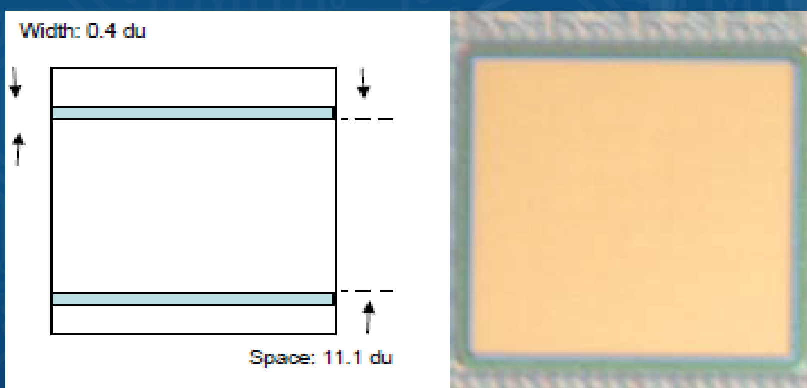


Test chip has different metal thickness and line and space designs under the probe pad

Robust Under-layer Metal design

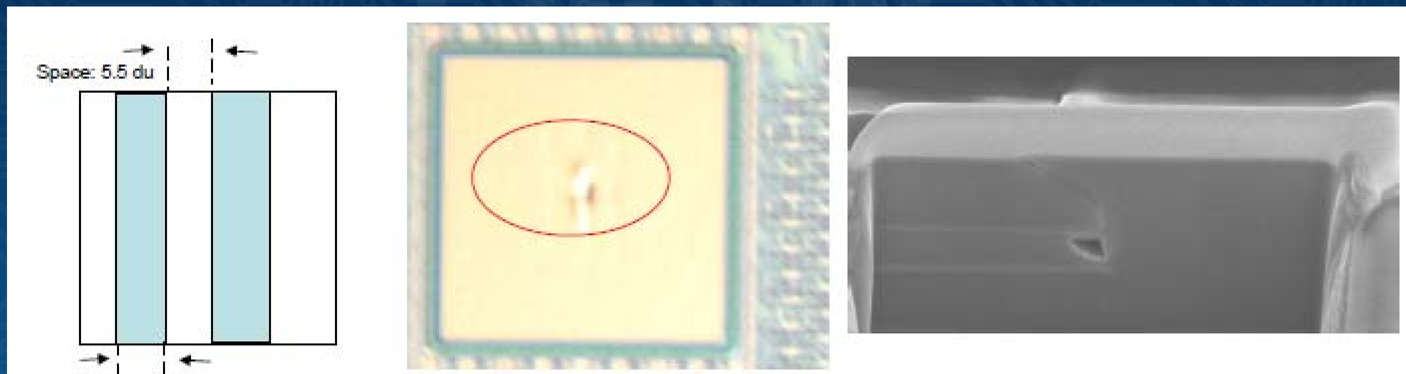


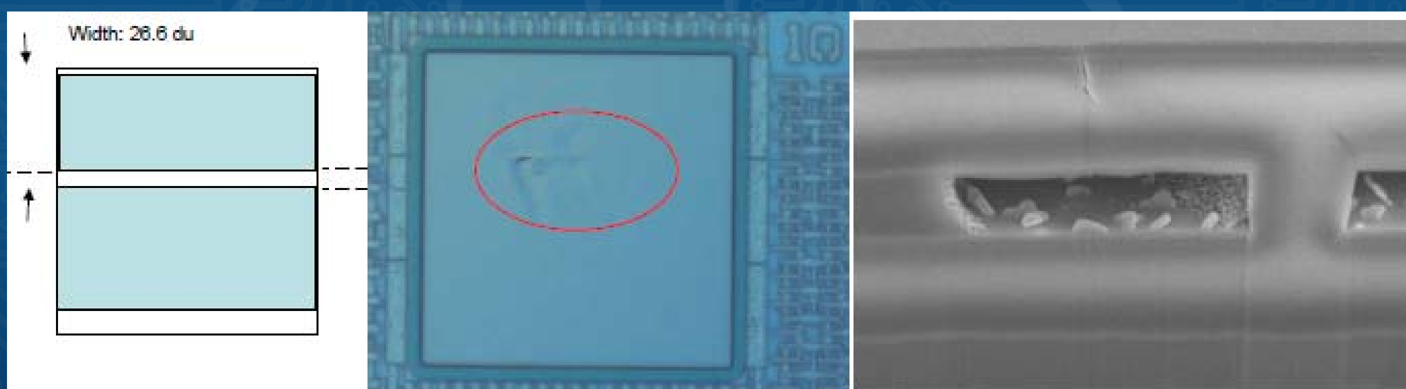




Thin line and space does not result in cracks.
Best performance occurs when probing in the direction of the trace lines

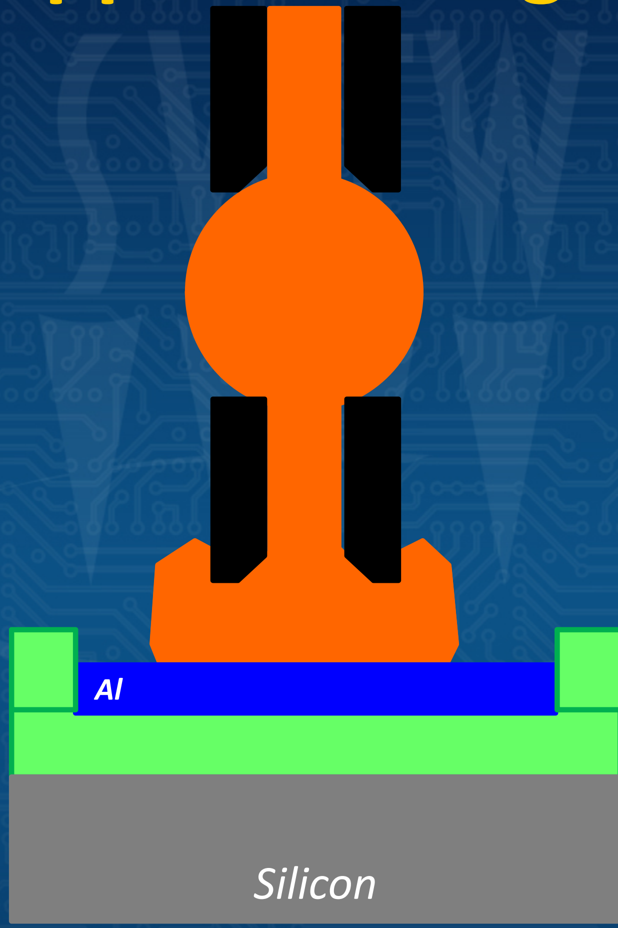
Poor Performing Metal Designs



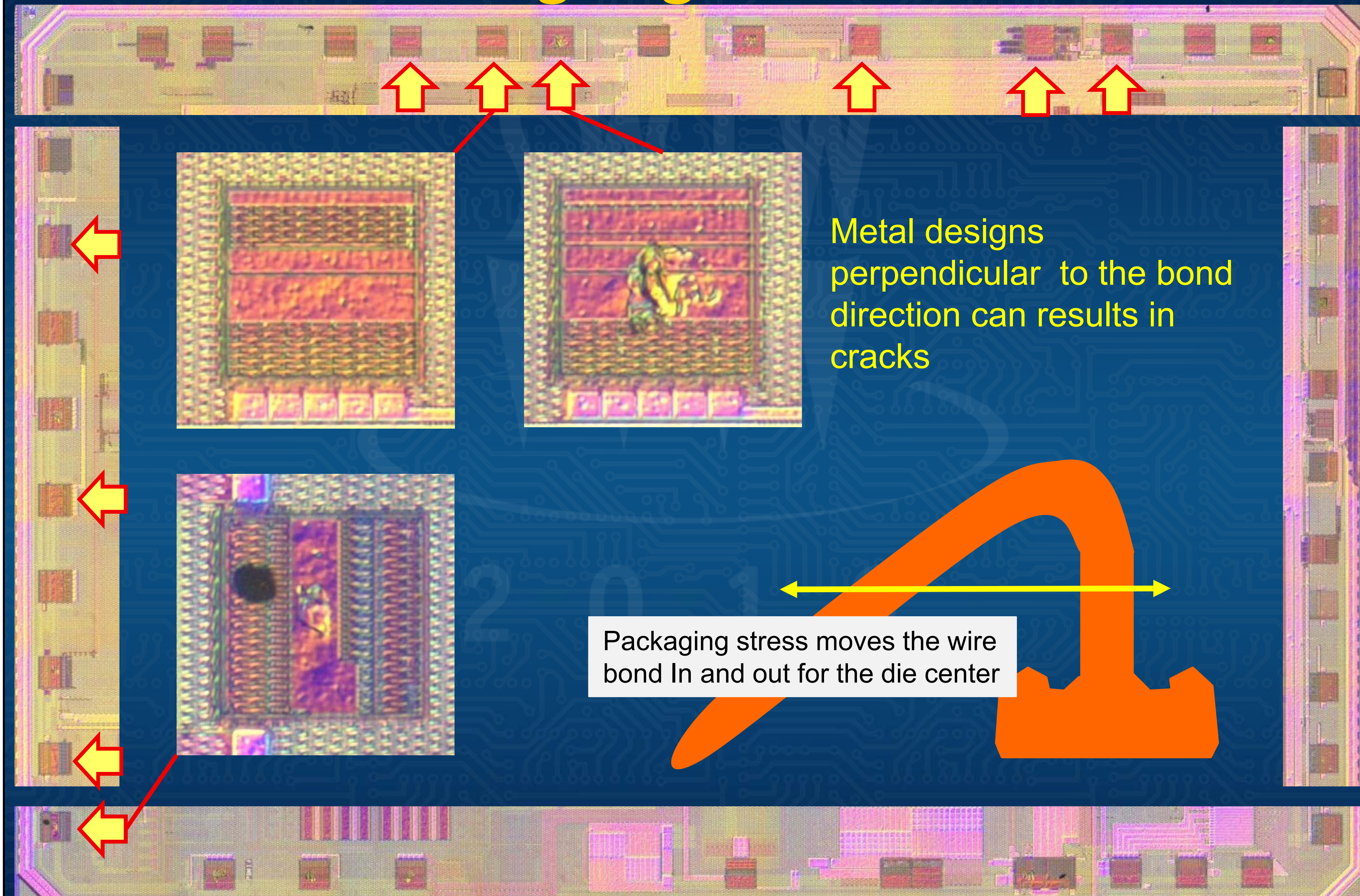


Different material elasticity between glass and metal results in a crack in the glass when wide metal traces are used

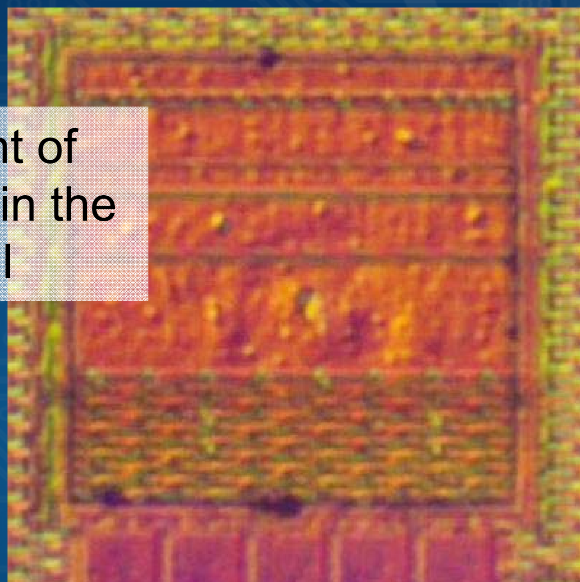
What happens during bonding?



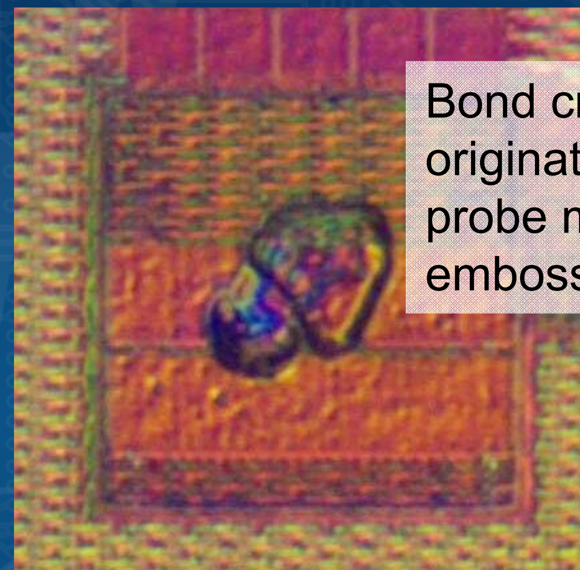
Designing for Probe



Probe Stress



Pad that is probed and not bonded



Pad that is probed and bonded

Summary of Findings

What do we know:

- **Thermal movement needs to be addressed and can add probing over travel that is unintentional**
- **Optimized touchdown speed can affect ILD cracking**
- **PC technology**
  - Thermal compensation for at temperature probing.
  - Optimization of prober performance and identification of prober deficiencies.
  - Solutions for high pin count / low force needed
- **End solution is Si design**
  - Design for robust stack up build a higher quality IC for production use

What is still to come:

- **Design in quality and minimize probe damage for our customers.**

Acknowledgements

- Connie Smith
- Imran Ahmed
- Brennan Tran
- Thomas Vaughan
- Al Griffin