SW Test Workshop
Semiconductor Wafer Test Workshop

A Customized Additional Advanced Loopback technology on Vertical Probe Card

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Overview

- Objectives
- Introduction
- Design of experiment robust
- Electrical Performance
- Experiment Validation
- Summary / Q & A

Overview

- **Objectives**
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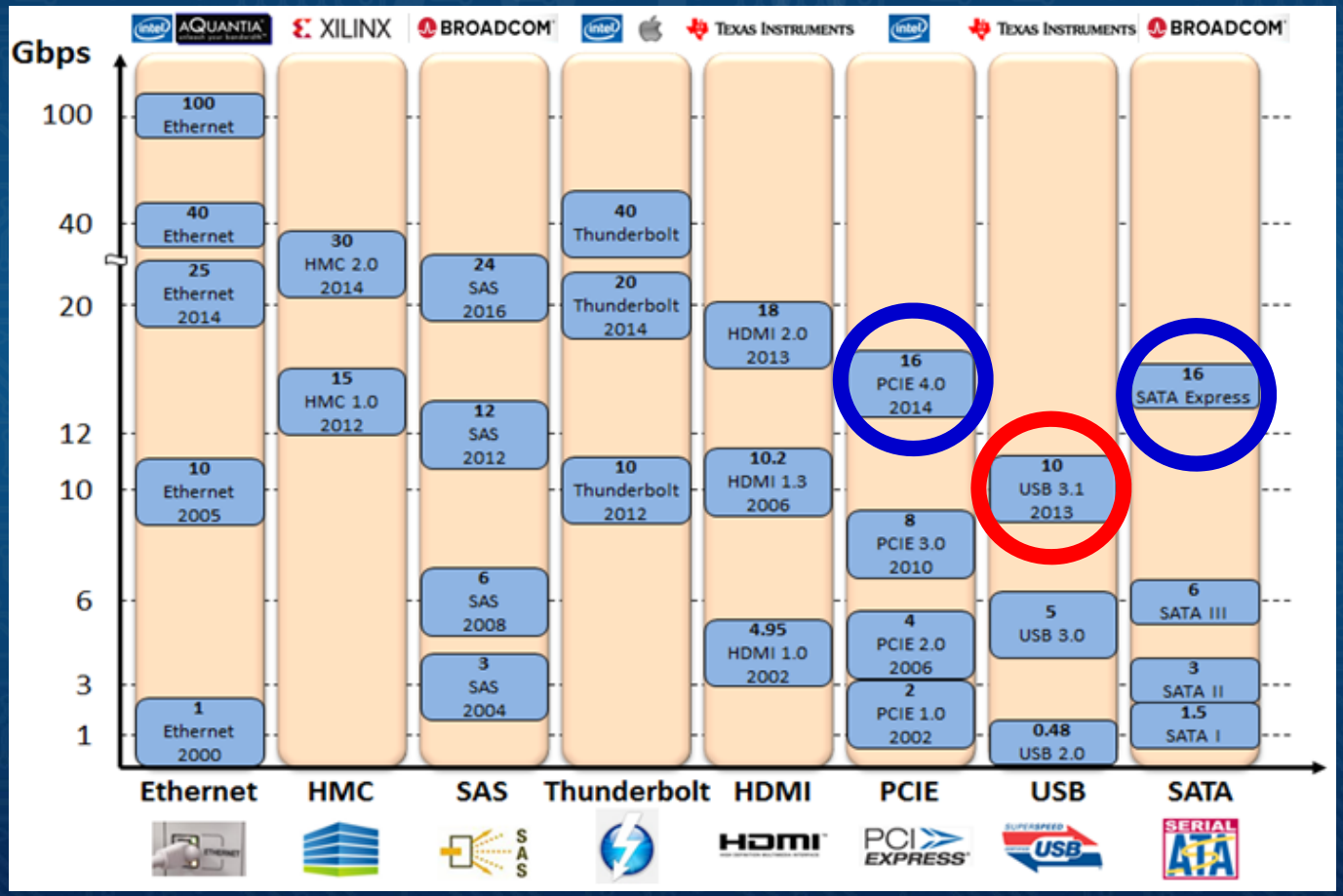
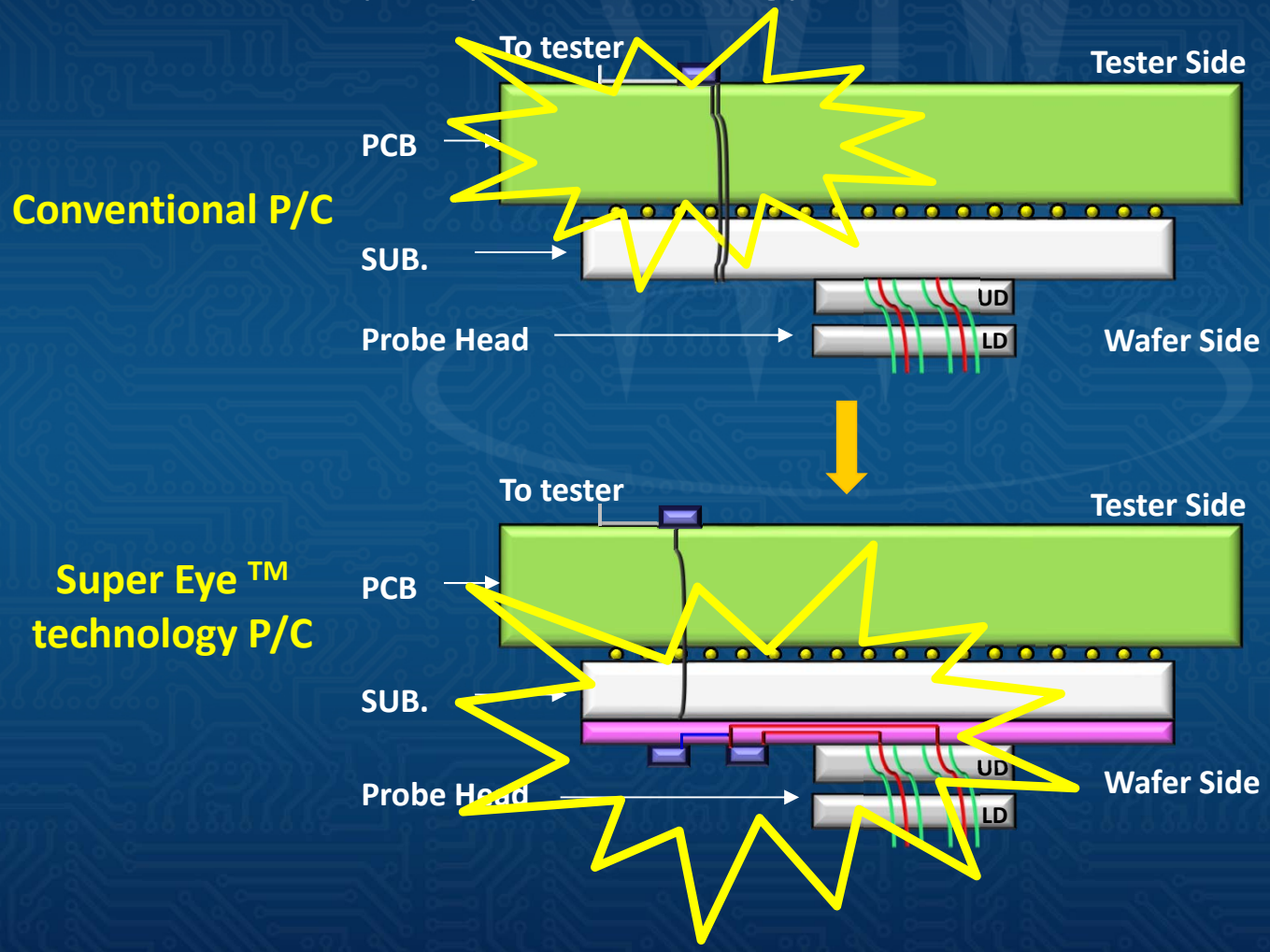
Objectives

- The high-speed transmission interface(such as: USB, SATA, PCIE,…) on wafer testing is increasingly demanding the high speed probing solution.



Objectives

- What is Super Eye ™ technology ?



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Introduction

- What is multilayer organic ceramic (MLOC)?

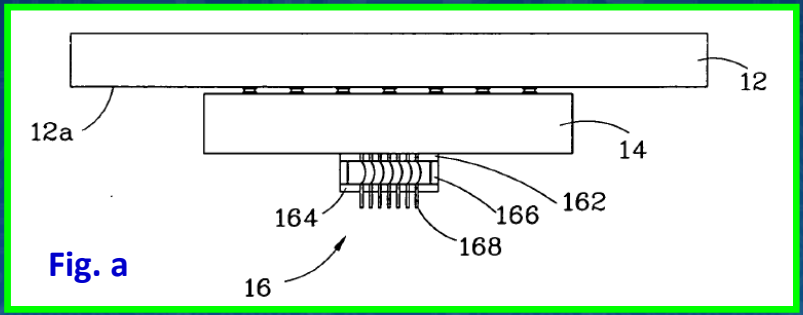


Fig. a

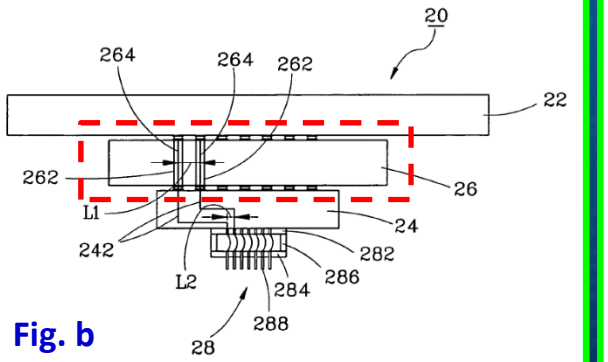


Fig. b

Additional S/B

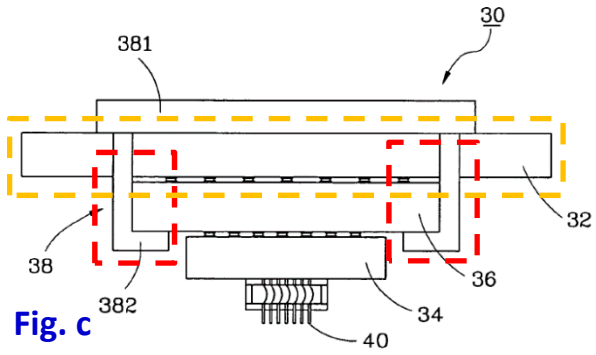


Fig. c

Fix with holder

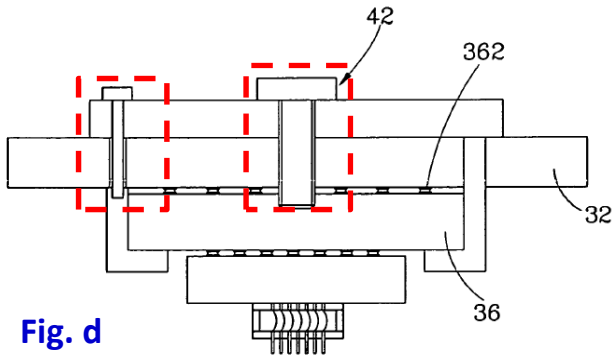


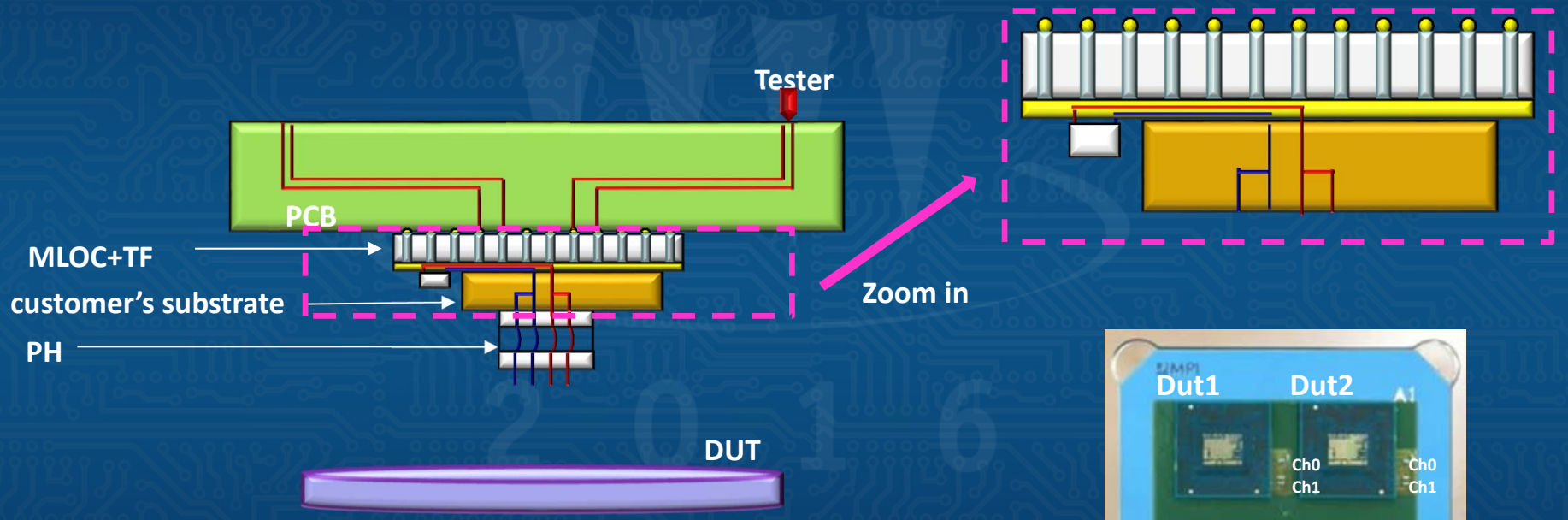
Fig. d

Fix with screw

MPI patent pending

Introduction

- Application of MLOC : In this case, we fabricated S/B in ceramic and contacted customer's substrate with IP and reflow technology.



Side view

Top view

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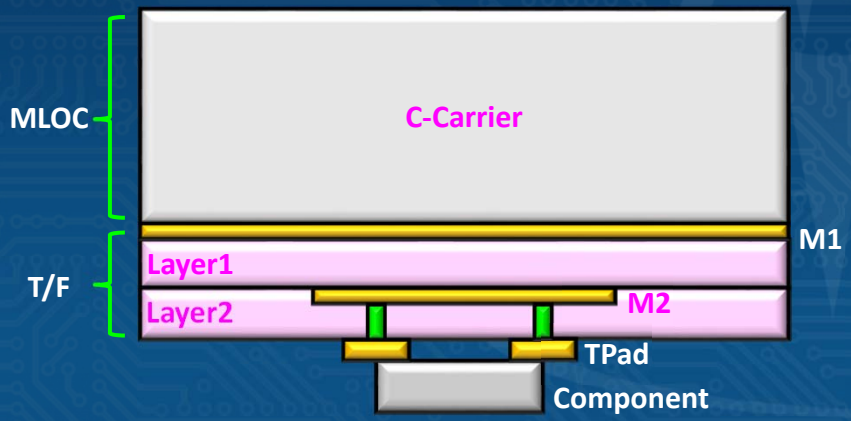
Design of experiment robust

- Adopt Taguchi method for robust design



Structure	Item
Layer 1	M1
	Via1
Layer 2	M2
	Via2
TPad	TPad

Factor effects:

- Solder ball
- Permittivity
- Substrate thickness
- Substrate loss
- Matching impedance
- Metal thickness
- Metal conductivity

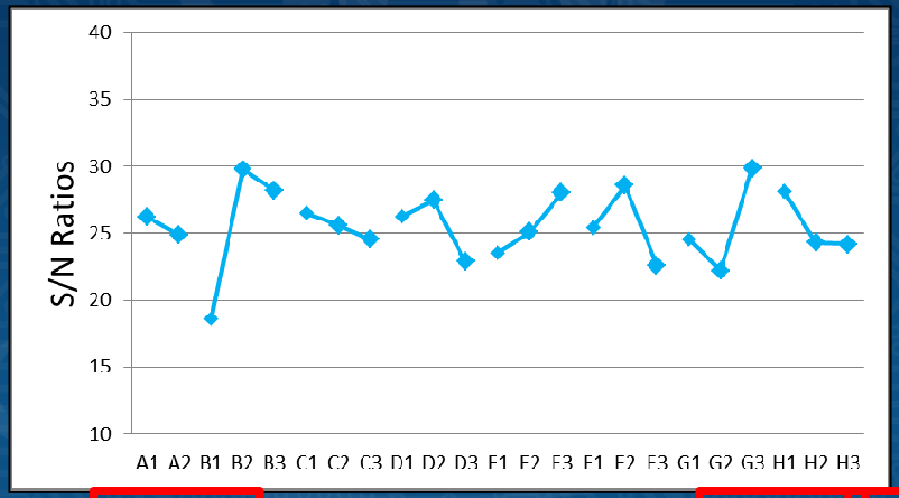
Design of experiment robust

- Taguchi method : Orthogonal array & experimental Log/Data (Parameters A~H stand for factors that affect our result.)

Experiment	A	B	C	D	E	F	G	H	Quality Characteristic	S/N Ratios
1	1	1	1	1	1	1	1	1	5.58	19.664
2	1	1	2	2	2	2	2	2	5.68	18.437
3	1	1	3	3	3	3	3	3	5.79	17.301
4	1	2	1	1	2	2	3	3	4.94	38.312
5	1	2	2	2	3	3	1	1	5.1	34.151
6	1	2	3	3	1	1	2	2	5.51	20.672
7	1	3	1	2	1	3	2	3	4.65	22.468
8	1	3	2	3	2	1	3	1	4.89	32.958
9	1	3	3	1	3	2	1	2	4.88	32.185
10	2	1	1	3	3	2	2	1	5.44	21.843
11	2	1	2	1	1	3	3	2	5.75	17.692
12	2	1	3	2	2	1	1	3	5.85	16.755
13	2	2	1	2	3	1	3	2	4.93	36.955
14	2	2	2	3	1	2	1	3	5.31	24.675
15	2	2	3	1	2	3	2	1	5.33	24.164
16	2	3	1	3	2	3	1	2	4.54	19.886
17	2	3	2	1	3	1	2	3	4.75	25.575
18	2	3	3	2	1	2	3	1	5.08	36.055

Design of experiment robust

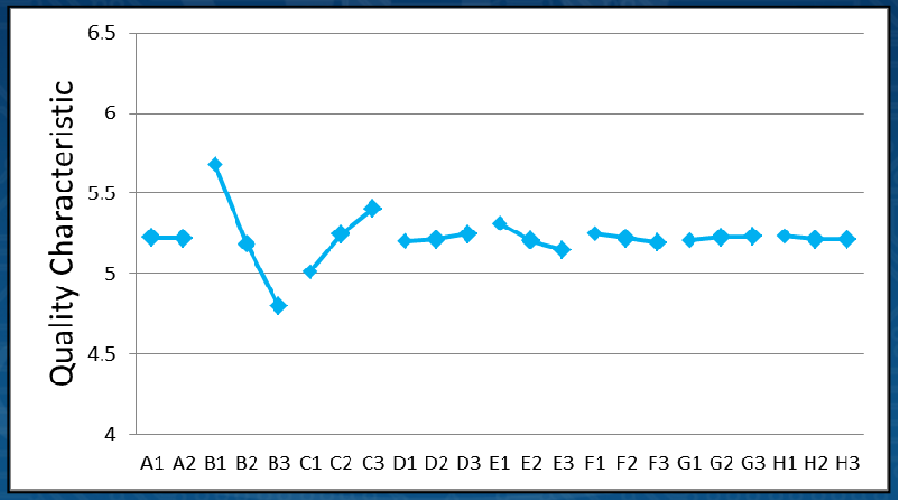
- Taguchi method : S/N ratios response table/Graph



S/N Ratios Response Table	A	B	C	D	E	F	G	H
Level 1	26.24	18.62	26.52	26.27	23.54	25.43	24.55	28.14
Level 2	24.84	29.82	25.58	27.47	25.09	28.58	22.19	24.3
Level 3	-	28.19	24.52	22.89	28	22.61	29.88	24.18
$E^{1\to2}$	-1.39	11.21	-0.94	1.205	1.548	3.155	-2.36	-3.84
$E^{2\to3}$	-	-1.63	-1.06	-4.58	2.916	-5.97	7.686	-0.12
Range	1.394	12.84	1.999	5.786	4.464	9.128	10.05	3.959
Rank	8	1	7	4	5	3	2	6
Significant	no	yes	no	yes	yes	yes	yes	no

Design of experiment robust

- Taguchi method : Quality characteristic response table/Graph

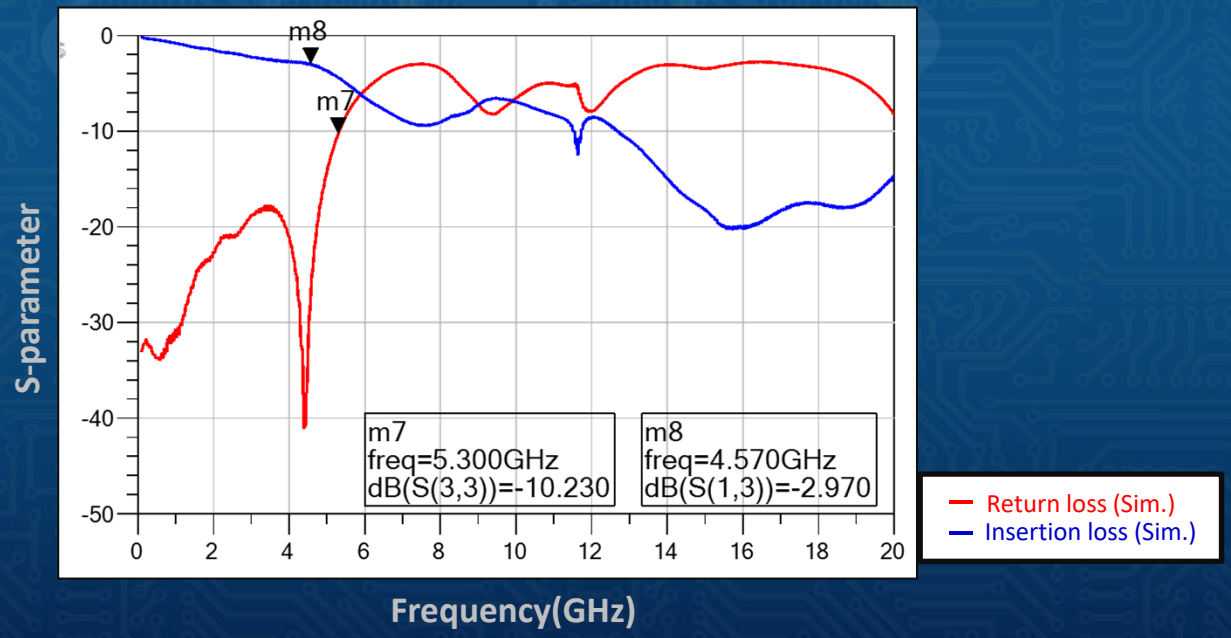


Quality Characteristic Response Table	A	B	C	D	E	F	G	H
Level 1	5.224	5.682	5.013	5.205	5.313	5.252	5.21	5.237
Level 2	5.22	5.187	5.247	5.215	5.205	5.222	5.227	5.215
Level 3	-	4.798	5.407	5.247	5.148	5.193	5.23	5.215
$E^{1\to2}$	-0.004	-0.5	0.233	0.01	-0.11	-0.03	0.017	-0.02
$E^{2\to3}$	-	-0.39	0.16	0.032	-0.06	-0.03	0.003	0
Range	0.004	0.883	0.393	0.042	0.165	0.058	0.02	0.022
Rank	8	1	3	5	4	2	7	6
Significant	no	yes	yes	yes	yes	yes	no	no

Design of experiment robust

- Benefit on Taguchi method, we had verified for robust performance

Factor Level	S/N effect ?	Quality Characteristic effect ?	Control factors
1	yes	yes / no	B, D, E, F,G
2	no	yes	C
3	no	no	A, H



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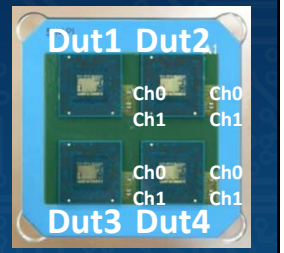
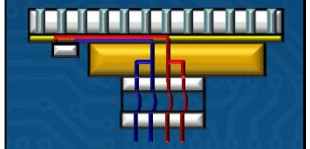
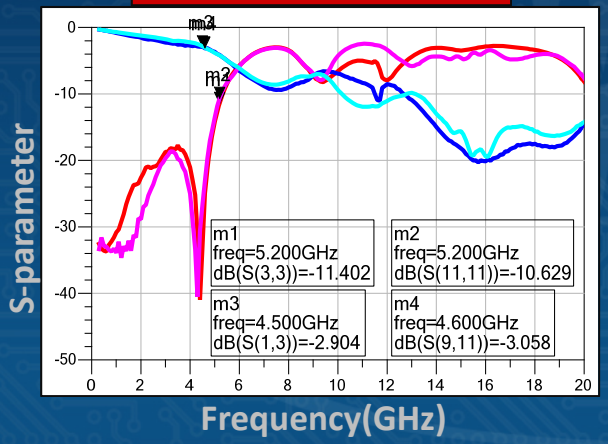
Electrical Performance

- Simulation and measurement result: Consistent and Reappear!

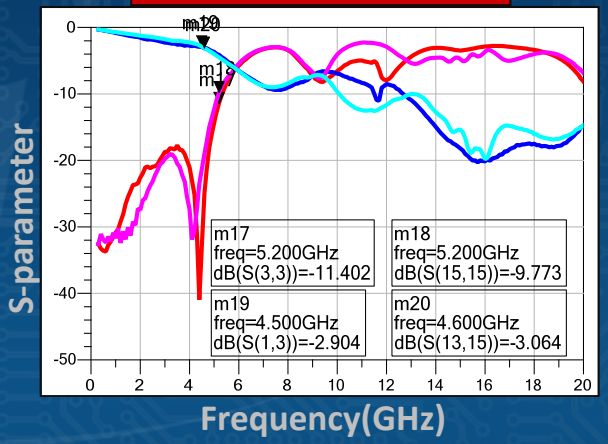




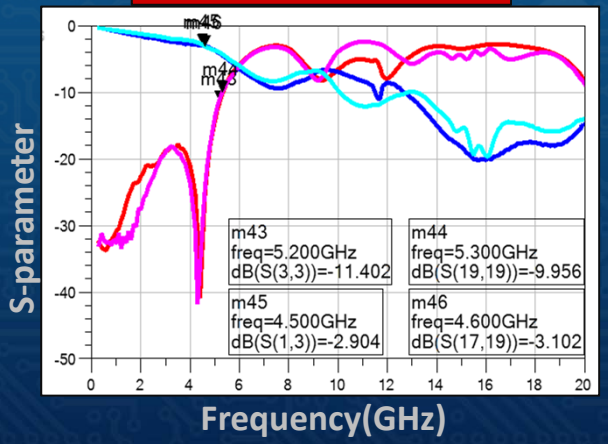
DUT1-Channel 0



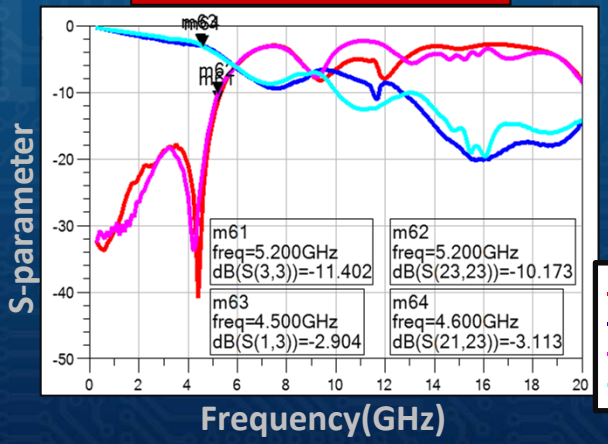
DUT2-Channel 0

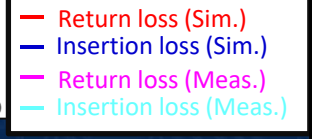


DUT3-Channel 0



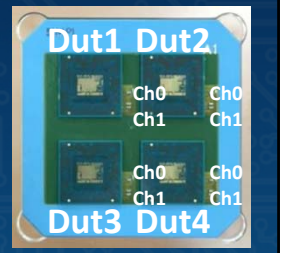
DUT4-Channel 0

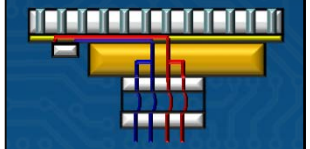




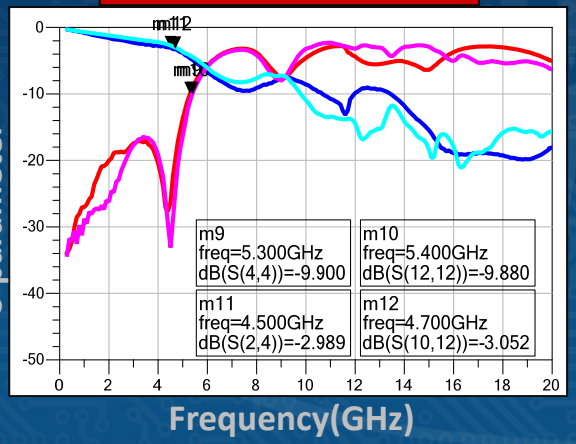
Electrical Performance

- Simulation and measurement result: Consistent and Reappear!

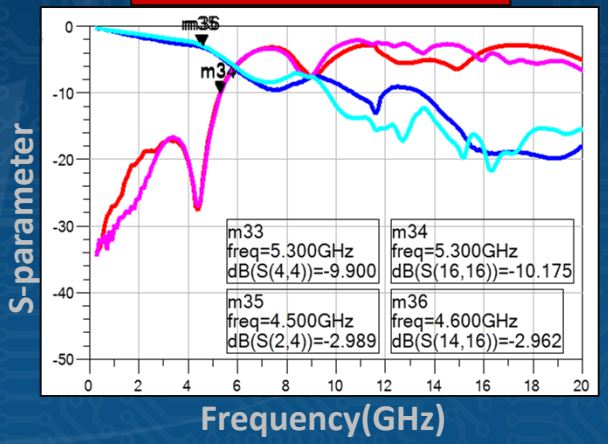




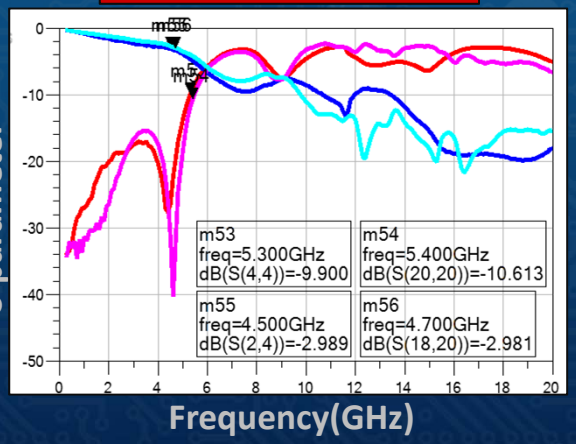
◆ DUT1-Channel 1



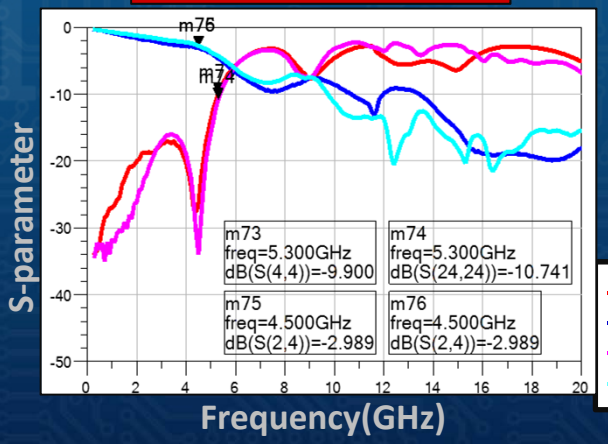
◆ DUT2-Channel 1

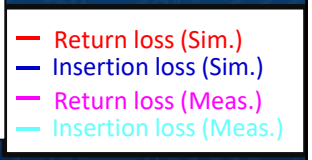


◆ DUT3-Channel 1



◆ DUT4-Channel 1

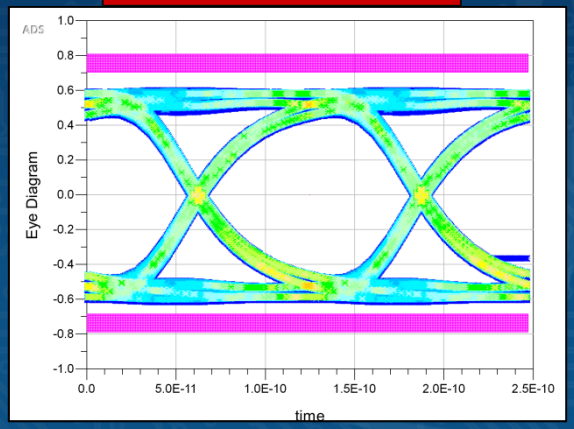




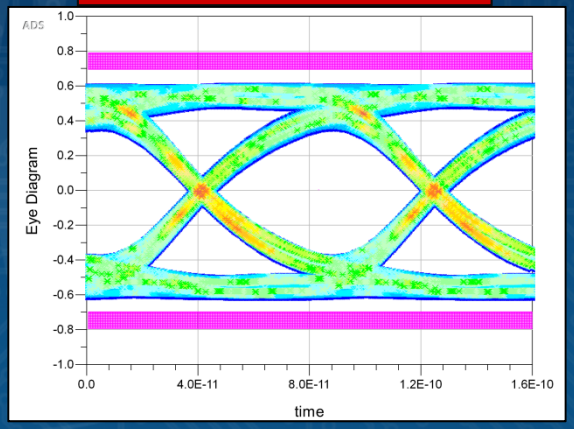
Electrical Performance

- Eye diagram : Simulation of Dut1-channel 0

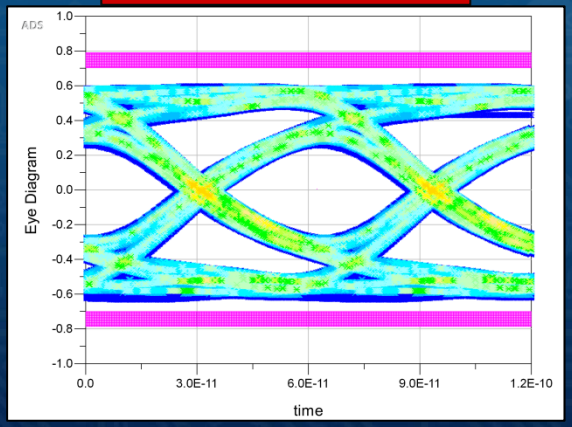
◆ Data rate 8Gbps



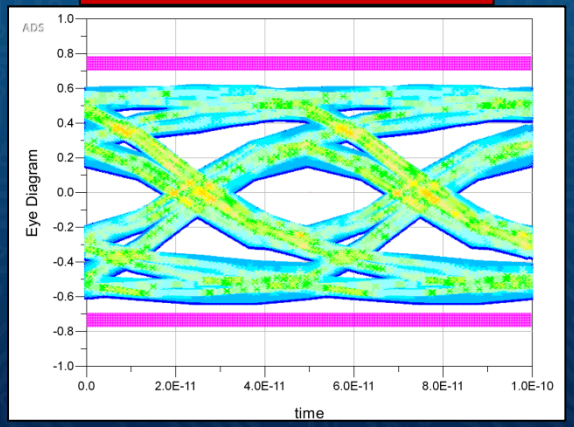
◆ Data rate 12Gbps



◆ Data rate 16Gbps



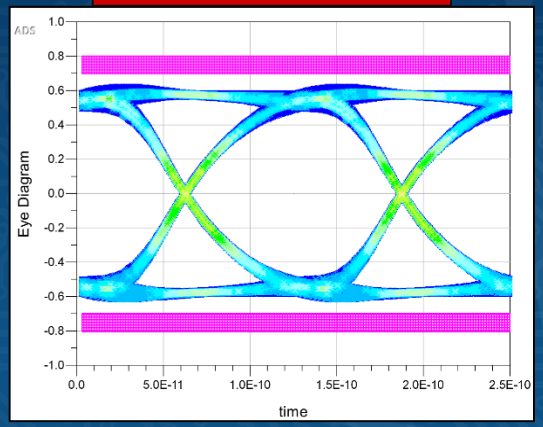
◆ Data rate 20Gbps



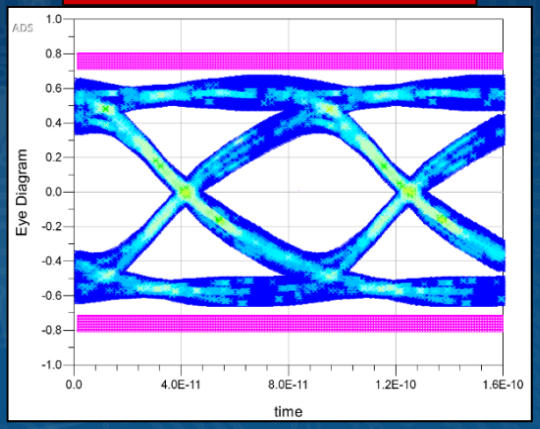
Electrical Performance

- Eye diagram : Measurement of Dut1-channel 0

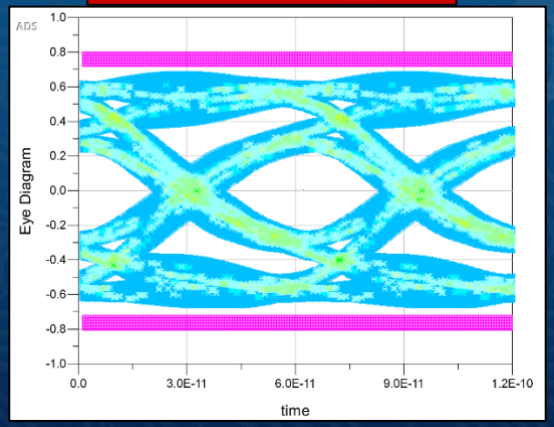
◆ Data rate 8Gbps



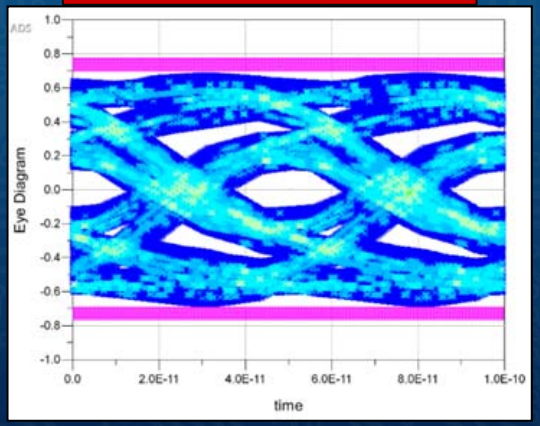
◆ Data rate 12Gbps



◆ Data rate 16Gbps



◆ Data rate 20Gbps



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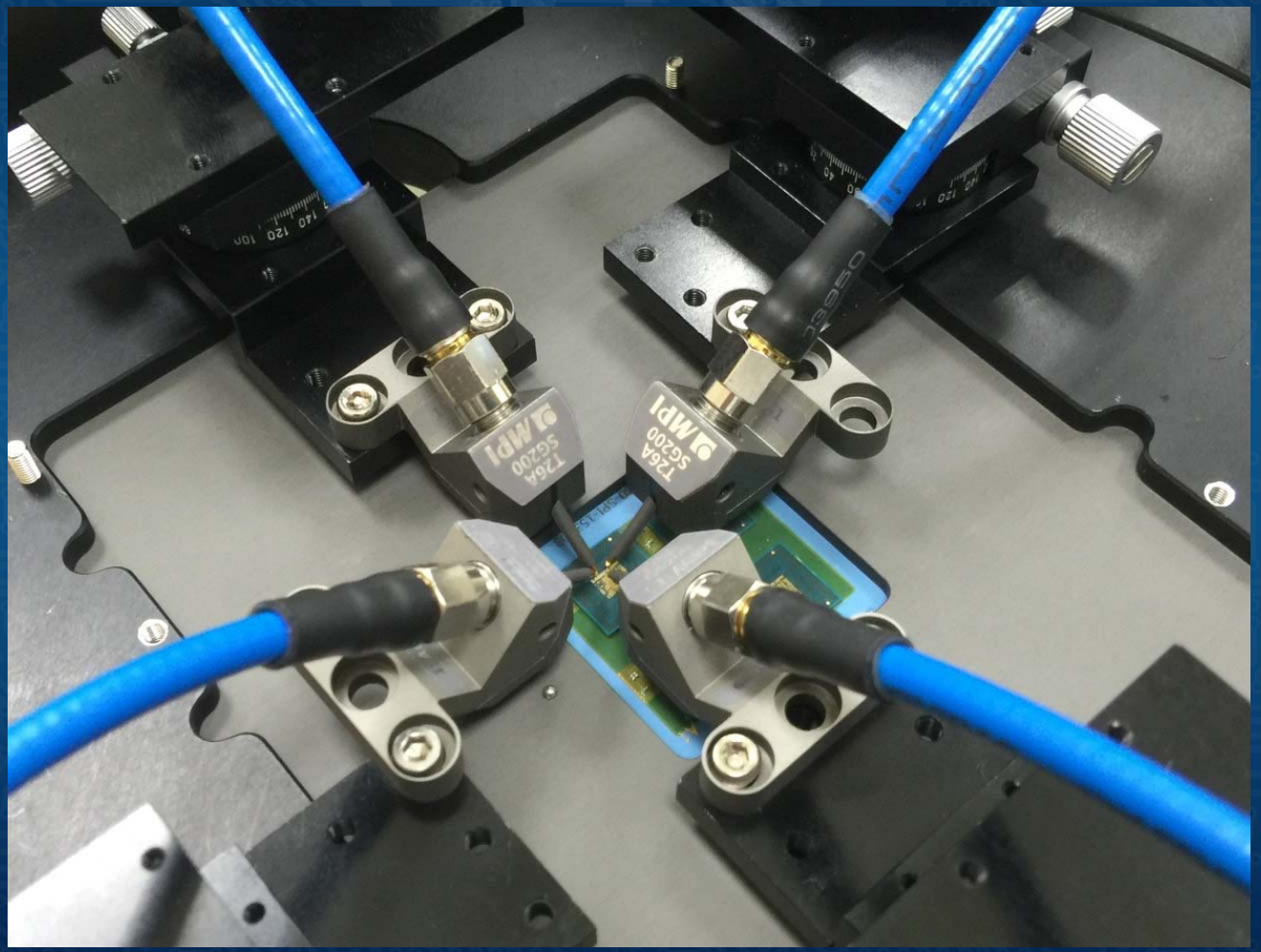
Experiment Validation

- Measurement system



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Summary

- 1. Benefit on MLOC/MLOO technology, even if customer provided substrate is uneven, we have good solution for testing without changing customer's substrate structure.
- 2. With Taguchi method, our design can be more effective and perform great consistent in simulation and measurement results.
- 3. In the future development, we will keep working on increasing bandwidth and data speed.

Acknowledgements

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(MPI)

Q & A

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Thanks for Listening!