Test and Validation in an Analog and Embedded Environment

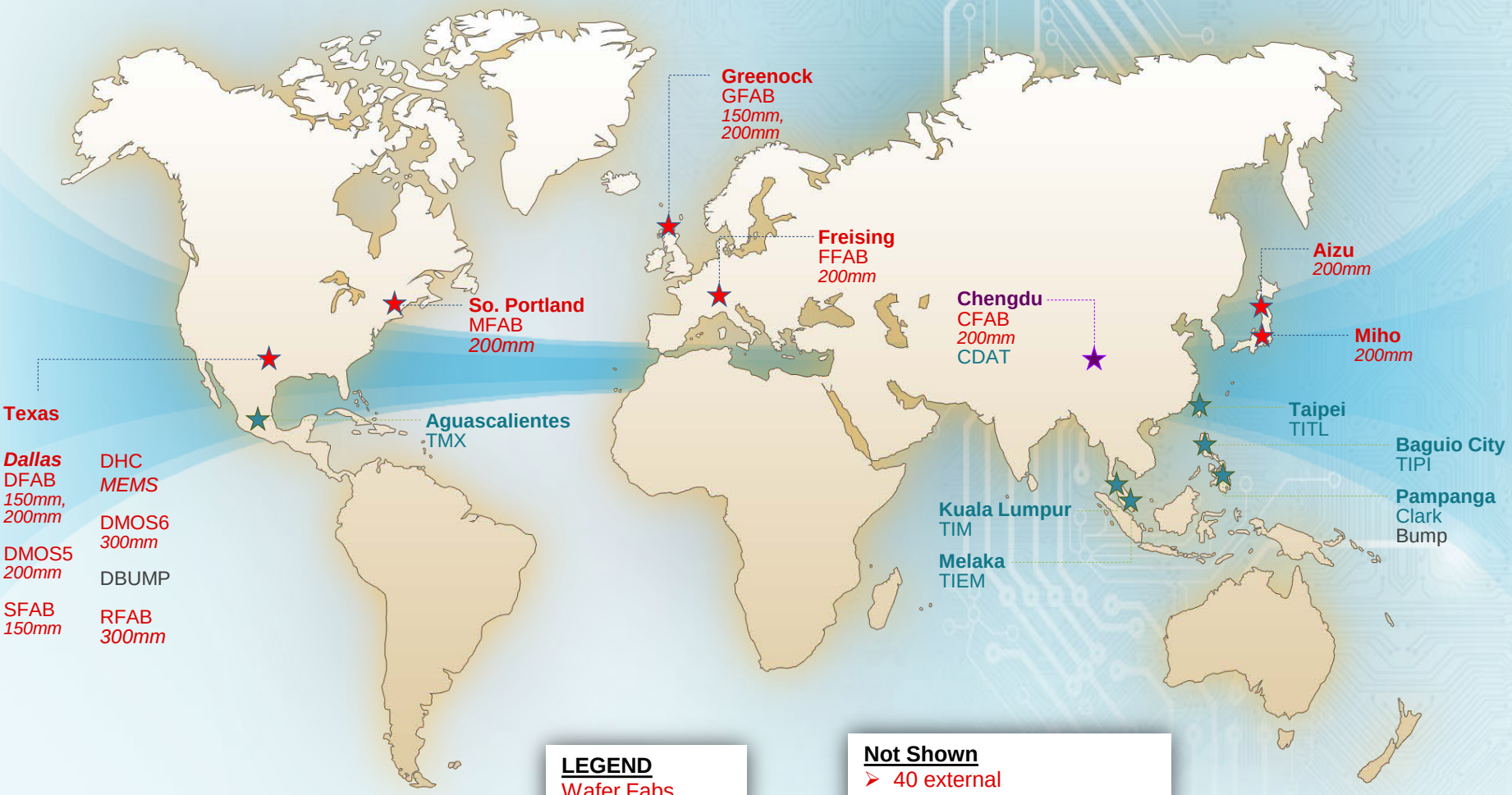
Challenges, Limitations, and Future in the Test Development Process

Dr. Friedrich Taenzler

Outline

- **TI Overview**
  - Sites
  - Products and markets
  - Technologies
- **Strategies**
  - Organization
  - Education
  - Standardization
- **Challenges**
  - Metal interfaces
  - Test parameter
  - Test for reliability
- **Examples**
  - High frequency
  - High voltage
  - Sensors
- **Future trends**
  - Market trends
  - Test trends

Worldwide manufacturing sites



LEGEND
Wafer Fabs
Assembly / Test
Bump

Not Shown
- 40 external
  - Fab
  - AT sites

Across US, Europe, and Asia

Analog, Embedded, and DLP Markets

Personal Electronics

- Wearables (non-medical)
- Mobile Phones
- PC/Notebooks
- Printers & other peripherals
- Storage
- Tablets
- TV/Set-top box/Audio

Communications Equipment

- Enterprise Switching
- Residential
- Telecom Infrastructure
- Wireless Infrastructure

Enterprise Systems

- Front Projection
- High-performance Computing
- Servers
- Thin Client

Industrial

- Appliances
- Building Automation
- Display & Digital Signage
- Electronic Point of Sale (EPOS)
- Factory Automation & Control
- Lighting
- Medical, Healthcare & Fitness
- Motor Drive & Control
- Grid Infrastructure
- Space, Avionics & Defense
- Test & Measurement
- Other Industrial

Automotive

- Advanced Driver Assistance Systems (ADAS)
- Body Electronics & Lighting
- Hybrid/Electric & Power Train Systems
- Infotainment & Cluster
- Passive Safety

Analog, Embedded, and DLP Wafer Processes

- More than 50 different wafer fab processes enable all of the different types of analog parts
- Maintains CMOS technologies in-house and in foundry for embedded and analog devices
- TI has developed and maintains four major analog process technology classes shown below

High-Speed BiCMOS

- SOI & Bulk
- SiGe NPN and PNP
- Precision thin film resistors and capacitors
- Low parasitic capacitance

High-Precision Analog CMOS

- Low power, low parasitic CMOS
- Low 1/f noise
- Precision thin film resistors and capacitors
- Non-volatile memories

High-Voltage BiCMOS

- Power LDMOS devices
- Broad and multi-voltage capability
- Thick metal technology
- SRAM and non-volatile memories

High-Density Analog CMOS

- Dense, low power CMOS
- Analog friendly CMOS
- Multi-Vt CMOS
- FRAM, SRAM & other low power memories

Strategies Organizational Structures

- Development teams are product centric
  - >70 development in independent Product Lines teams with diversified markets and needs
  - High variance in expertise level
- Centralized teams supporting development and drive standardization
  - ATE, Handler and probe teams
  - Data and Yield teams
  - Packaging Team
  - Sustaining Team
  - Process development
- Councils
  - Test and Design councils
  - ESD council
- Centralized tools and infrastructure
  - Expert support
  - Internal E2E rooms (forums)
- Roadmap development by centralized teams and councils

Strategies Education and Training

Classes

- Test techniques for mixed signal and digital test methods
- Dedicated classes on supporting Tools
- Lab and bench related classes
- Topic specific brown bag events
- Seminars on wide variety of topics
- International test conferences and workshops to track general and industry trends

Training on the Job

- Structured mentoring programs
- Rotation programs enabling deep insight to multiple functions
- Internal conferences to share knowledge across teams and functions
- Continuous lessons learned session
- Roadshows sharing newest developments and tools

University

- Direct and indirect (SRC) funding of projects in fab technologies and CADT
- Support or jointly developed University classes
- Providing class/lab material
- Consign equipment and ATE to support test education
- Textbook to share industrial view on test
- Liaisons to train students

Strategies Wafer vs. Package Test

Open question to be asked for every development project on share between probe and package test

- **Cost**
  - Throughput with short index time
  - Development cost and time
  - Cost of ownership
  - Cost benefit of early defect detection
  - Spatial data prediction to shorten test time e.g. to optimize trim time
- **Performance**
  - Reliability of contacts
  - Current capability
  - Signal integrity
  - Temperature capability and accuracy
- **Manufacturing**
  - MTBF significantly different
  - Temperature capability
  - Die traceability vs. die Id requirement for traceability
  - Post test data handling for outlier screen including next neighbor screen capability

Probe test coverage is preferable, only tests which could not be performed at probe should be executed at package level

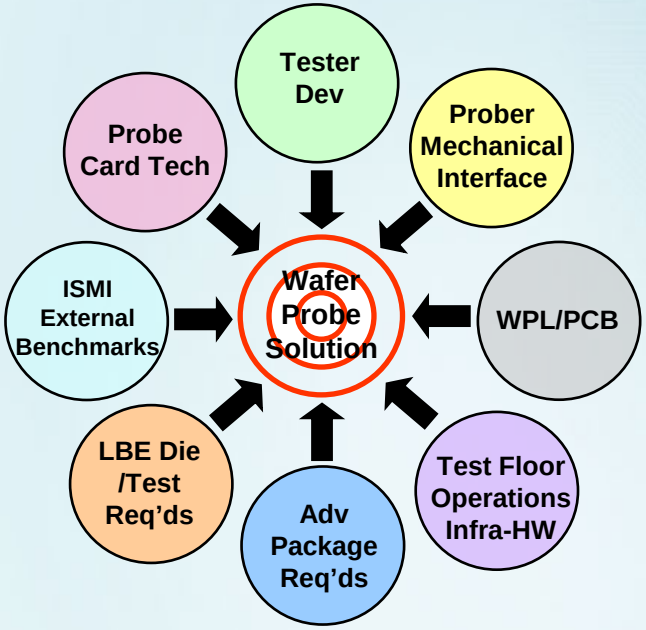
Strategies Standardization

Example Standardized DfP (Design for Probe) flow

- H/W standardization
  - Same interface for all handler and prober
  - Same mechanical interface for all ATE allowing to mate with any handler or prober
  - Standardized test sockets
- Pre-selected qualified probe technologies with defined use conditions (current, voltage, temp, frequency, metallic interface, cleaning media, …
- Database
  - Binning
  - Standardized Probe setups to all sites

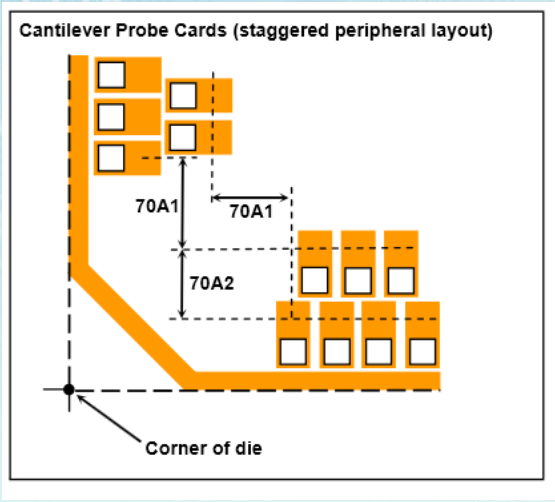
Strategies Design for Probe

DFP-Design For Probe is a **risk-review process** involving a cross functional team with the objective to align the probe solution to TI's **roadmap and best practices**.



Example

- Cantilever design rules for pad layout.
- Minimum spacing and pad size
- #of rows and location of pads
- Probe temperature



Benefits

- Optimize the probe card technology selection
- Streamline the RFQ to ensure best pricing!
- Maintain and optimize design rules for various silicon technologies and use conditions
- Help to provide robust solutions that can easily be transferred across various TI sites worldwide.

Strategies Validation vs Test

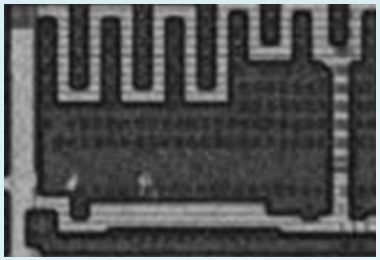
- Digital Test:
  - Clear divide between functional validation and production test
    - Structural rather than parametric Test
    - “Defect based” test to defect models
    - Known test coverage to defined fault model

- Mixed Signal Test:
  - Mostly ad-hoc DfT and test coverage definition
  - Parametric test mostly capable of good percentage of validation
  - In-depth validation of corner performance with variation of temp, ramp rates, sequences, … mainly with bench equipment

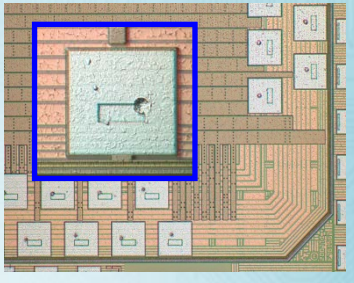
- Memory Test
  - Strategy between digital and mixed Signal test
  - Additional long term verification with process qualification
  - Mainly driven with ATE test and characterization

Challenges Metal Interfaces

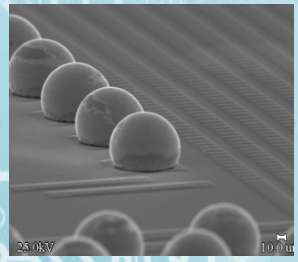
BOAC (NiPd) Pad



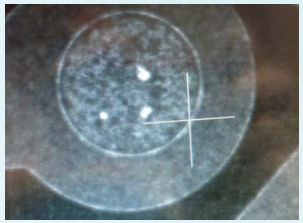
Al Pad

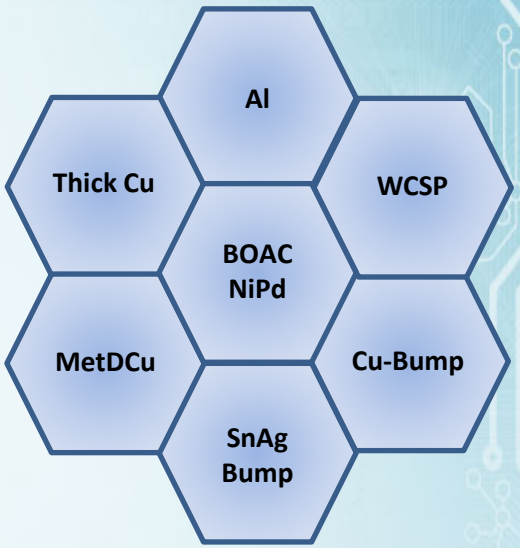


Spherical Bump

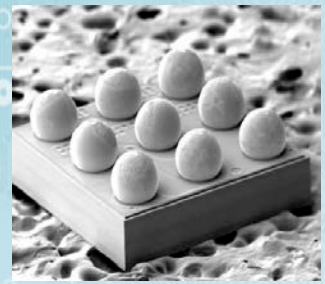


Cu Pad

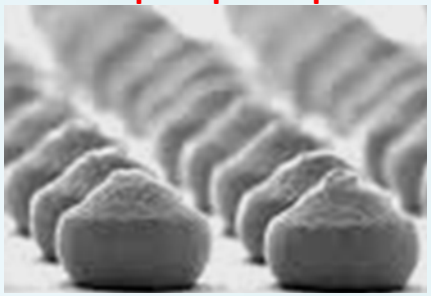




Wafer-Level Chip

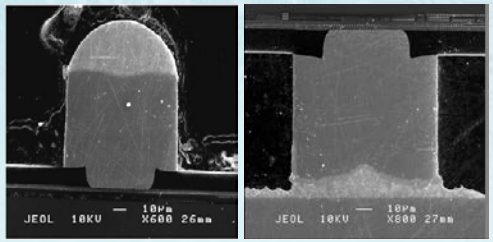


Flip Chip Bump



Mushroom Bump

Cu Post



Challenges Electrical Parameter

- **Voltages**
  - nV to kV covering noise to isolation
- **Currents**
  - pA (or fA) to Ampere covering ultra low power devices to high volume power devices (e.g. switcher, PMICs, …)
- **Frequencies**
  - All from DC to 100GHz now
  - Above 200GHz soon ???
- **Resistance & Impedance**
  - Low DUT input impedance requires low contact resistance for nominal DUT performance
  - All from lowest (few mΩ) to high impedance (several GΩ) inputs
  - For RF applications often defined input and output impedance for nominal DUT performance

Challenges Non-electrical Parameter

- **Non-electrical Parameter**
  - Temperature (absolute)
  - Humidity
  - Pressure (absolute and relative)
  - Light
  - Magnetics
  - Radiation
  - Acceleration
- **Future**
  - Bio/Chemical parameter

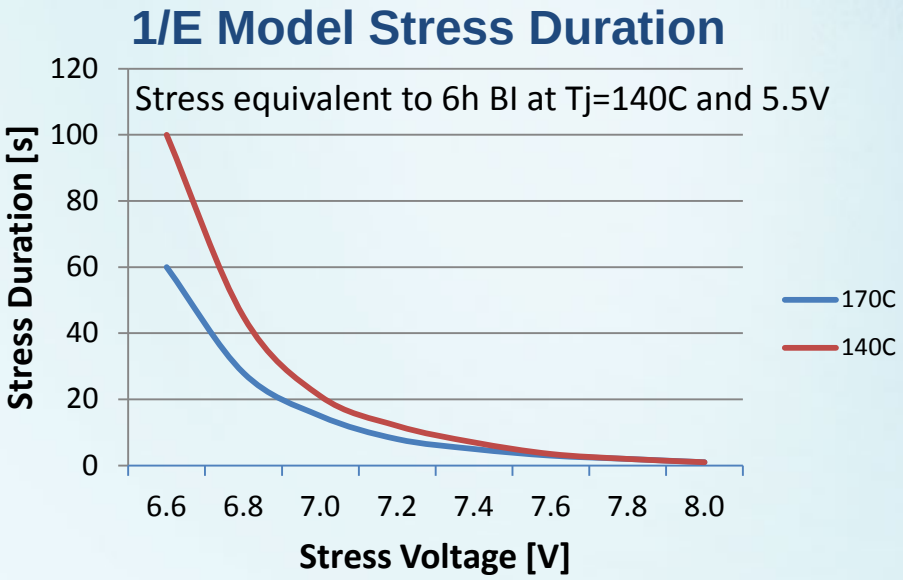
Challenges Temperature

- Single defect rates including temperature defect modes are reaching <<1‰ range and are highly lot dependent
- High end commercial and automotive devices require <1DPPM defect level
- A screen for temperature defects might need to be implemented
- Temperature accuracy at final test is often not sufficient
- Temperature accuracy at probe is superior
- Need interface (probe technology handling full temperature range, best with single probe card
- Temperature and humidity control of both sites of test board to avoid early device and component breakage

Challenges Test for Reliability

Probe level Burn-In (PBI)

- Elevated temperature with voltage and current accelerated stress to address TDDB
- Probe level Burn-In (PBI) has now been widely accepted as valid option as an replacement for package BI
- Part of the temperature acceleration is replaced by voltage and current acceleration
- Stress time is reduced from 3-6 hours to a couple of hundred msec



Critical to have high temperature probe capability to allow lower stress voltage below V_{BD}

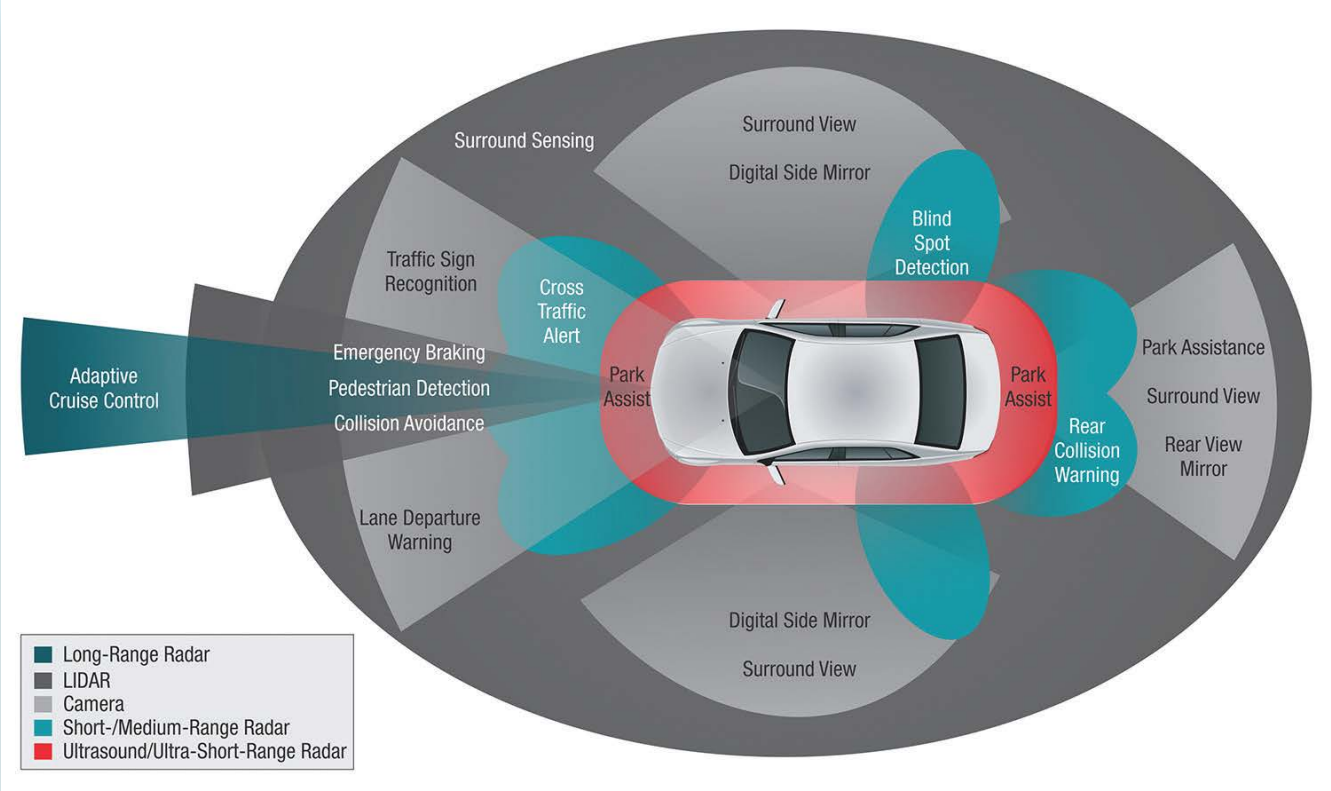
Challenges Other Factors

Other Impacting Facts:

- **Process**
  - Metal stack and intermetallic structure
  - Wafer contamination or oxidation (data retention bake?)
  - Planarity of bump
  - Multi-insertions and pad damage
- **Device dependent**
  - Pitch
  - Temperature including PBI
  - Frequency
  - Voltage
  - Current
- **Environment dependent**
  - Test environment (testing GSM devices next to cell tower)
  - Humidity
  - Temperature

Examples

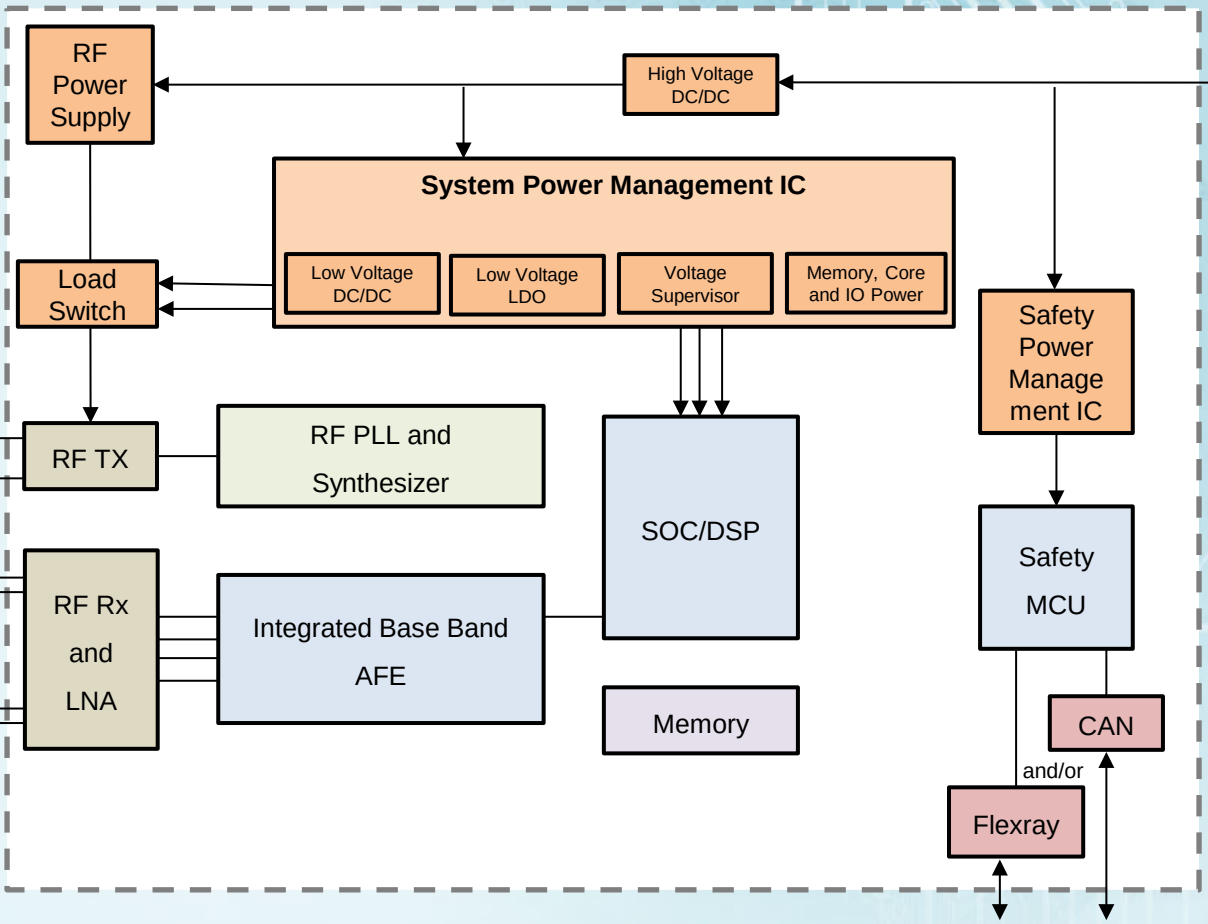
Examples High Frequency



	Freq. [GHz]	BW [GHz]	Modulation	Angle	Range	Resolution	Application
Short Range	24	7	Pulsed	70°	10m	<10cm	Side-Crash Parking
Mid Range	24	0.25	FMCW	30°-~60°	40m	~1m	Stop & Go
Long Range	77	1	FMCW	16°	150m	~1m	ACC

Examples High Frequency

Typical ADAS Long Range Radar Block Diagram



Critical TX Parameter

- Power
- Channel matching
- Noise
- Phase noise

Critical RX Parameter

- Noise Figure
- Channel matching
- IP1dB
- SFDR

Examples High Frequency

RF Performance for different technologies

	RFCMOS	SiGe	GaAs
Logic Integration Capabilities	High	Low	Very low
System on Chip Capabilities/ Roadmap	Excellent	Poor	Poor
Mainstream technology	Yes	No	No
BIST Capabilities	Excellent	Very Low	Very Low
Max Frequency	High	High	Very High
Power Output RF	Medium	High	Very High
Efficiency (Power Losses)	Medium	Medium	High
Logic Power Consumption	Very Low	High	n.a.
Junction Temperature	Medium	High	High
ADC Capabilities	Very high	Medium	n.a.
Temperature Dependency of parameters	Medium	Medium	Medium
1/f Noise	Medium	Low	High

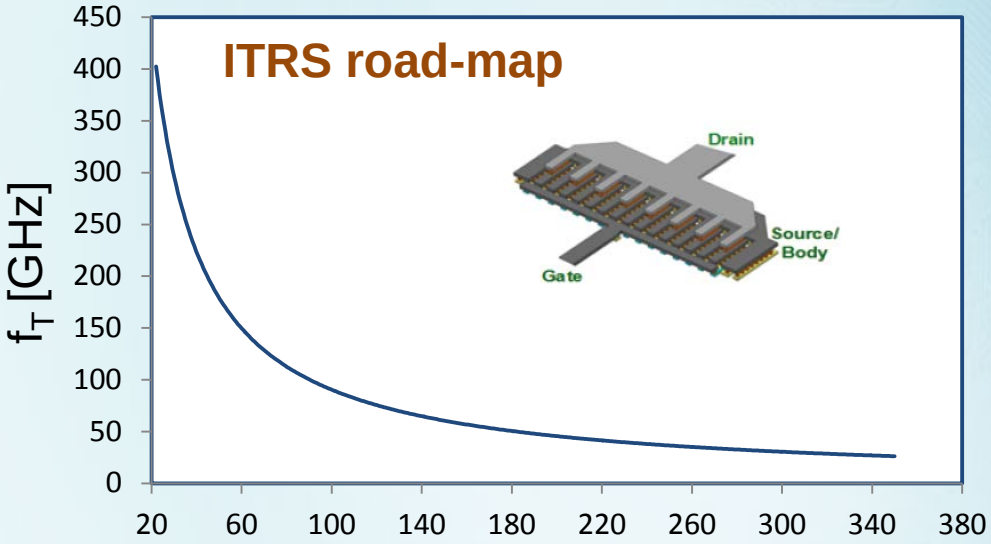
NXP Radar Technologies

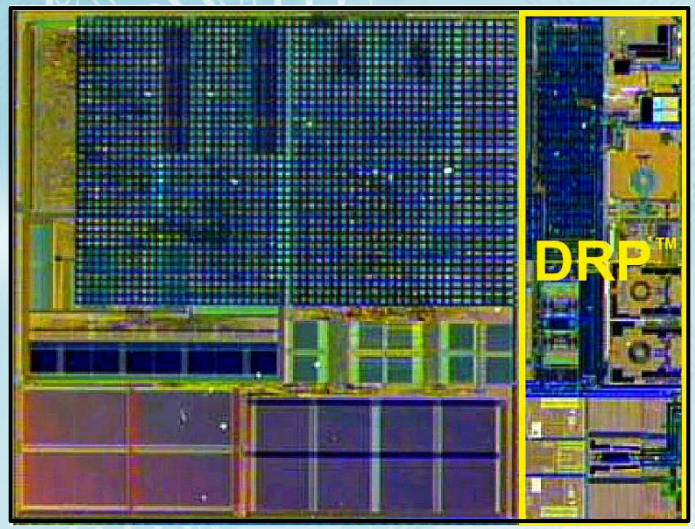
- **Existing:**
  - multi-chip SiGe radar
- **Transition to:**
  - highly integrated RF CMOS radar enabling complete SoC with built-in self-test (BIST) capabilities
  - RF CMOS reduces cost and allows technology scaling.

Examples High Frequency

f_T performance increases dramatically with technology scaling, broadening the horizon for RF CMOS applications into areas previously limited to III-V or SiGe solutions

RF CMOS f_T performance





DRP (Krenik et al)

Advanced technology nodes enable CMOS integration for THz applications e.g.

- 60 GHz for next generation Wi-Fi,
- 77 GHz CMOS long range radar for the automotive industry,
- 71-76 GHz and 81-86 GHz E-band backhaul

Examples High Frequency

Brief Snapshot

[1] **A Fully-Integrated 77-GHz FMCW Radar Transceiver in 65-nm CMOS Technology**
Jri Lee, Yi-An Li, Meng-Hsiung Hung, and Shih-Jou Huang; IEEE JOURNAL OF SOLID-STATE CIRCUITS, VOL. 45, NO. 12, DECEMBER 2010

[2] Y. Kawano *et al.*, "A 77 GHz transceiver in 90 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. (ISSCC) Dig. Tech. Papers*, Feb. 2009, pp. 310–311.

[3] D. Salle *et al.*, "A fully integrated 77 GHz FMCW radar transmitter using a fractional-N frequency synthesizer," in *Proc. Eur. Radar Conf. (EuRAD)*, Sept. 2009, pp. 149–152

[4] T. Mitomo *et al.*, "A 77 GHz 90 nm CMOS transceiver for FMCW radar applications," in *Symp. VLSI Circuits Dig. Tech. Papers*, Jun. 2009, pp. 246–247.

	2009 [2]	2009 [3]	2009 [4]	2010 [1]
Function	RF front-end only	PLL + RF front-end	Transmitter only	Fully-integrated
FMCW Generation	None	External DDFS	Fractional-N	Fractional-N
RMS Freq. Error w/edge points w/o edge points	 N/A N/A	 >1MHz N/A	 N/A <100kHz	 < 300kHz ~ 64kHz
Operating Freq.	73.5 ~ 77.1 GHz	78.1 ~ 78.8 GHz	76.8 ~ 77 GHz	75.6 ~ 76.3 GHz
Phase Noise (@ 1MHz Offset)	-86dBc/Hz	-85dBc/Hz	-74dBc/Hz	-85.33dBc/Hz
TX Output Power	3.3 ~ 6.3dBm	-2.8dBm	18dBm	13.7dBm
PA Power Gain	16dB	14dB (with DA)	N/A	13.7dB
RX Conv. Gain	0.5 ~ 3.5dB	23.1 dB	N/A	13.7dB
LNA Noise Figure	6.8dB	15.6dB	N/A	7.4dB
Max. Measured Distance	N/A	8m	N/A	106m
Power Consumption	920mW	520mW	N/A	243mW
Chip Area	2.4 x 1.2mm^2	3.5 x 1.95mm^2	N/A	0.95 x 1.1mm^2
Technology	90nm CMOS	90nm CMOS	0.18umSiGe	65nm CMOS

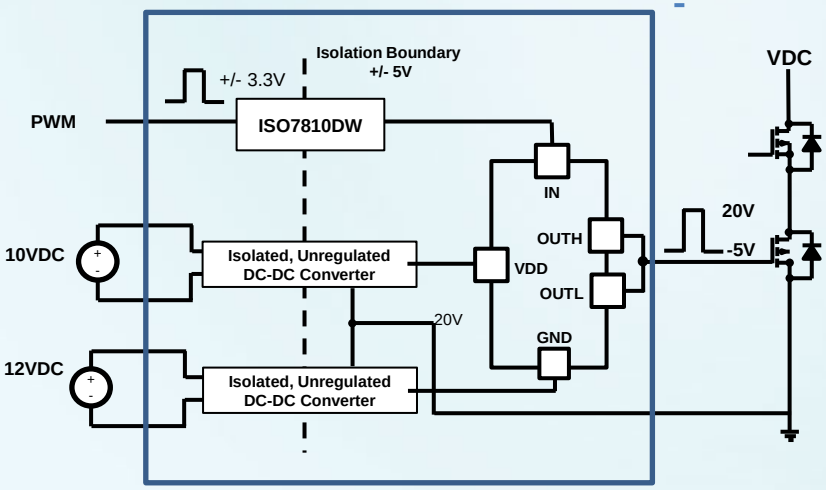
Examples High Frequency

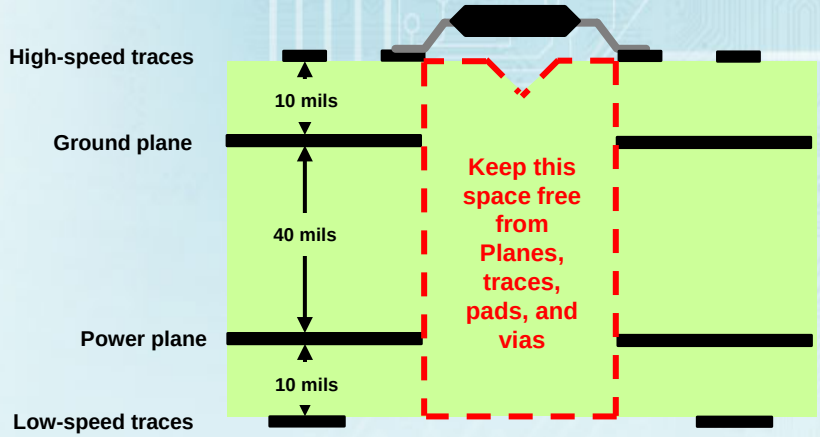
Test Challenge	Risk
Production testing @81Ghz requires new ATE with source and measure capability	No such ATE solution exists. Will require new development by partnering with external vendors
New parameters for test have tight specs - TX/RX Phase Drift, Phase Shift, Phase mis-match, Return Loss	These new RF parameters have no prior understanding. New frequency range (81Ghz) resets many of the past lessons learned.
No proven test interface at package and wafer level	• Test Socket with Pogo pin is not an option for 81Ghz test. Socket solution doesn't exist today • Only path to test might be a RF Probe technology • However – for BGA ball height tolerance some probe technologies might not be feasible
No proven ATE board designs with components and routing of 81GHz	• Waveguides are rigid, heavy, and expensive. They will eat up lot of board real-estate limiting multi-site capability • These waveguides will either require to be built into ATE or a separate box for proper interface to ATE and wafer (DUT).
Risk to RF Test removal is high due to 0 DPPM requirements.	ASIL-B requires guaranteeing <1 DPPM • Straight statistical math says requiring 2.3Mu defect free devices for proper confidence level.

Examples High Voltage Devices

Examples Isolation Devices

Solar Centralized/String Inverter Block Diagram





Examples Isolation Devices

Isolation products with test requirement of 8kV

High voltage can

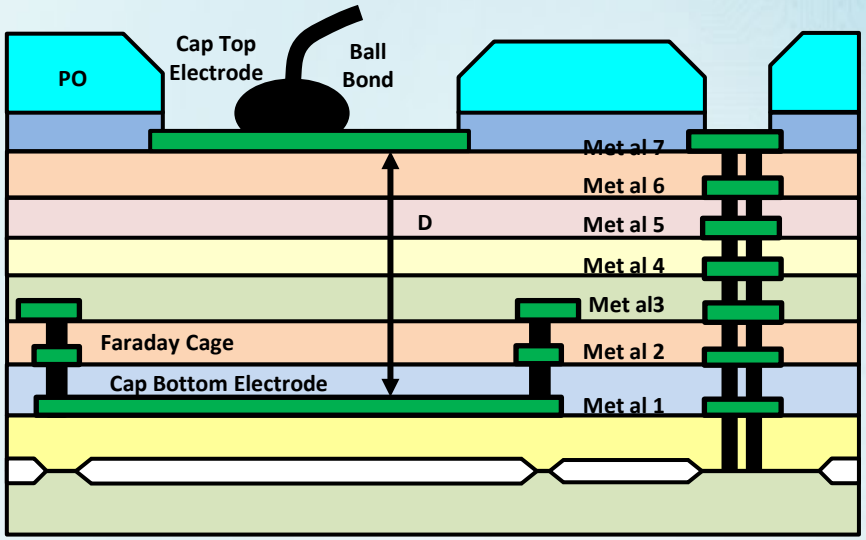
- Generate In-situ voltage break down
- Cause Air voltage breakdown
- Require special packaging material
- Layout rules
- Can have own defect modes not observable with low voltage tests

Probe card

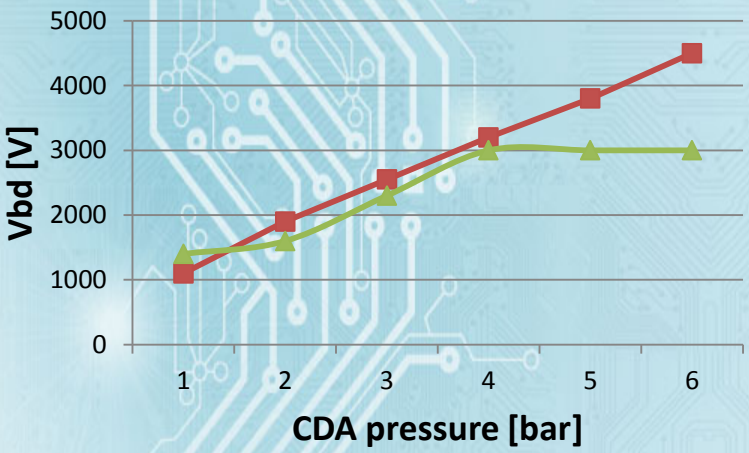
Wafer

Examples Isolation Devices

Test Structure to evaluate Vbd



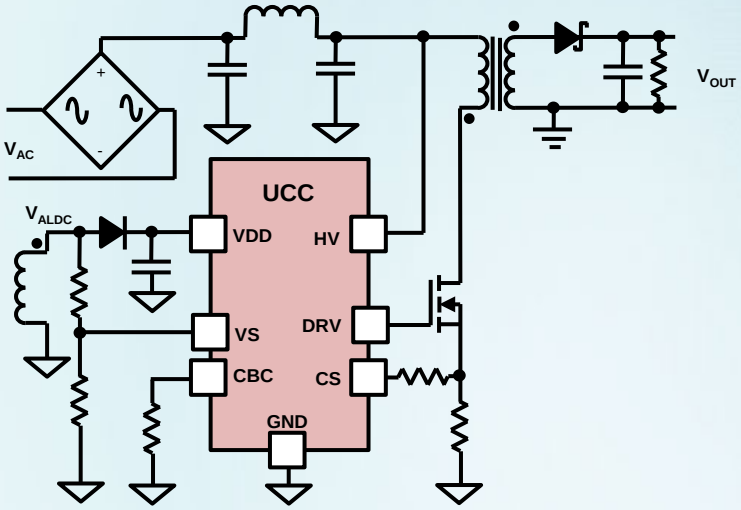
Paschen Law vs Results



Test Challenge	Risk
Test with voltages >5kV	Break down of • Air • Device • Test H/W
Usage of Paschen Law	Implementation of over-pressure into production test H/W
Safety concern	• Handle of voltages >>50V in an production environment • Service of equipment and safety features

Examples 700-V Flyback Switcher

The UCC28xxx family of flyback power supply controllers provides isolated-output Constant-Voltage and Constant-Current output regulation for line voltage applications



Specifications

VHV Start-up pin voltage, HV 700V

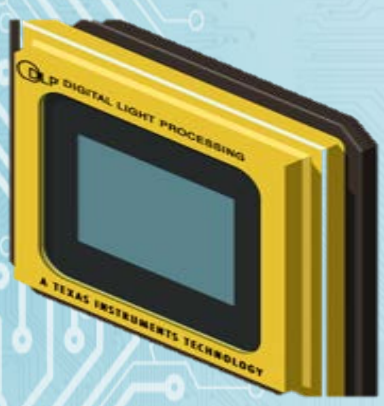
Test Challenge	Risk
Test of HV breakdown voltage Vbd in production	Low number of HV (>~50V) limits to low multisite Long charge times of parasitic capacitor
Test of HV leakage	Board leakage might exceed DUT leakage current
HV have own defect modes	Need to test break down voltage rather than correlation to other parameter
Safety concern	• Handle of voltages >>50V in an production environment • Service of equipment and safety features

Examples Digital Light Processing (DLP)

Digital Micromirror Device

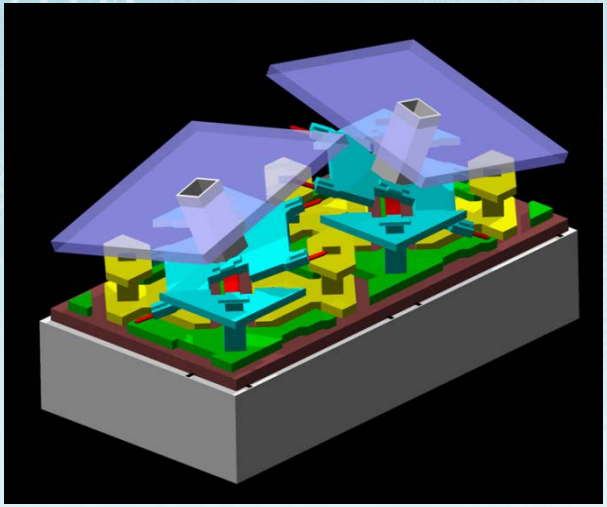
- Up to >2M mirrors integrated in one IC
- Lifetime up to 100,000 hours
- Al as mechanical elements
- Process: low temp sputter deposition with plasma etch in standard IC fabrication process
- 3.3V CMOS technology
- Optical hermetic welded lid

Hermetic welded DLP

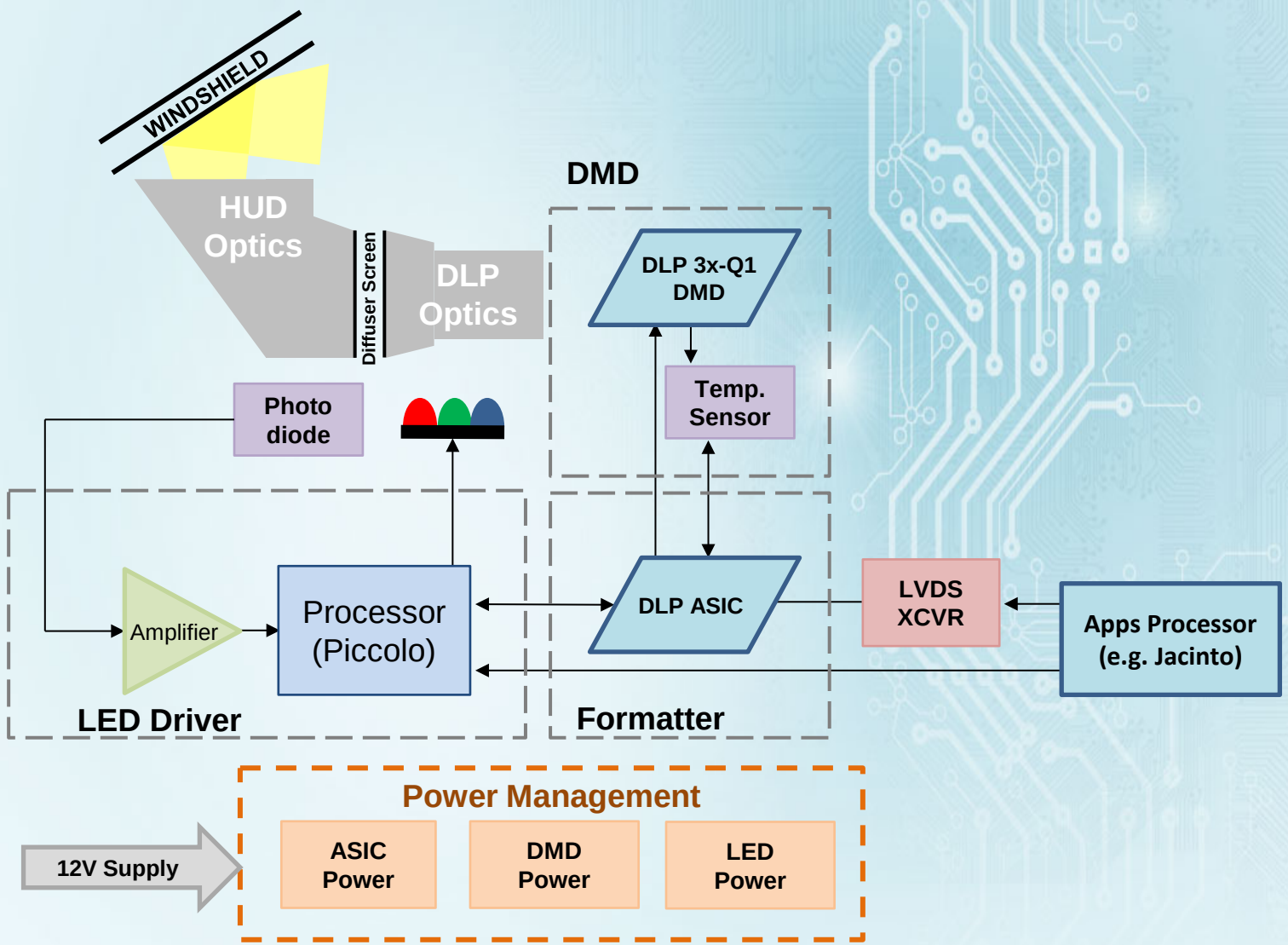


Heads-Up Display (HUD)

Micromirror

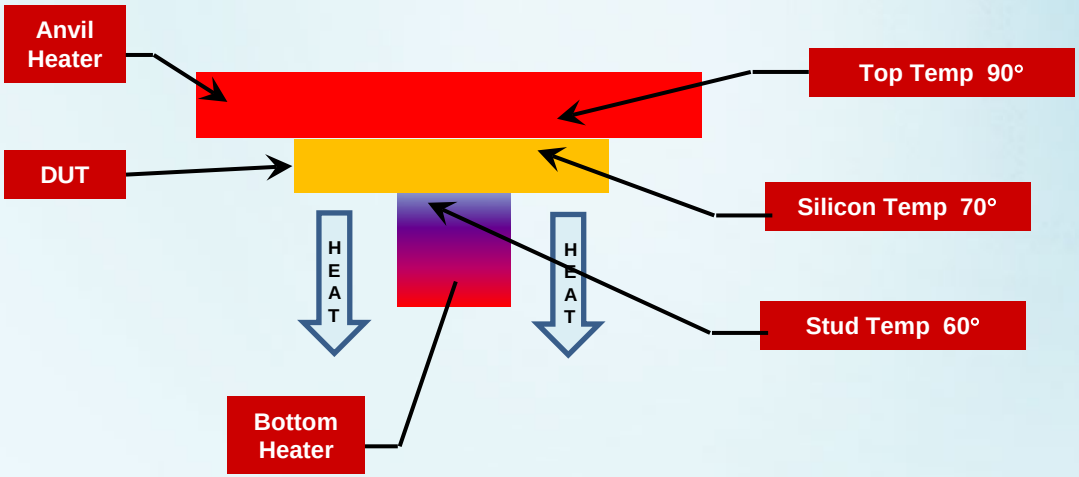


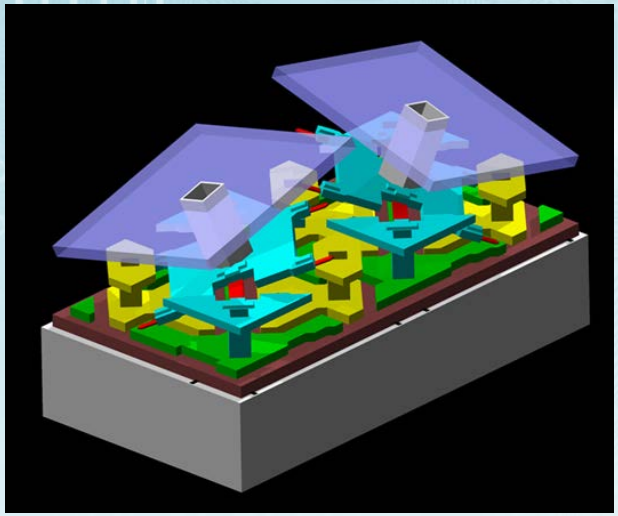
Examples DLP



Examples DLP

Test Challenge	Risk
Test of optical defects at high temp	Heat DMD device using physical contact heaters No chamber based heating due to tester space
Long test time of optical performance	Anvil (top) only heating is not sufficient to maintain the temperature; showed a 30degC gradient to bottom of DMD
Automotive application require high temperature test in production	hot testing had to be implemented on existing MirrorMax tester platform
Mirage Effect	Mirage Effect: "A mirage is a naturally occurring optical phenomenon in which light rays are bent to produce a displaced image of distant objects"

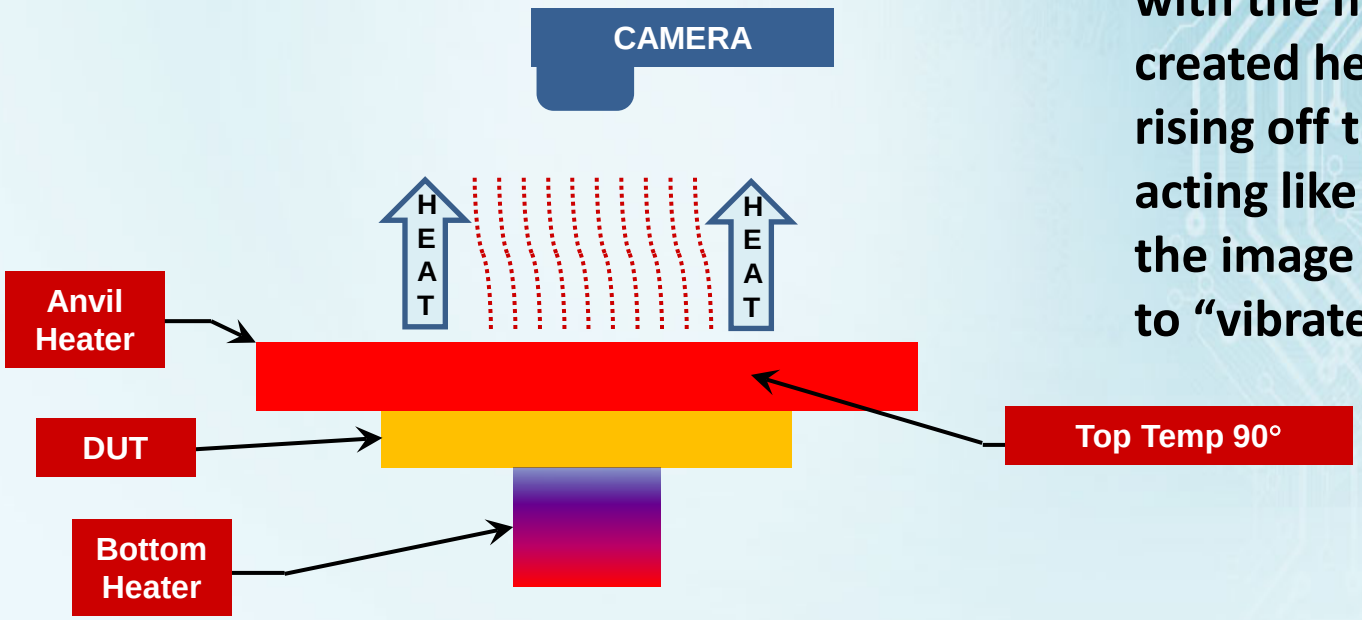




Examples DLP

Mirage Effect: “A mirage is a naturally occurring optical phenomenon in which light rays are bent to produce a displaced image of distant objects”.

The confined space combined with the high temperature created heated air columns rising off the anvil which is acting like micro-lens causing the image of the DMD mirrors to “vibrate”.



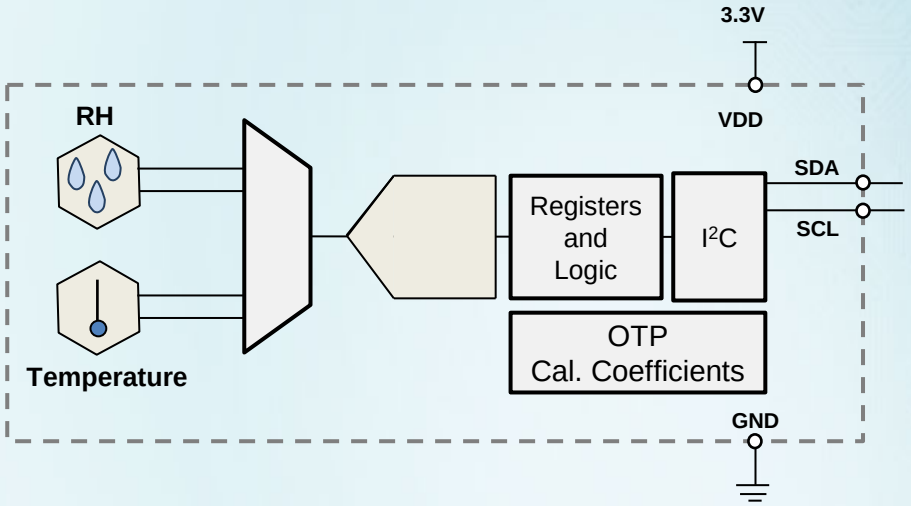
Examples Sensors

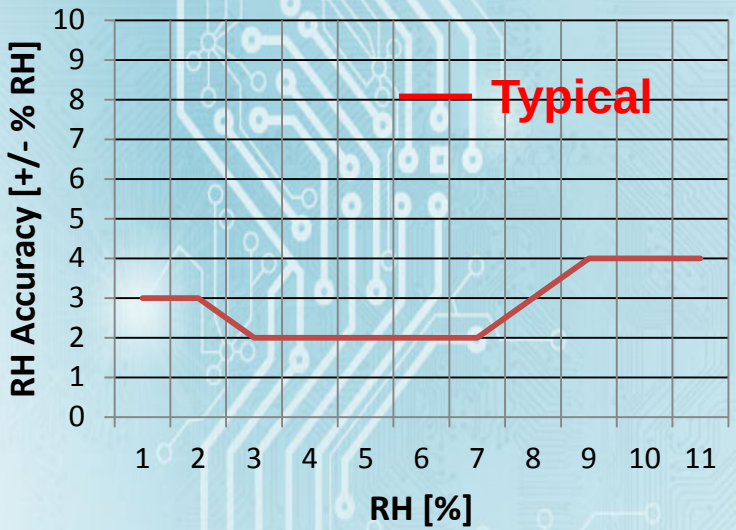
Sensors:

- Biosensing
- Fluid and gas
- Light
- Proximity
- Current/power
- Humidity
- Position/motion
- Temperature
- Flow
- Level
- Pressure
- Magnetic field

Examples Humidity Sensor

Humidity sensors determine the amount of water vapor / moisture in the air. Because relative humidity is a function of temperature, humidity sensors also usually include integrated temperature sensors





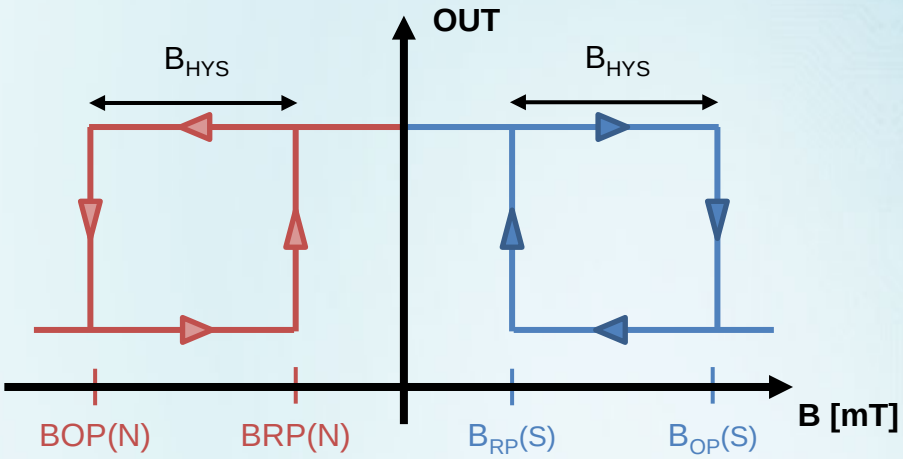
HDC1080

Applications

- HVAC
- Smart Thermostats and Room Monitors
- White Goods
- Printers
- Handheld Meters
- Medical Devices
- Wireless Sensor

Examples Magnetic Sensor

Magnetic sensor – aka Hall sensor



A magnetic field of either polarity causes the output to pull low (operate point, BOP), and a weaker magnetic field causes the output to release (release point, BRP)

Test Challenge	Risk
Magnetic signal activation	Many ferromagnetic parts in handler will deform magnetic field Accurate homogeneous field only with two Helmholtz coils Internal generation of magnetic field will require significant current causing thermal shifts
Defect mode test	Direct test of hall element with special test mode assumes specific defect model

Future Trends

Outline

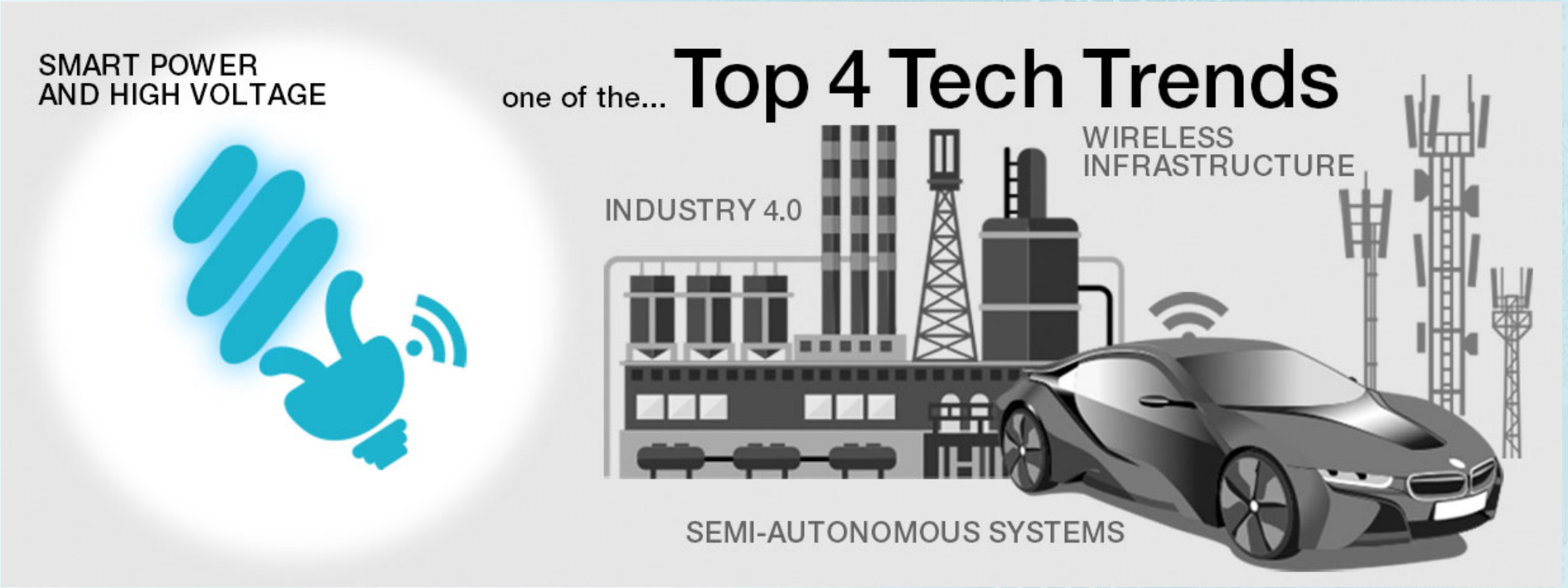
- Trends in Embedded and Analog Markets (personal view)
- Test techniques trends
  - DfT to reduce ATE and Interface constraints
  - Analog BIST and DfT to avoid costly ATE instruments or costly test interface
  - Observer or model based testing

Future Trends

From Past to Future

- Some examples:
  - Portable driven applications grew significant due to evolving battery technologies together with power management devices (e.g. 7805 to DCDC switcher)
    - Linear test sufficient for 7805 but at current and voltage requirement for DCDC switcher
  - WLAN/mobile phone grew to commodity due to market driven and technology enabled developments; from multiple devices to single chip SOC.
    - RF test had to be implemented to digital test environment and for highest volume.
    - Similarity to sub-THz application (auto Radar, high data rate communication) today and near future

Future Top 4 Tech Trends



- Smart power and High Voltage
- Semi-Autonomous Systems
- Industry 4.0
- Wireless Infrastructure

Future Top 4 Tech Trends

Smart power and high voltage:

- Trends for higher power efficiency in power management are evident:
  - Server farms are constantly growing to accommodate new cloud services and social networks efficiency resulting in criticality of power management
  - Smaller and faster chargers for portable devices are in demand
- Smart power solutions are being deployed in many applications
  - LED array controllers in automotive
  - High performance battery management for high power drones and e-bikes.
  - extremely low standby and sleep mode current for wearable
- The market for alternative energy
  - solar and electric/hybrid vehicles are experiencing healthy growth.
  - Semiconductor content in higher voltage applications, particularly 600-1200V is growing
- Long awaited III-V materials such as GaN and SiC will enables new applications

Future Top 4 Tech Trends

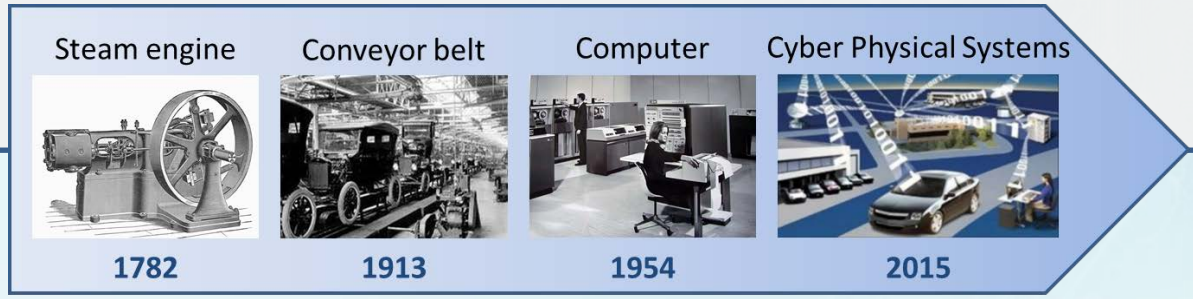
Semi-Autonomous Systems

- Electronic content continues to be the differentiating feature of new vehicles
- Advanced Driver Assistance Systems (ADAS) in semi-autonomous vehicles are going beyond beta tests and luxury vehicles into the mainstream
- Extensive use of cameras (up to 10 per vehicle)
- Integrated radar, sonar and eventually Lidar, which demand for higher-speed interfaces and hierarchical signal processing
- These technologies have enabled features such as collision avoidance, lane detection and smooth hovering at affordable prices

Future Top 4 Tech Trends

Industry 4.0:

- Key enabling technologies to transition to a smart manufacturing and inventory management are
  - low-power connectivity
  - embedded processing and embedded sensing
- Key features are already available or in development
  - low power, intelligent networked sensing solutions.
  - security and reliability concerns needs to be solved
- Multi-mode sensing solutions, such as humidity, temperature and pressure sensing will become the industry standard.
- Integrated ultrasonic and millimeter wave sensing solutions can offer new multimodal functionalities in flow metering, diagnostic and many other industrial applications.



Future Top 4 Tech Trends

Communication Infrastructure:

- Access to
  - Multimedia
  - social networking
  - e-commerce and other data-intensive applications

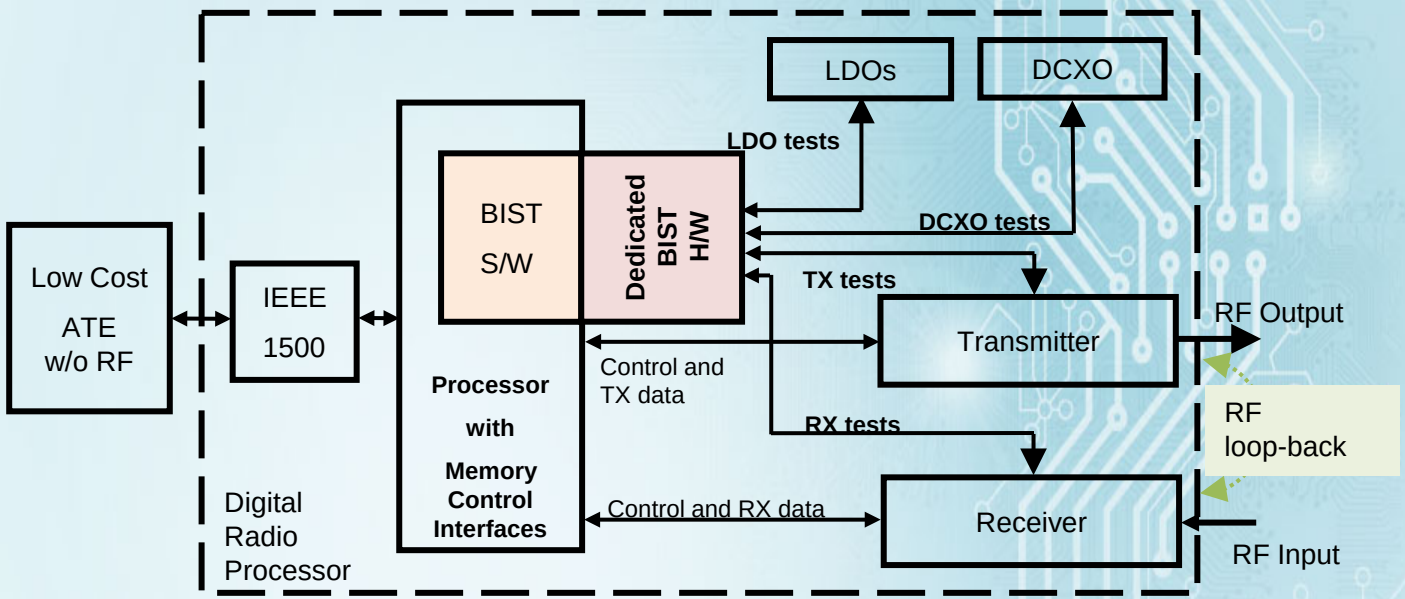
  drives the growing demand for higher wireless data rates.
- Urban peak data density in many major cities around the world is rising.
- Despite LTE deployment, there are some peak data limitations at the hot spots
- Small cells have been developed to improve network capacity but have not ramped up as expected due to evolving business models

Future Test Trends

- **Defect testing rather than testing for parameter**
  - Common in digital designs with a series of standardized tests like ATPG, Delay Fault Test, etc.
  - In its infancy for analog test
  - Lack of fault models for analog circuits
- **BIST to reduce ATE and Interface requirements**
  - RF BIST with
    - Digital implementation of analog functions e.g. ADPLL
    - Internal sensors enable BIST techniques
- **Model and Observer based test avoiding specialized test equipment, interfaces, or optimize test times and cost**
  - ADC test
  - RF Transceiver

Examples RF-BIST testing

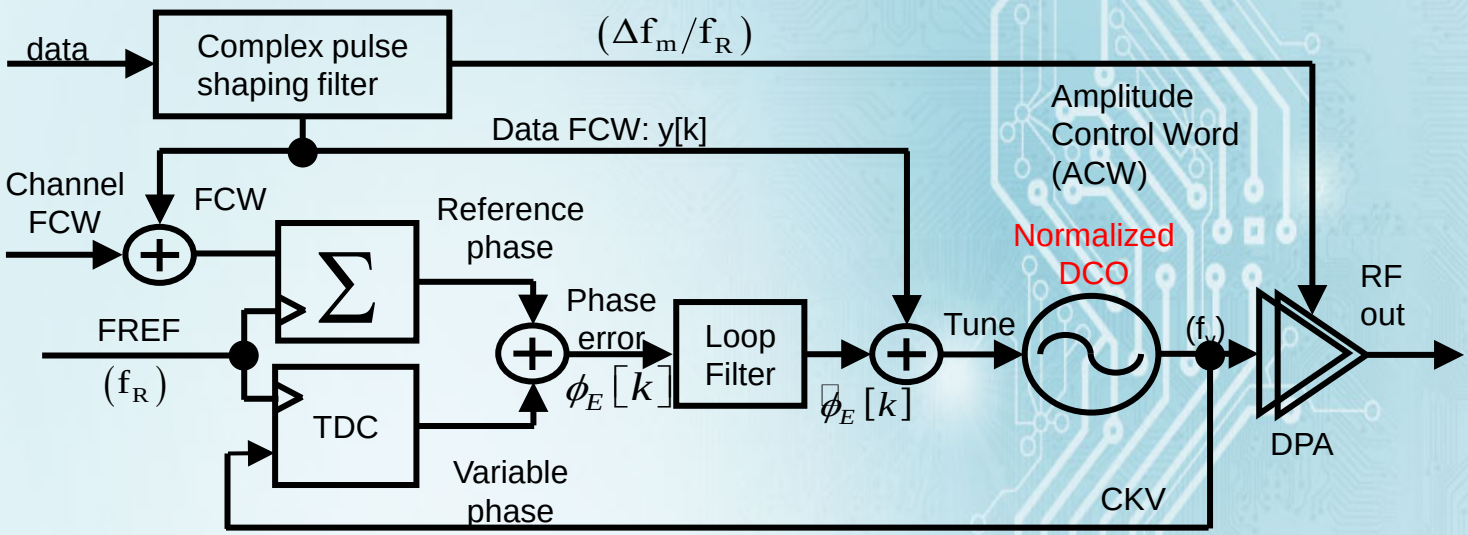
RF BIST - On Radio Build In Test (ORBIT)



- Developed and integrated from conceptual design start
- BIST takes advantage of the built in processor used for normal operation
- With additional hardware modules internal tests of the receiver, transmitter, LDOs and DCXO can be performed utilizing the software module
- Results can be extracted off-chip via the IEEE 1500 test bus with a low cost ATE
- With the high integration of the BIST structure into the SoC, tests can be performed at probe, final production test and at any convenient time in the field

Examples ADPLL-testing

All-Digital-PLL (ADPLL)

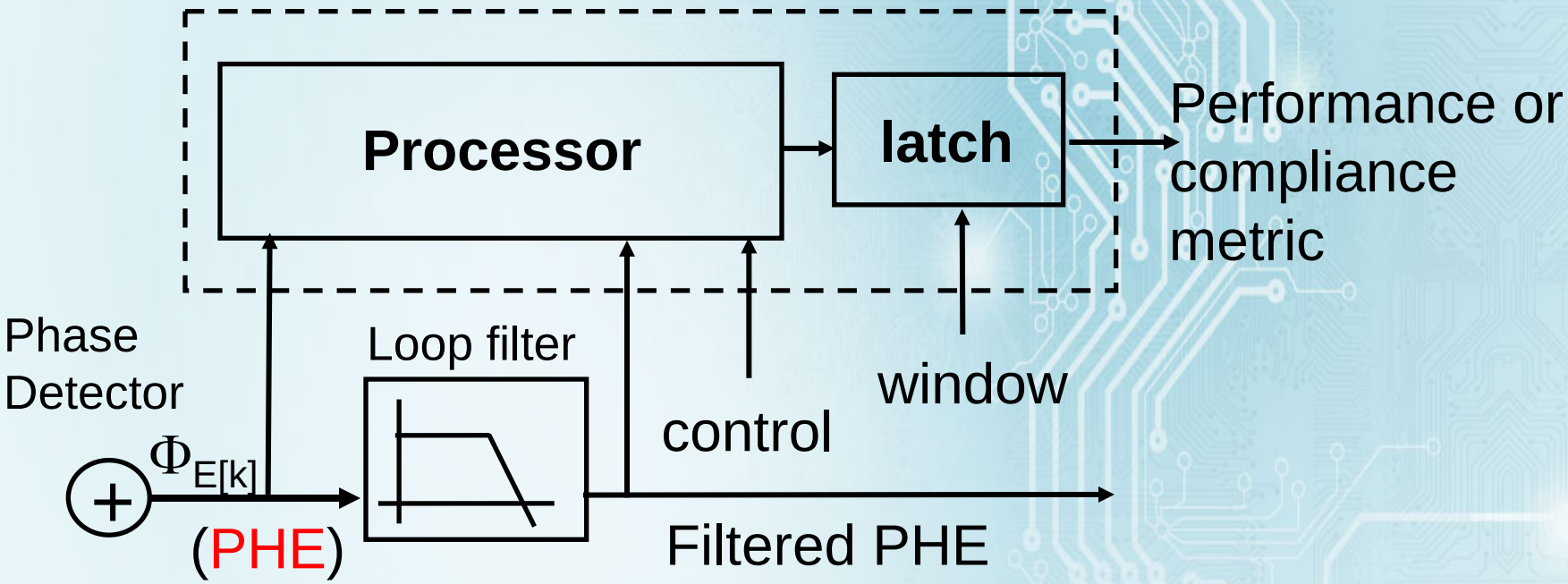


- ADPLL operates in a digitally synchronous fixed-point phase domain.
- Since the implementation of the ADPLL is by definition digital, the hooks for BIST are digital as well and are designed in the same VHDL design environment.
- The BIST structure targets two different entities of analog nature:
  - oscillator noise, which is not only useful for detecting fabrication defects that can results in a degraded noise performance DCO
  - test of the frequency tuning elements in the DCO

RF Built-in Self Test of a Wireless Transmitter; Robert Bogdan Staszewski, Imran Bashir, and Oren Eliezer; IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS—II: EXPRESS BRIEFS, VOL. 54, NO. 2, FEBRUARY 2007

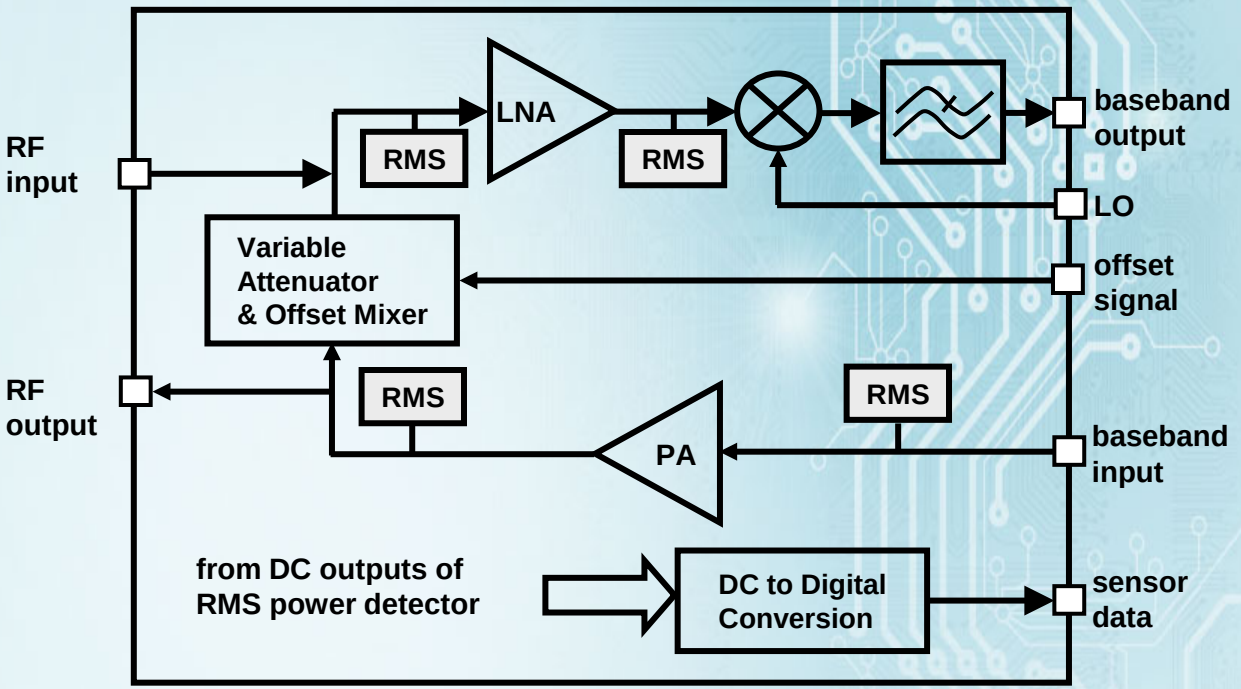
Examples ADPLL-testing

Analysis of ADPLL's Digital Phase Error



- properties of RF output strongly correlated with the loop's phase-error signal (at phase detector output)
- the phase error "PHE" is a multi-bit digital signal, which is read and analyzed digitally (hardware/software)

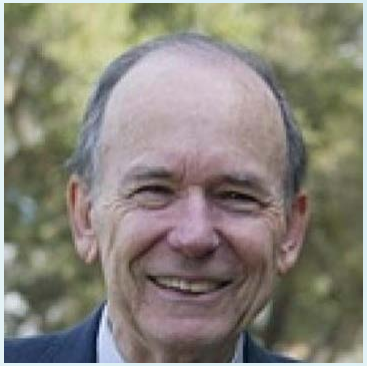
Examples Integrated Power Sensors



Integration of internal sensors and ADC can

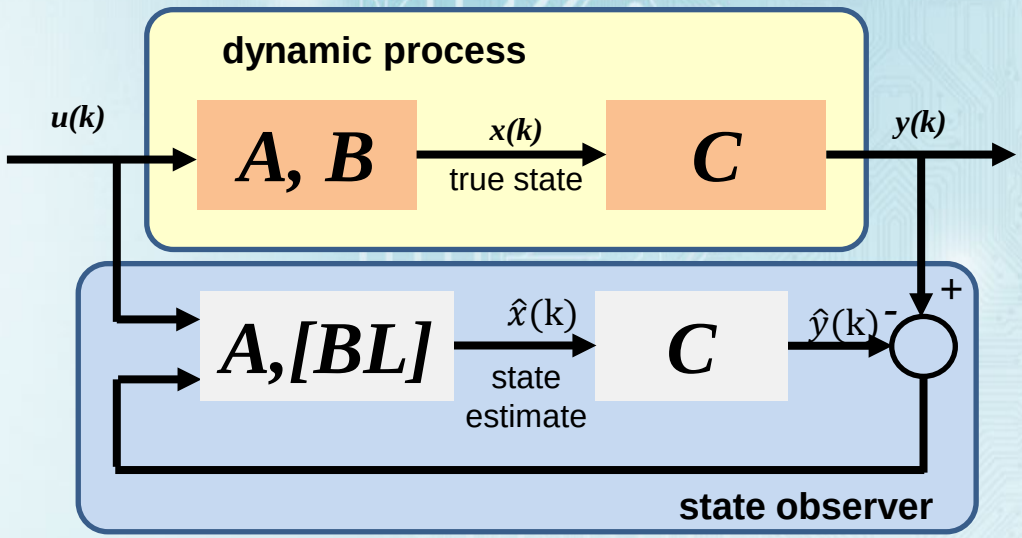
- Reduce the constrains of a high performing ATE and Interface (probe or socket)
- Can be used for internal calibration during usage to avoid early EOL
- Build in autonomous BIST to reduce test cost

Examples Model or Observer based test



David Gilbert **Luenberger** (born 1937) is a professor in the department of Management Science and Engineering at Stanford University.
In **1963** his dissertation Luenberger introduced new methods for construction of state observers which are named after him Luenberger observer.

In **control theory**, a state or Luenberger observer is a system that provides an **estimate** of the internal state of a given real system, from measurements of the input and output of the real system. It is typically implemented as a computer model



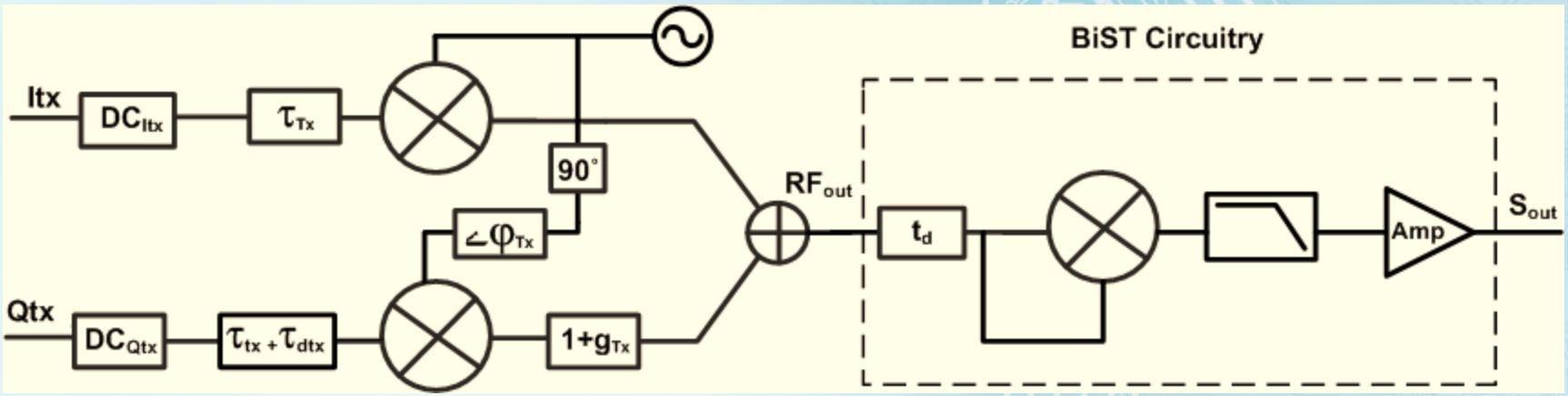
Examples Model or Observer based test

- If excited with a **specially designed stimulus signal** and the measurement of internal and external signals, the device performance can be determined using the **model**
- Using the observer functions, test signals can be designed to target multiple parameters
- Two approaches are prevalent for the modeling of the system
  - Statistical modeling or training: learning the behavior by observing the input-output signals of a set of similar sample devices
  - Analytical modeling: deriving the necessary mathematical expressions as a multidimensional function between an input and an output or internal signal

Examples Model or Observer based test

System Model

RF Transmitter and BIST System level block diagram including modeled impairments



Parameters		Parameters	
Gain mismatch	g_{tx}	**Self mixing delay**	t_d
Phase Mismatch	ϕ_{tx}	**LO frequency**	ω_c
TX DC offsets	DC_{Itx},DC_{Qtx}	**Path gain**	**G**
Baseband time skew	T_{dtx}	**Self mixing attenuation**	**K**
		Baseband Delay	t_{tx}

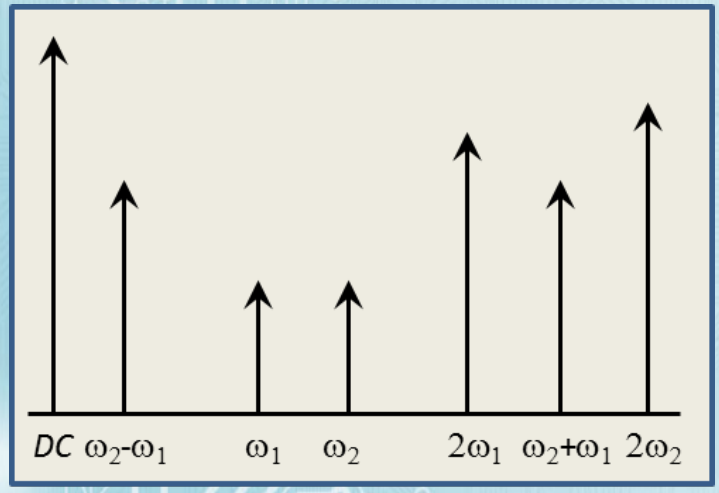
- Only amplitude information is used to determine target parameters, which can be easily obtained using FFT at the desired frequency locations.

Examples Model or Observer based test

- A special test signal is designed to separate out the effect of each impairment parameters:

$$I(t) = \cos(\omega_1 t) \qquad Q(t) = \cos(\omega_2 t)$$

- If the frequency of the two signals are distinct then the information will be separated out to DC, ω1, ω2, 2ω1, 2ω2, ω1-ω2 , ω1-ω2 as it is shown in the figure.



- Signal amplitude in different frequencies:

$$A_{DC} = \frac{1}{2}\left(\frac{G}{K}\right)^2 \left(\frac{1}{2} + \frac{1}{2}(1+g_{tx})^2 + DC_{Itx}{}^2 + (1+g_{tx})^2 DC^2{}_{Qtx}\right) + \left(\frac{G}{K}\right)^2 (1+g_{tx}) DC_{Itx} DC_{Qtx} \sin(\varphi_{tx})$$

$$A_{\omega 1} = \left(\frac{G}{K}\right)^2 DC_{Itx} + \left(\frac{G}{K}\right)^2 (1+g_{tx}) DC_{Qtx} \sin(\varphi_{tx})$$

$$A_{\omega 2} = \left(\frac{G}{K}\right)^2 (1+g_{tx}) DC_{Itx} \sin(\varphi_{tx}) + \left(\frac{G}{K}\right)^2 (1+g_{tx})^2 DC_{Qtx}$$

$$A_{2\omega 1} = \frac{1}{4}\left(\frac{G}{K}\right)^2$$

$$A_{2\omega 2} = \frac{1}{4}\left(\frac{G}{K}\right)^2 (1+g_{tx})^2$$

$$A_{\omega 1+\omega 2} = \frac{1}{2}\left(\frac{G}{K}\right)^2 (1+g_{tx}) \sin(\varphi_{tx})$$

$$A_{\omega 1-\omega 2} = \frac{1}{2}\left(\frac{G}{K}\right)^2 (1+g_{tx}) \sin(\varphi_{tx})$$

Examples Model or Observer based test

- There are 7 equations, but there are 5 usable linearly independent equations and 5 unknowns as:
  - $2\omega_1$ and $2\omega_2$ Have the same amplitude.
  - DC terms is not usable, as the blocks offset will be added to DC term and the LO leakage will self mix with itself and show up on DC term.

Impairment Calculation Steps:

- **Step1 - Path Gain:**

$$\left(\frac{G}{K}\right) = \sqrt{4 \times A_{2\omega 1}}$$

- **Step2 – Gain imbalance:**

$$g_{tx} = \sqrt{\frac{A_{2\omega 2}}{\frac{1}{4}\left(\frac{G}{K}\right)^2}} - 1$$

- **Step3 – TX Phase Mismatch**

$$\varphi_{tx} = \sin^{-1}\left(\frac{A_{\omega 1-\omega 2}}{\frac{1}{2}\left(\frac{G}{K}\right)^2 (1+g_{tx})}\right)$$

- **Step4 – DC offset Voltages:**

$$DC_{Itx} = \frac{A_{\omega 1}(1+g_{tx}) - A_{\omega 2}\sin(\varphi_{tx})}{\left(\frac{G}{K}\right)^2 (1+g_{tx})\cos^2(\varphi_{tx})}$$

$$DC_{Qtx} = \frac{A_{\omega 2} - A_{\omega 1}(1+g_{tx})\sin(\varphi_{tx})}{\left(\frac{G}{K}\right)^2 (1+g_{tx})^2\cos^2(\varphi_{tx})}$$

Sule Ozev, Arizona State University

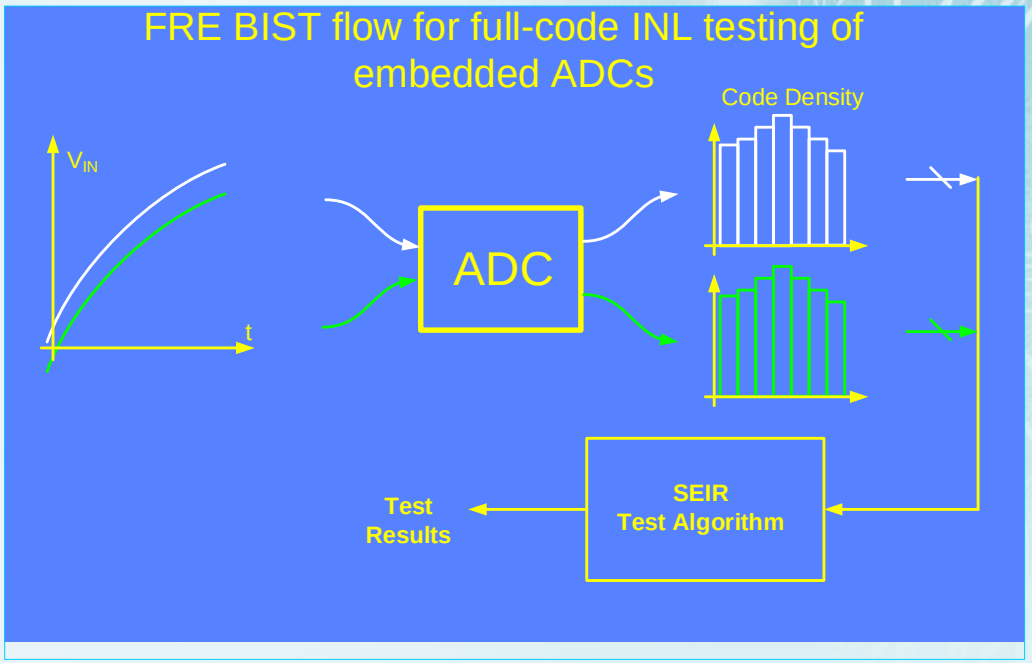
Examples Model or Observer based test

A New Method for Testing Spectral Performance of ADC from INL (Degang Chen, Randy Geiger, Iowa State University)

- A method of testing ADCs that does not require precise signal generators
- Based upon using unknown modestly nonlinear *Functionally Related Excitations* (FRE) that can be generated with very small and simple circuits
- Testing is accomplished by using system identification and signal processing concepts from digital outputs obtained from the FRE
- Area overhead for system identification and signal processing circuits are modest but if on-board DSP is available, requires little digital support circuitry
- FRE testing technique validated on 16-bit SAR ADC but can be practically used for linearity testing of lower resolution ADCs
- **Method can be practically adapted to BIST solution**

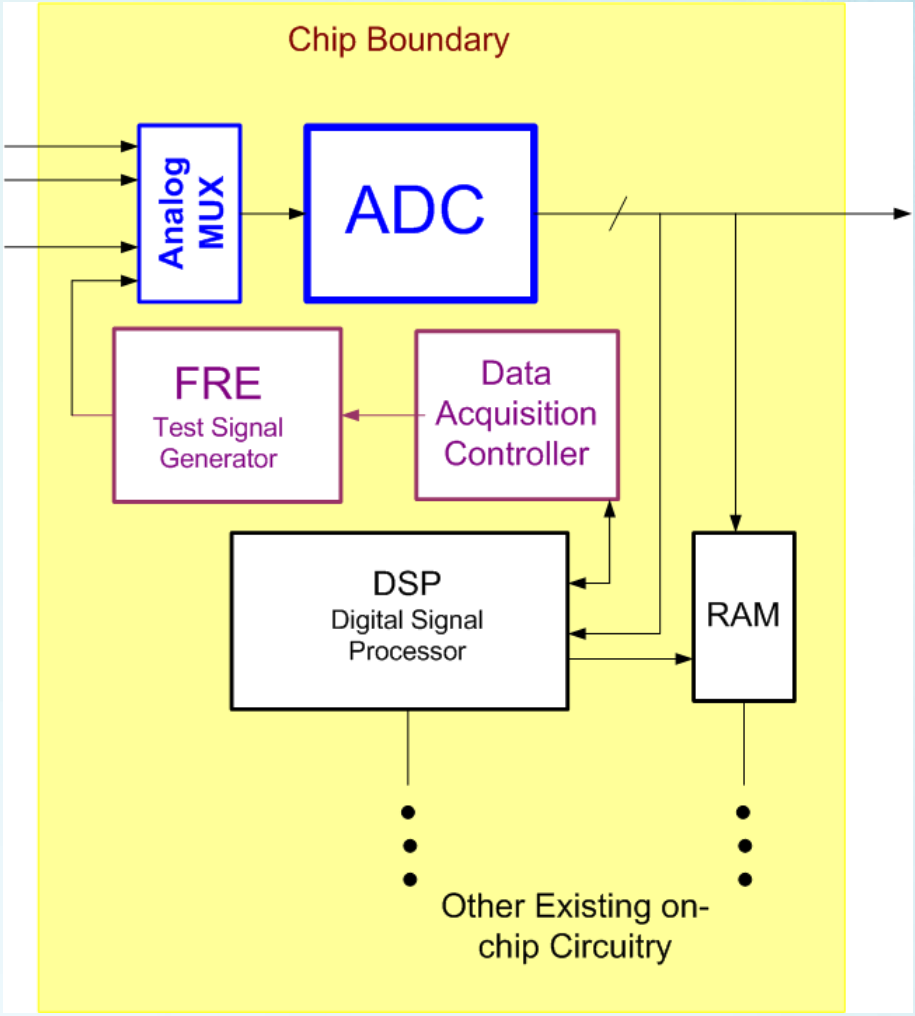
Examples Model or Observer based test

- Functionally Related Excitations (FRE) for linearity testing offer tradeoffs between extreme linearity in test signal for precise control of functional relationship
- Some precise function relationships (here a precise constant shift of both signals) can be practically realized on silicon
- Stimulus Error Identification and Removal (SEIR) algorithm used with FRE to separate nonlinearities of signal source from DUT



Examples Model or Observer based test

Possible implementation of FRE-based BIST for fast ADC test



- Area overhead for BIST very small (shown in purple)
- Use of existing DSP resources during test is minimal
- ADC can be tested on demand throughout life of product
- Very accurate test results possible
- Concept can be extended to reduce size and increase performance of ADC using BIST-based calibration
- Key patent owned by Texas Instruments and Iowa State University

Conclusion

- Highly diversified processes are used to address the wide variety of markets and device requirements in the analog and embedded environment
- High diversity of processes require flexible test interfaces to standardize test flows and equipment
- New processes and devices will drive new test interfaces, technologies and DfT techniques especially for high frequency and high voltages
- Embedded and analog market is extending to non-electrical to electrical integrated devises
- Analog DfT is still in its infancy state

Acknowledgement

- Colleagues from TI
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  - Degang Chen
  - Randy Geiger
  - Sule Ozev

Questions