SW Test Workshop
Semiconductor Wafer Test Workshop

Automatic probe card finding using MSO

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June 4-7, 2017

Overview

- Introduction
- Case studies targets
- Means used in case studies
- Results of MSO calculations
- Summary / Conclusion
- Follow-On Work

Introduction

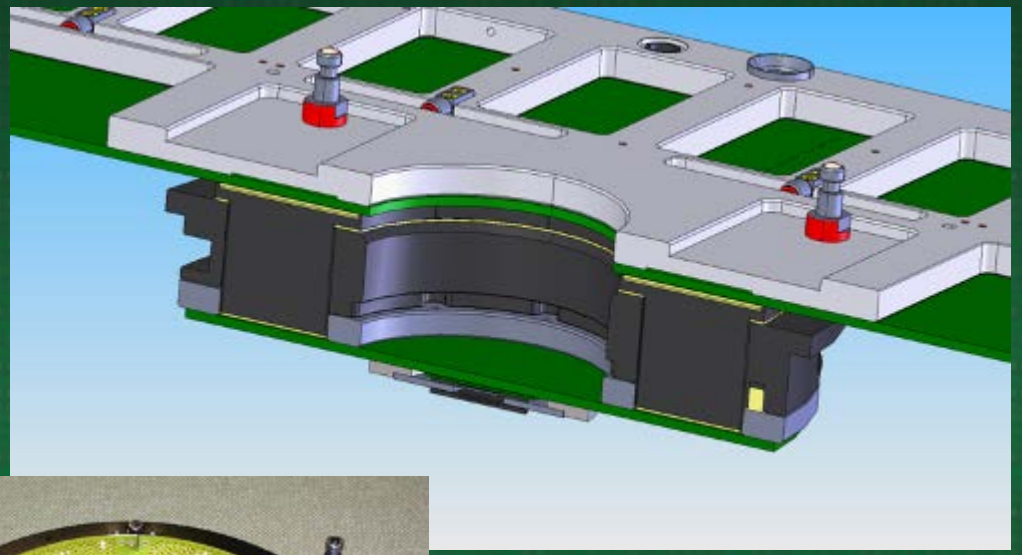
- **Tester perspective**
  - Latest tester generation with more test capacity
  - Direct docking, High Density (HD)
  - Market towards massive increase of DUT count (cost of ownership)
  - Limitations in TDE, space translation and PCB technologies limiting higher site count
- **Probecard perspective**
  - React to new tester capabilities
- **MSO perspective**
  - Optimization software for multi site layouts, touchdowns, steppings, and temperature probing
  - SWTW archive links: BLEYL, et al, 2011; FREDRIKSEN, 2011; MARTENS, et al, 2013

Introduction

- **Tester perspective – Advantest (past to recent)**
  - Earlier Tester platforms:

V93000 – 512 Channel Pogo Tower

V93000 – 1024 Pogo Tower

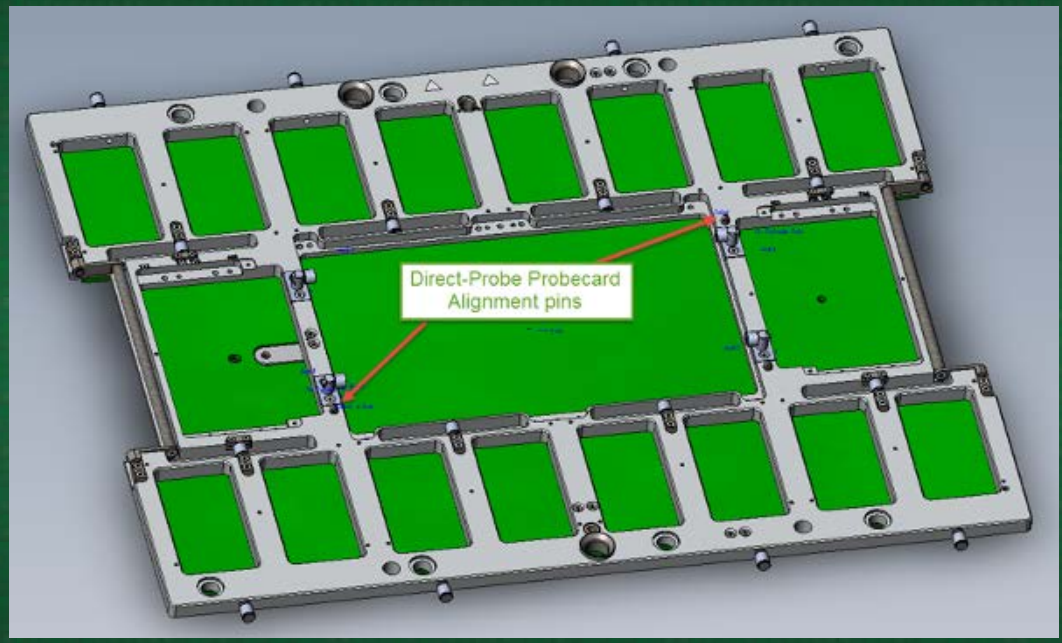


Introduction

- **Tester perspective – Advantest V93000 Direct Probe (recent and future)**
  - Latest Tester platform:

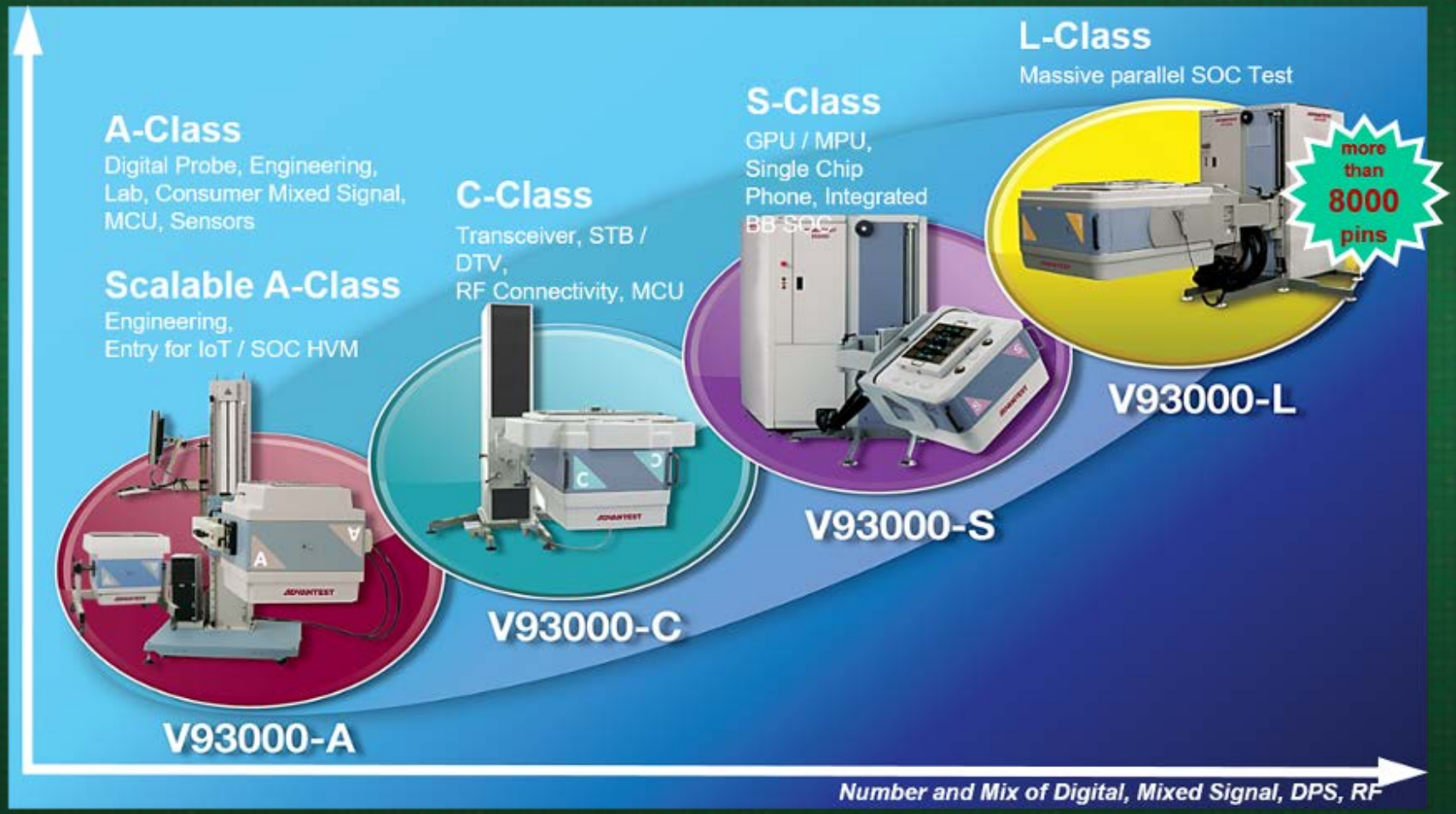
V93000 Direct Probe

PCB Size 600mm x 400mm



Introduction

- **Tester perspective – Advantest V93000 Direct Docking**



V93000-A:
Max. 1024 Channels

V93000-C:
Max. 2048 Channels

V93000-S:
Max. 4096 Channels

V93000-L:
Max. 8192 Channels

Introduction

- **Tester perspective – Teradyne (past to recent)**
  - Earlier Tester platforms:

J750 with Tower (512-1024 channels)

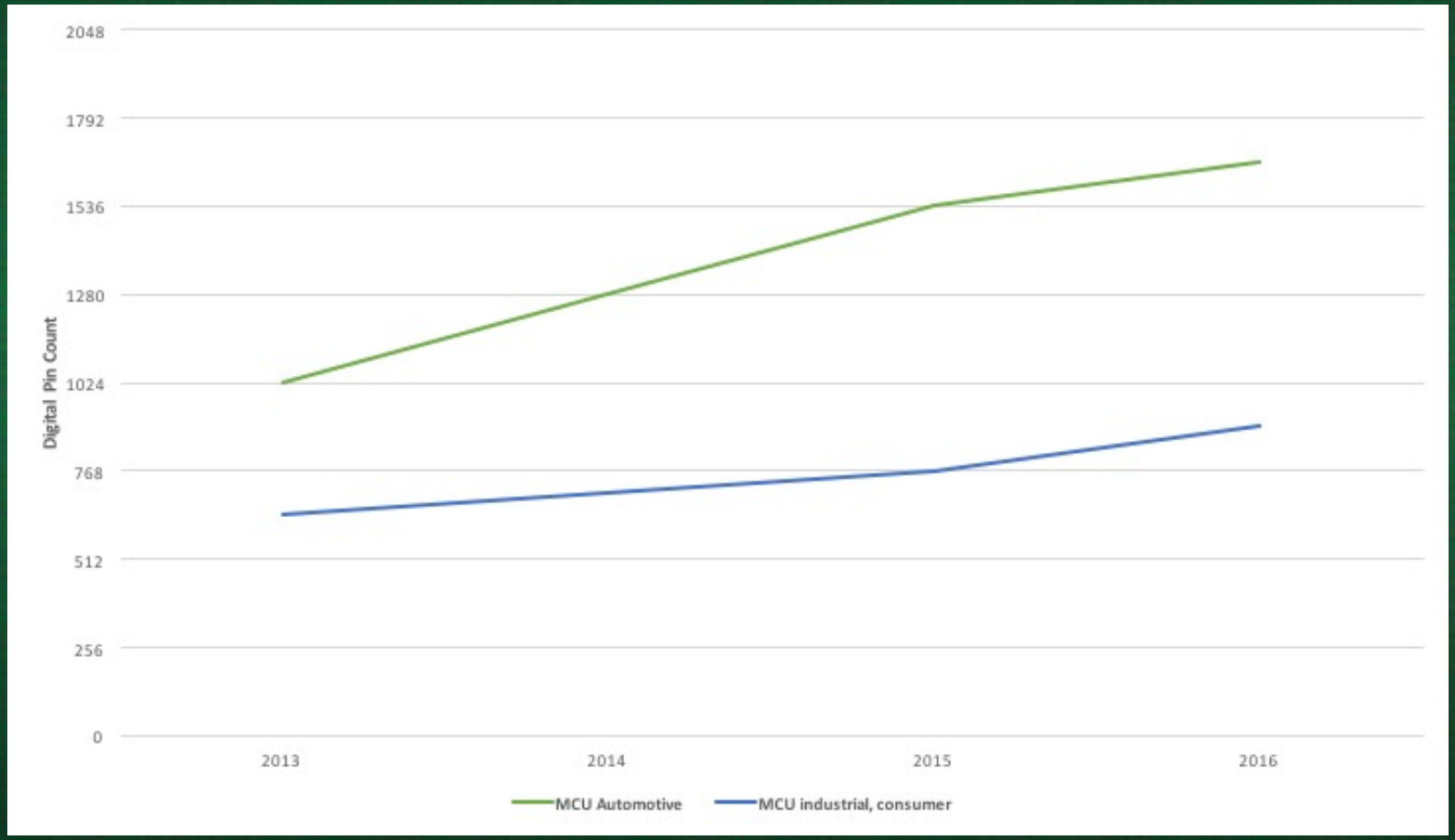
Flex with Tower (512-1024 channels)

Introduction

- **Tester perspective – Teradyne J750EX-HD (recent and future)**
  - Latest Tester platform:

Teradyne J750EX-HD

Max. 2048 Channels

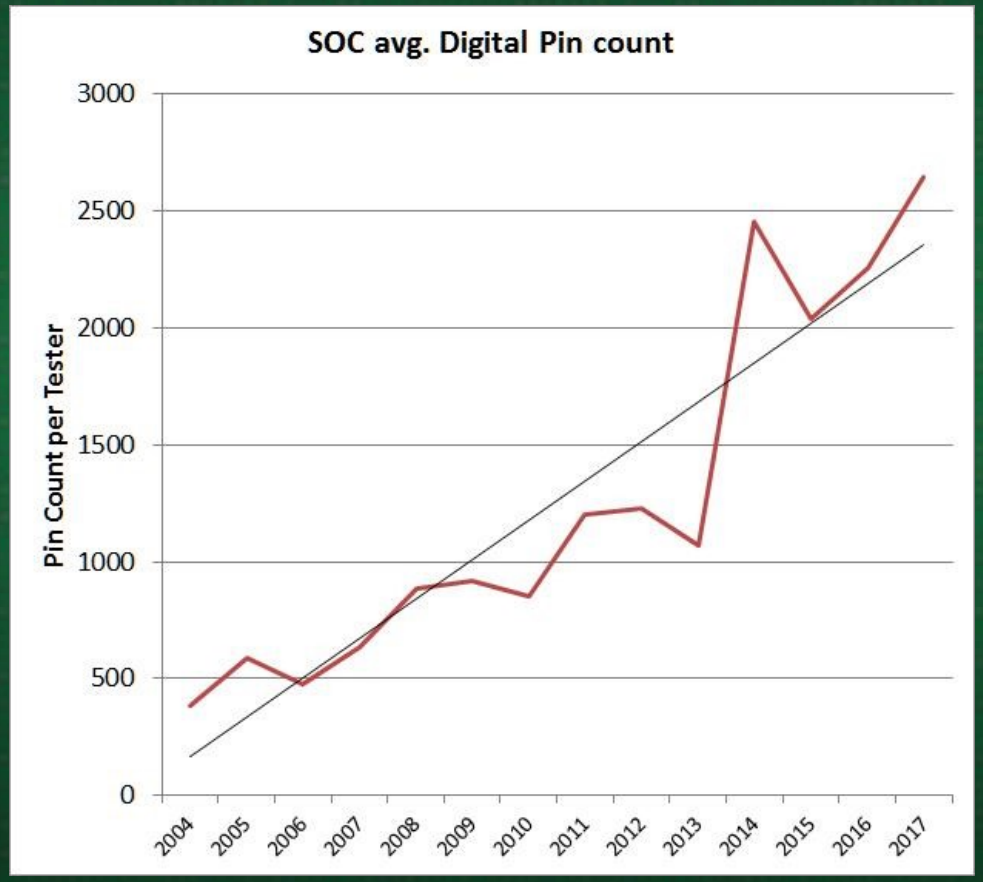


Introduction

- **Tester perspective – Teradyne UltraFlex (Ultraprobe) (recent and future)**
  - Latest Tester platform:

    Teradyne UltraFlex

    Max. 8192 Channels



Introduction

- **Probe card perspective – Past**

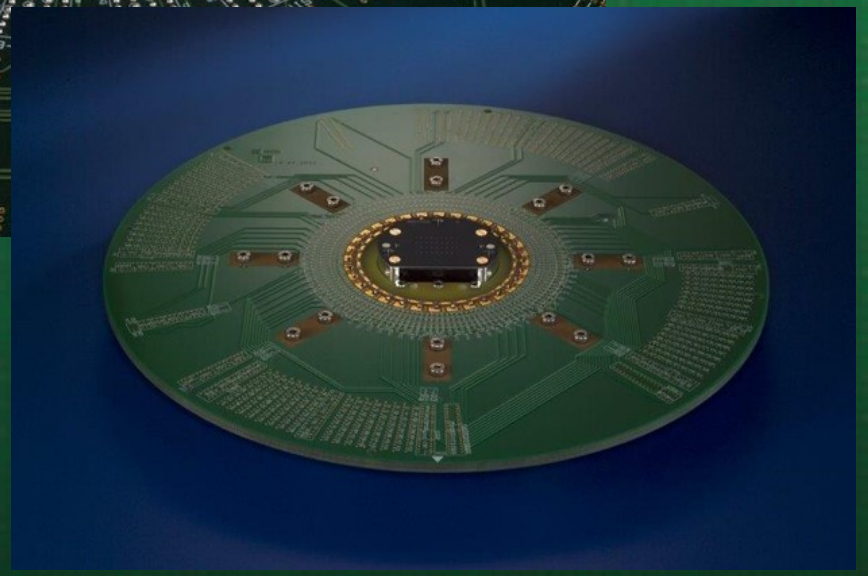
SOC:

Single DUT and up to 16-32DUT

Active Area up to 40mm x 30mm

Limitations:

- Feasibility
- Available Tester Interface Spacing for Probe Head and Connector
- Force per Beam (Prober Deflection) => Pin Count
- Price per Probe Card / Cost of Ownership



Introduction

- **Probe card perspective – Recent**

SOC:

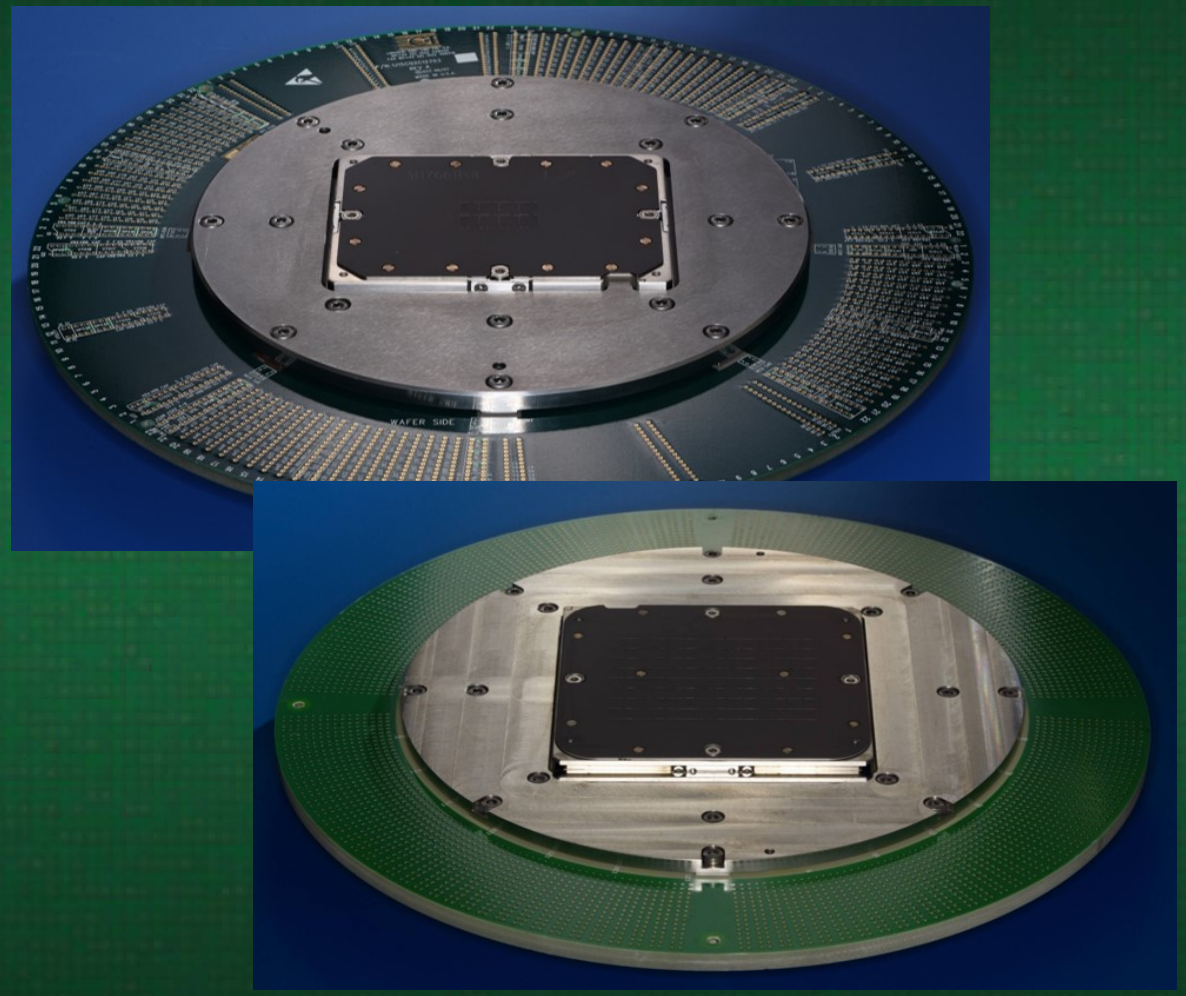
MCU up to 64-128DUT

Chipcard up to 2000 DUT

Active Area up to 100mm x 100mm

Limitations:

- Tester Ressources
- Available Tester Interface Spacing for Probe Head
- Necessary Components on Probe Card for Channel Sharing, Power Sharing… => Available Areas for components
- Force (Test Cell Deflection) / Pin Count
- Cost of Ownership



Introduction

- **Probe card perspective – Future**

SOC:

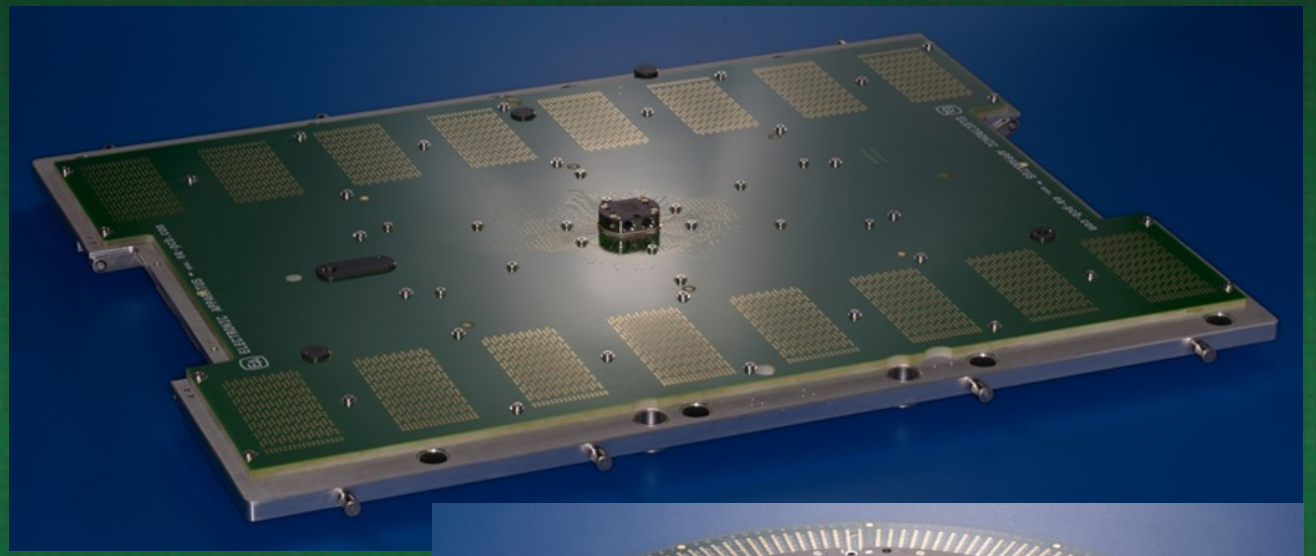
MCU: 128-256-512 (?)

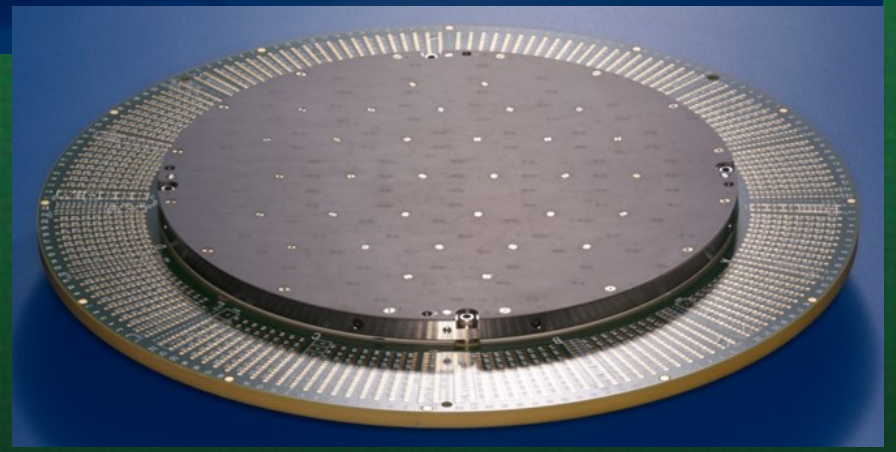
Chipcard: Over 5000 DUT

Active Area 150mmx150mm up to 300mm

TD Optimized Probe Card (?)

Full Wafer Probe Card (?)



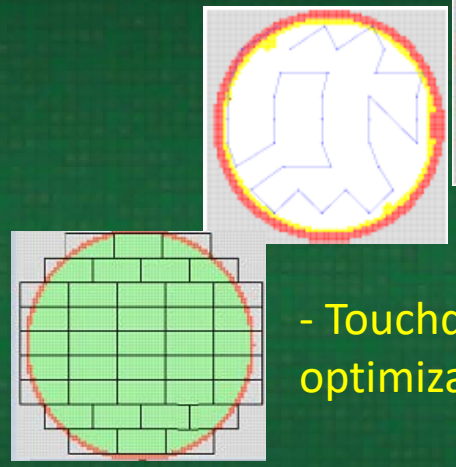


Limitations:

- Space Translation and PCB technologies
- Probe Force (vertical force) per Probe Card
- CTE Matching – Thermal Movement
- Electrical Performance (need for Skip column/ row?)
- Ergo Limit & Handling – weight per probe card…
- Cost of Ownership / Price per Probe Card (price per beam)

Introduction

- **MSO perspective**

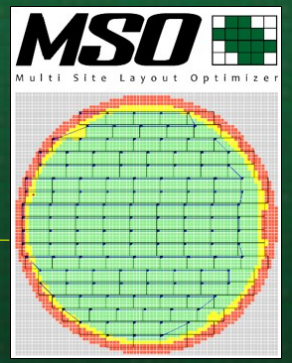


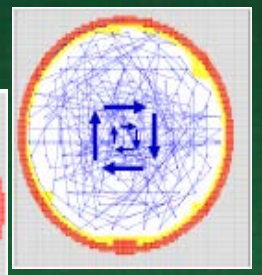
- Touchdown optimizations

Initiated by

IS-TEST

2009

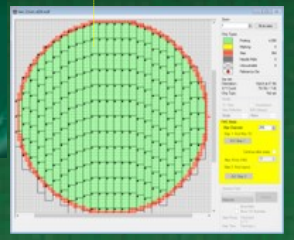




* BLEYL, et al, SWTW 2011

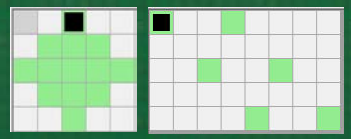
* FREDRIKSEN, SWTW 2011

- Stepping optimizations

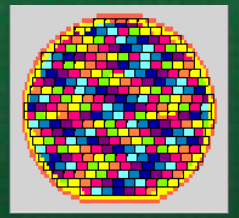


* MARTENS, et al, SWTW 2013

- Full Wafer Contact



- Layout enhancements

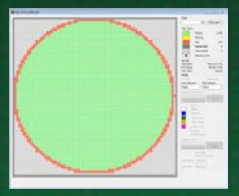


- Stress test probing (testing at the limits)

Automatic
Layout
Finder 2017

Case studies with Feinmetall

- **Workflow principle**



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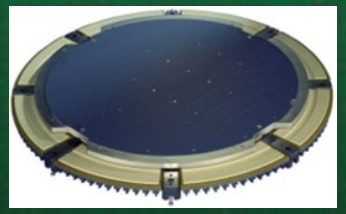
Wafer map Multi site parameter

MSO Multi Site Layout Optimizer

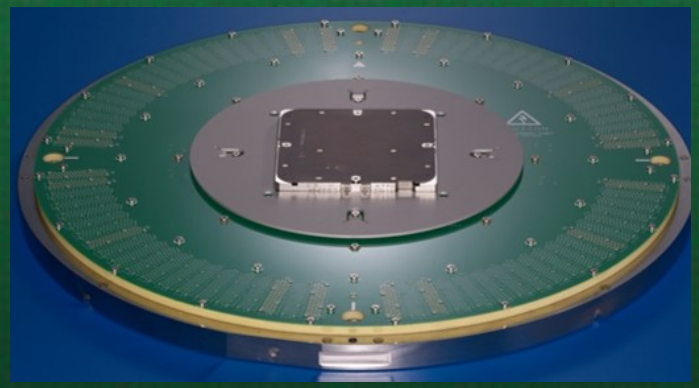


Find ideal multi site **probe card layout**

Case study #1 / targets

Recent world with 2048 DUTs

- Tester: Max. 2048 DUT (for example Teradyne J750)
- Probecard: typical probe head size 80mm x 80mm
- Test temperature: -40° C to 125° C
- 1 Signal – 1 Power – 1 Ground = 3 Beams per DUT
- Test Time: approx. 10 seconds per TD



New world tester with 5k+ DUTs

Question 1

What is the maximum DUT count in predefined probe head sizes (80x80mm^2 vs. 100x100 mm^2) ?

Question 2

Which probe head size is the best (TD-optimized, DUT-count, multi site efficiency) ?

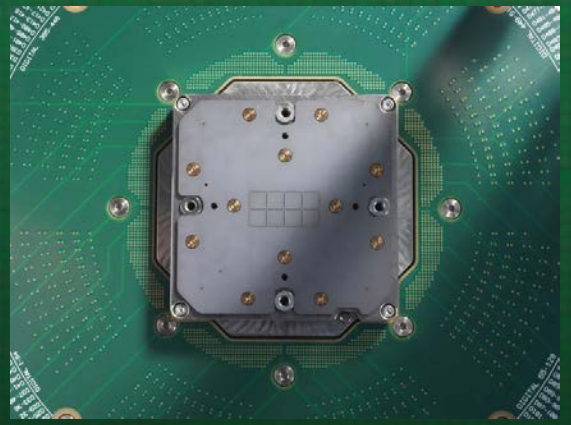
Question 3

What is the best cost/effective solution?

Case study #2 / targets

Recent world MCU testing

- Probe card: typical probe head sizes 40mm x 40mm up to 100mm x 100mm
- Test temperature: -40° C to 180° C
- 12 signals per DUT => 237 Beam per DUT
- Test time: approx. 5 minutes per TD



New world tester with up to 256 DUT

Question 1

64 vs 128 vs 256 DUT: how much efficiency increase is possible?

Question 2

How do necessary skip DUTs influence the overall efficiency ?

Question 3

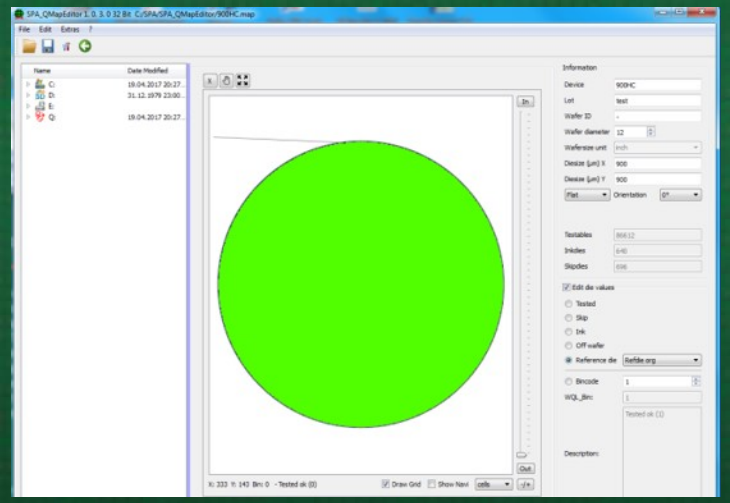
What is the best cost/effective solution ?

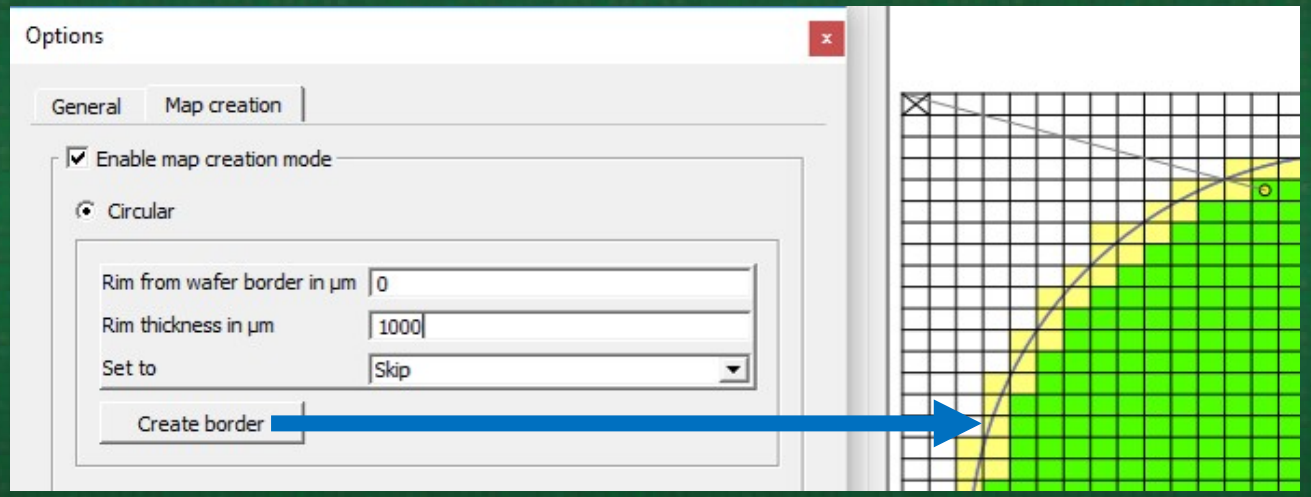
Question 4

Square vs rectangular head size: what is the better choice ?

Means used in the case studies

- **Map creator tool**
  - Select wafer diameter 6“ 8“ 12“
  - Create grid matrix (DUT size)
  - Import created map into MSO
  - Define wafer edge thickness (µm)
  - Create specific DUT sizes and amounts for case studies

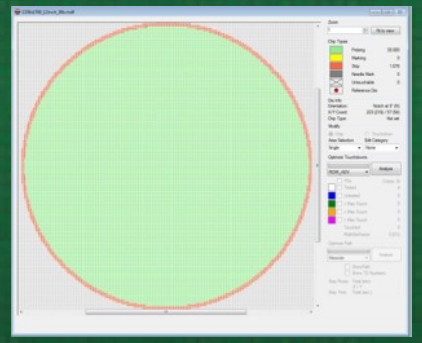




Means used in the case studies

Case study #1
(5k+ DUT)

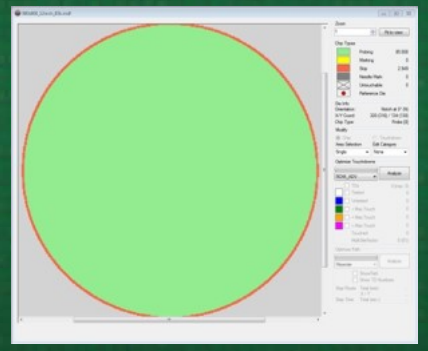
12“ Wafermap A



1,33 x 1,7mm² DUT size

30.000 DUT amount

12“ Wafermap B

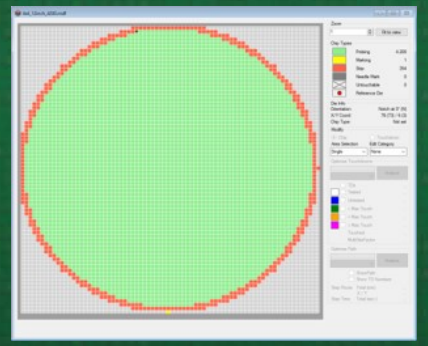


0,9 x 0,9mm² DUT size

85.000 DUT amount

Case study #2
(MCU up to 256 DUT)

12“ Wafermap C



4 x 4mm² DUT size

4200 DUT amount

Means used in the case studies

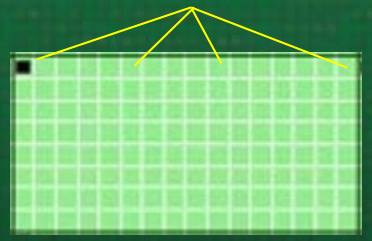
- **MSO application**

used for

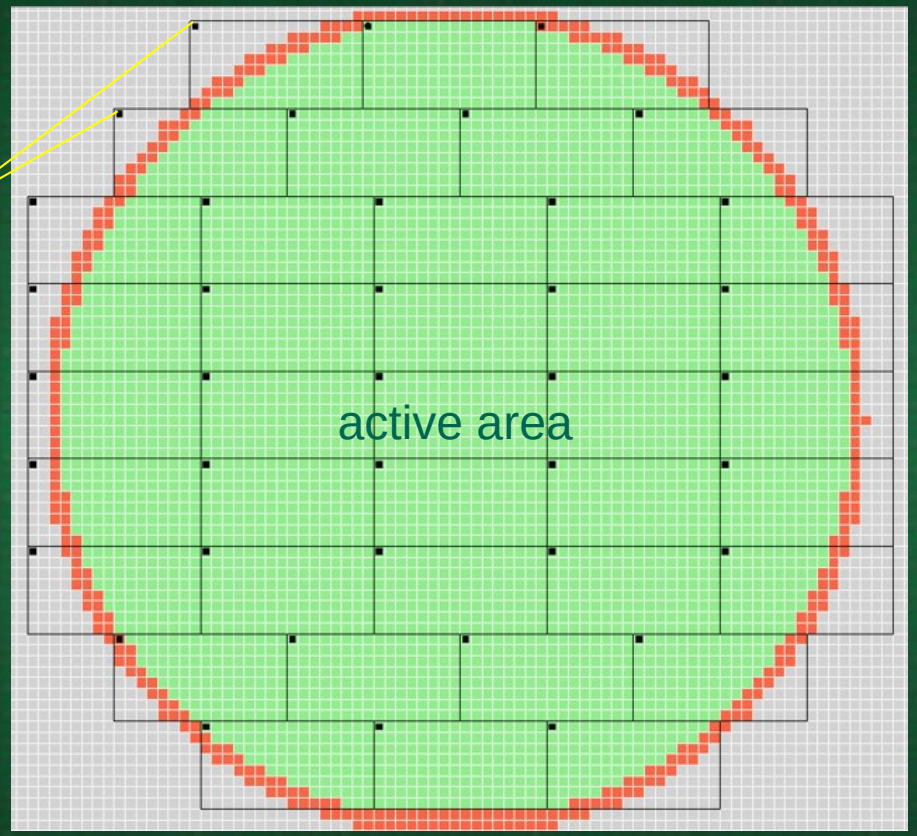
touchdown optimization

and

multi site arrangement



optimization
(with ALF)



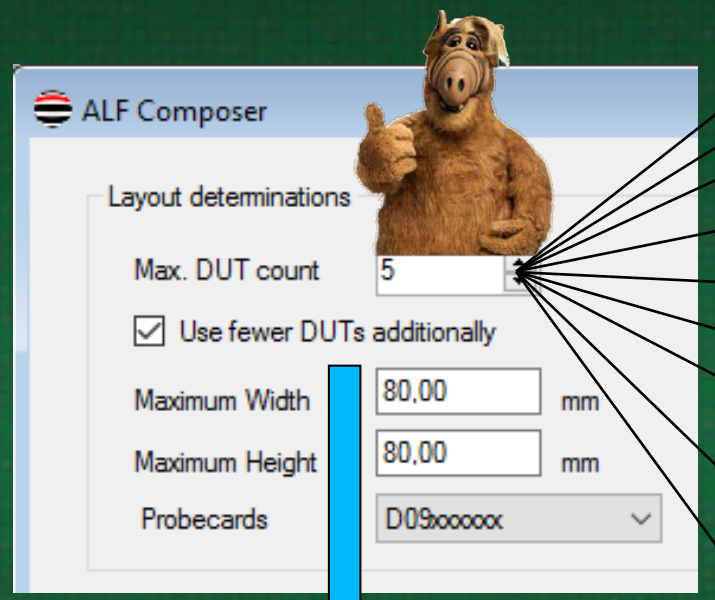
Multi site efficiency
= % average of probe card touching active area dies overall on the wafer
(e.g. 84 % of 128 DUT)

☑ TDs	39 (max. 43)
☐ Tested	4.187
☐ Untested	0
☐ < Max.Touch	0
☐ = Max.Touch	0
☐ > Max.Touch	0
Touched	4.992
MultiSiteFactor	107,4 (84%)

Means used in the case studies

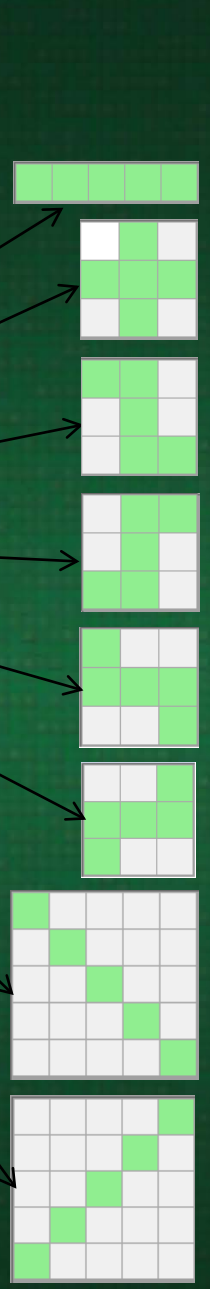
Automatic Layout Finder (ALF)

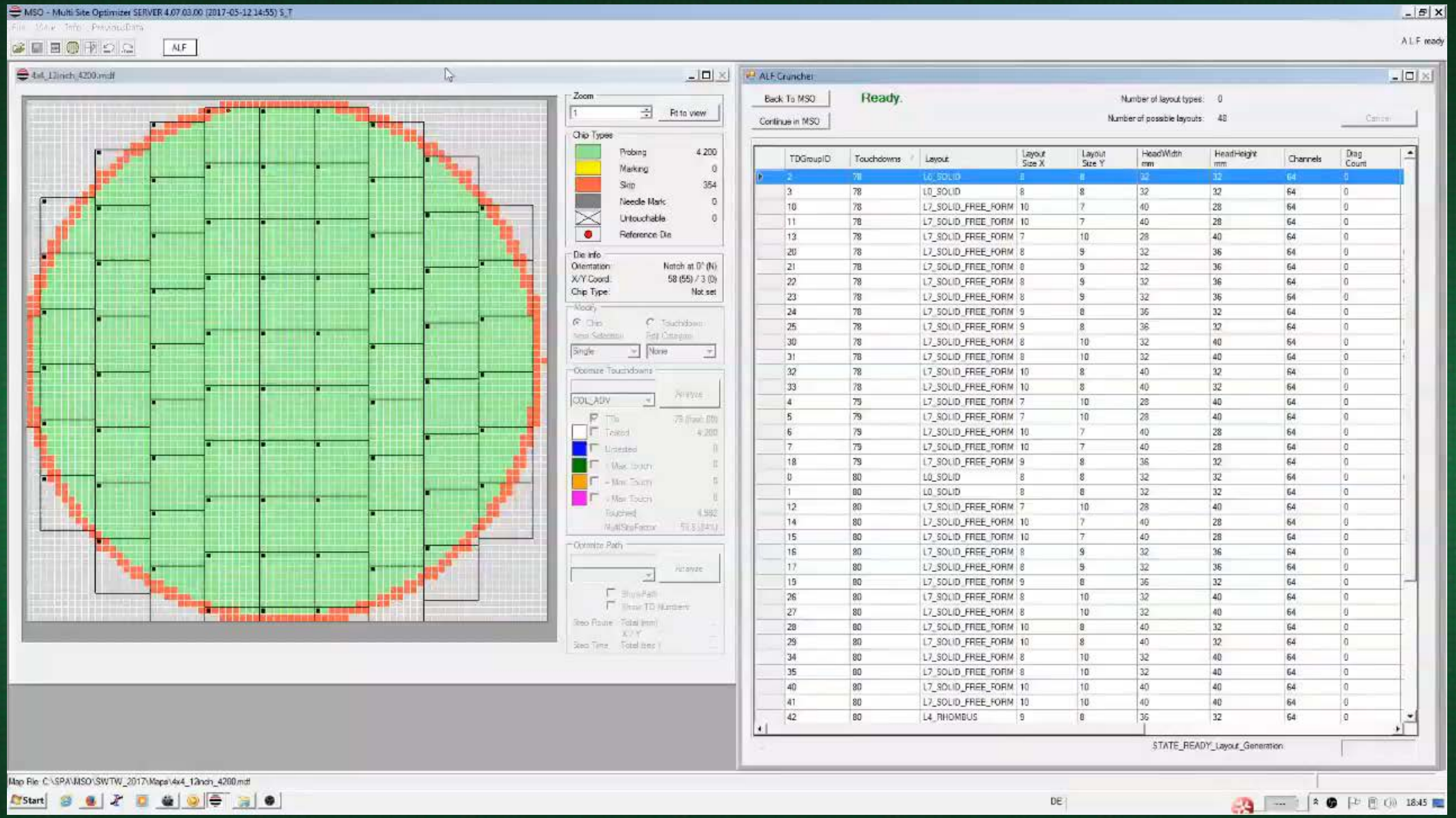
- Calculate multi site variants with given DUT amount
- Limit the results by predefined probe card size
- Calculate ideal DUT amount for best TD result
- Allowing dynamic data analysis for decision making within the multi site probing purchase and -process



- Set multi site DUT amount
- Optionally add DUT range
- Set maximum active area

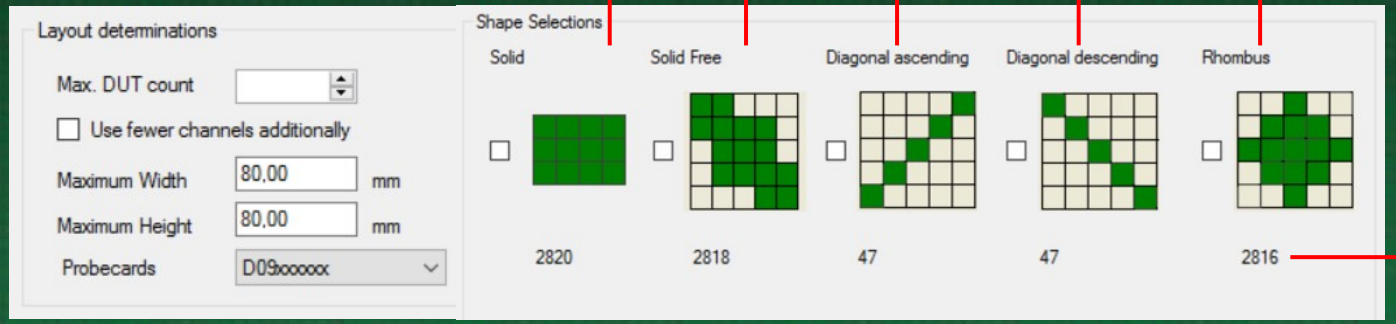
Start calculation




MSO - Multi Site Optimizer SERVER 4.07.03.00 (2017-05-12 14:55) S_T
ALF
ALF ready
4x4_12inch_4200.mdf
Zoom
Fit to view
Chip Types
Probing 4,200
Marking 0
Skip 354
Needle Mark 0
Untouchable 0
Reference Die
Die Info
Orientation: Notch at 0° (N)
X/Y Coord: 58 (55) / 3 (0)
Chip Type: Not set
Modify
Optimize Touchdowns
Optimize Path
ALF Cruncher
Back To MSO
Continue in MSO
Ready.
Number of layout types: 0
Number of possible layouts: 48
Cancel
TDGroupID | Touchdowns | Layout | Layout Size X | Layout Size Y | HeadWidth mm | HeadHeight mm | Channels | Drag Count
2 | 78 | L0_SOLID | 8 | 8 | 32 | 32 | 64 | 0
3 | 78 | L0_SOLID | 8 | 8 | 32 | 32 | 64 | 0
10 | 78 | L7_SOLID_FREE_FORM | 10 | 7 | 40 | 28 | 64 | 0
11 | 78 | L7_SOLID_FREE_FORM | 10 | 7 | 40 | 28 | 64 | 0
13 | 78 | L7_SOLID_FREE_FORM | 7 | 10 | 28 | 40 | 64 | 0
20 | 78 | L7_SOLID_FREE_FORM | 8 | 9 | 32 | 36 | 64 | 0
21 | 78 | L7_SOLID_FREE_FORM | 8 | 9 | 32 | 36 | 64 | 0
22 | 78 | L7_SOLID_FREE_FORM | 8 | 9 | 32 | 36 | 64 | 0
23 | 78 | L7_SOLID_FREE_FORM | 8 | 9 | 32 | 36 | 64 | 0
24 | 78 | L7_SOLID_FREE_FORM | 9 | 8 | 36 | 32 | 64 | 0
25 | 78 | L7_SOLID_FREE_FORM | 9 | 8 | 36 | 32 | 64 | 0
30 | 78 | L7_SOLID_FREE_FORM | 8 | 10 | 32 | 40 | 64 | 0
31 | 78 | L7_SOLID_FREE_FORM | 8 | 10 | 32 | 40 | 64 | 0
32 | 78 | L7_SOLID_FREE_FORM | 10 | 8 | 40 | 32 | 64 | 0
33 | 78 | L7_SOLID_FREE_FORM | 10 | 8 | 40 | 32 | 64 | 0
4 | 79 | L7_SOLID_FREE_FORM | 7 | 10 | 28 | 40 | 64 | 0
5 | 79 | L7_SOLID_FREE_FORM | 7 | 10 | 28 | 40 | 64 | 0
6 | 79 | L7_SOLID_FREE_FORM | 10 | 7 | 40 | 28 | 64 | 0
7 | 79 | L7_SOLID_FREE_FORM | 10 | 7 | 40 | 28 | 64 | 0
18 | 79 | L7_SOLID_FREE_FORM | 9 | 8 | 36 | 32 | 64 | 0
0 | 80 | L0_SOLID | 8 | 8 | 32 | 32 | 64 | 0
1 | 80 | L0_SOLID | 8 | 8 | 32 | 32 | 64 | 0
12 | 80 | L7_SOLID_FREE_FORM | 7 | 10 | 28 | 40 | 64 | 0
14 | 80 | L7_SOLID_FREE_FORM | 10 | 7 | 40 | 28 | 64 | 0
15 | 80 | L7_SOLID_FREE_FORM | 10 | 7 | 40 | 28 | 64 | 0
16 | 80 | L7_SOLID_FREE_FORM | 8 | 9 | 32 | 36 | 64 | 0
17 | 80 | L7_SOLID_FREE_FORM | 8 | 9 | 32 | 36 | 64 | 0
19 | 80 | L7_SOLID_FREE_FORM | 9 | 8 | 36 | 32 | 64 | 0
26 | 80 | L7_SOLID_FREE_FORM | 8 | 10 | 32 | 40 | 64 | 0
27 | 80 | L7_SOLID_FREE_FORM | 8 | 10 | 32 | 40 | 64 | 0
28 | 80 | L7_SOLID_FREE_FORM | 10 | 8 | 40 | 32 | 64 | 0
29 | 80 | L7_SOLID_FREE_FORM | 10 | 8 | 40 | 32 | 64 | 0
34 | 80 | L7_SOLID_FREE_FORM | 8 | 10 | 32 | 40 | 64 | 0
35 | 80 | L7_SOLID_FREE_FORM | 8 | 10 | 32 | 40 | 64 | 0
40 | 80 | L7_SOLID_FREE_FORM | 10 | 10 | 40 | 40 | 64 | 0
41 | 80 | L7_SOLID_FREE_FORM | 10 | 10 | 40 | 40 | 64 | 0
42 | 80 | L4_RHOMBUS | 9 | 8 | 36 | 32 | 64 | 0
STATE_READY_Layout_Generation
Map File: C:\SPA\MSO\SWTW_2017\Maps\4x4_12inch_4200.mdf
Start
DE
18:45

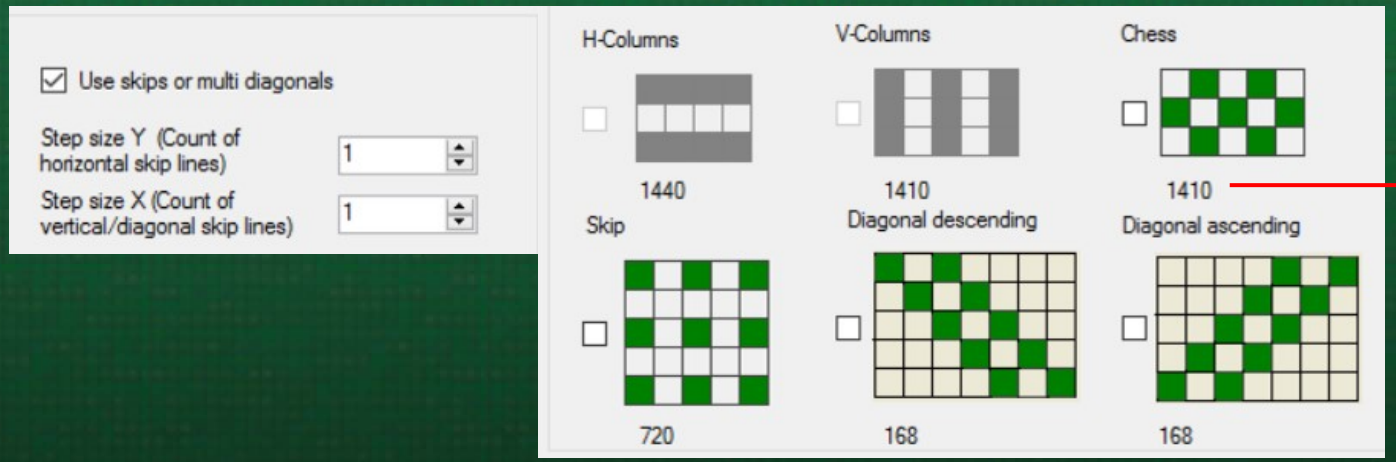
Means used in the case studies

SOLID multi sites



Select multi site shape types for ALF calculations

Multi sites with skips



Max. DUT amount visualized fitting into shape with given active area
e.g. 80mm x 80mm

Results of case study #1

Question 1 -> What is the maximum DUT count in predefined probe head sizes ?

Answer is visualized in MSO-ALF

Wafer / Head	80x80mm² head	100x100mm² head	+ 56,25 % space
Wafermap A (1,33mm x 1,7mm DUT)	2820 DUT	4350 DUT	+ 54,26 % DUT
Wafermap B (0,9mm x 0,9mm DUT)	7744 DUT	12321 DUT	+ 59,10 % DUT

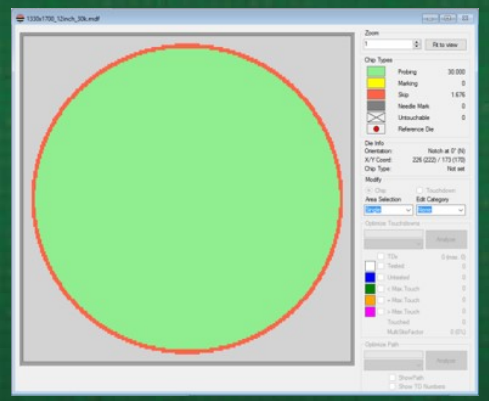
For handling 5000-6000 DUT tester (= new world) the example wafermap A would require a larger probe head than 100x100mm²

Results of case study #1

Question 2 -> which multi site probe card is best (TD-optimized, DUT-count, multi site efficiency) ?

Recent world with 2048 DUT (max.)

12“ Wafermap A



1,33mm x 1,7mm DUT size

30.000 DUT amount

Analysis

80mm x 80mm max. head

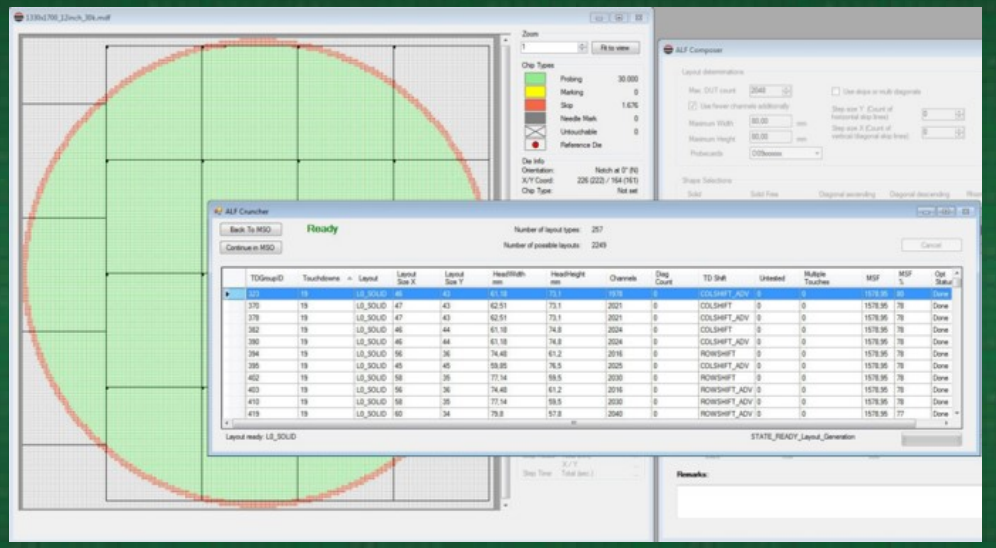
2048 max. DUT

& search 256 less DUT

==========

DUT search range

= 1792 - 2048 DUT !!



Best result = **1978 DUT** with **19 touchdowns**

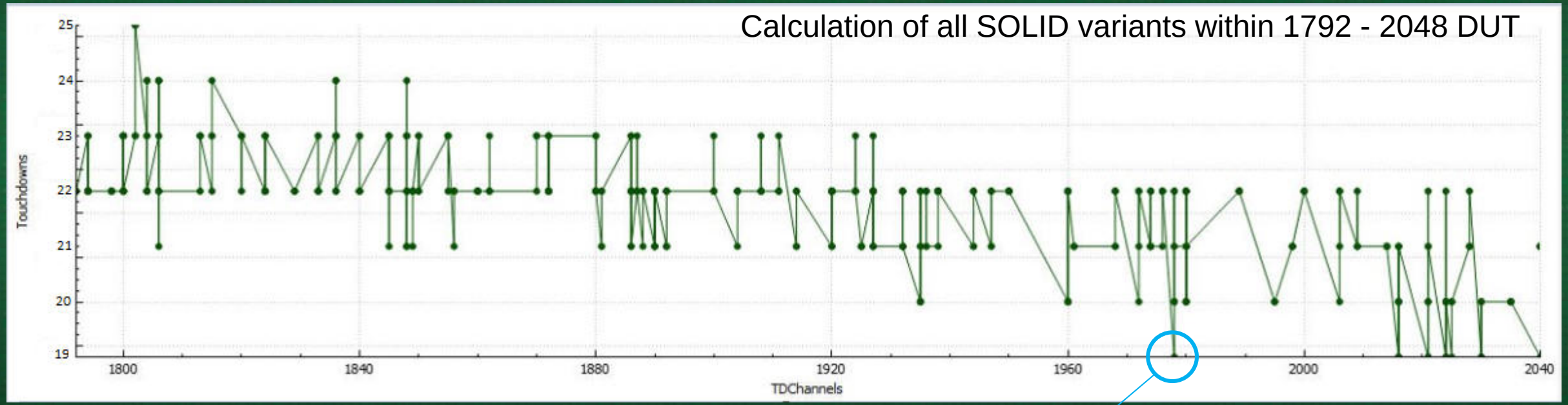
in SOLID layout = 43x46 (61,18 x 73,1mm²)

and highest multi site efficiency of 80%

Results of case study #1

Question 2 -> which multi site probe card is best (TD-optimized, DUT-count, multi site efficiency) ?

Recent world with 2048 DUT (max.)



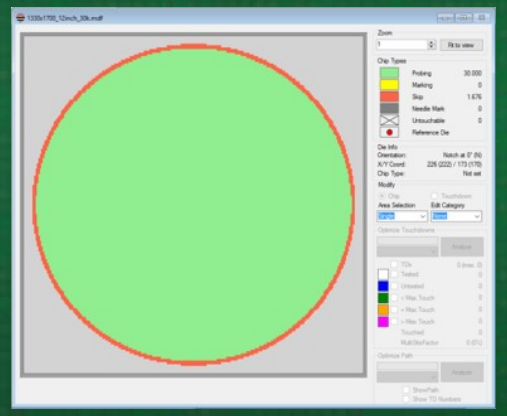
Smallest DUT number (=1978) and equally best touchdowns

Results of case study #1

Question 2 -> which multi site probe card is best (TD-optimized, DUT-count, multi site efficiency) ?

New world tester with 5k+ DUTs

12“ Wafermap A



1,33mm x 1,7mm DUT size

30.000 DUT amount

Analysis

80mm x 80mm max. head

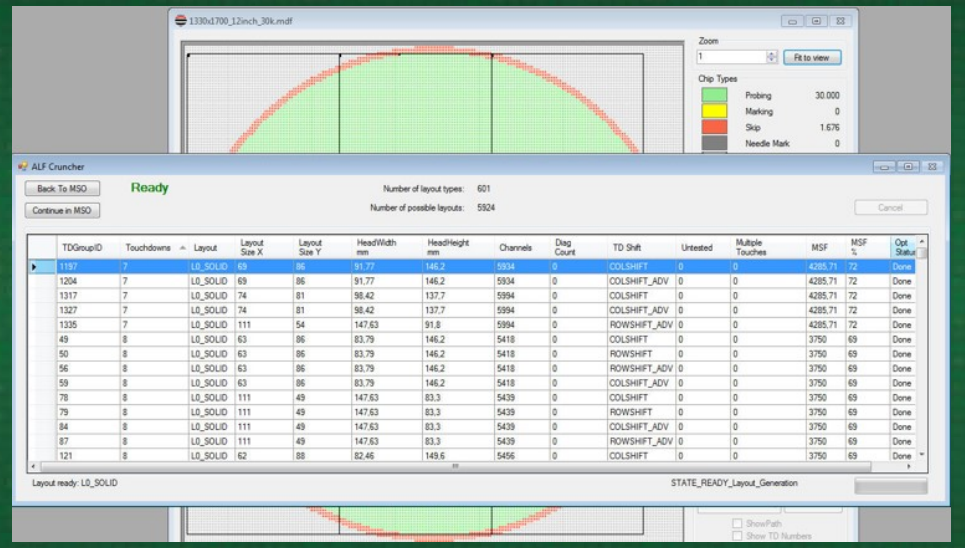
6000 max. DUT

+ Search 10% less DUT

==========

DUT search range

= 5400 - 6000 DUT



Best result = **5934 DUT** with **7 touchdowns**

in SOLID layout = 69x86 (91,77 x 146,2mm²)

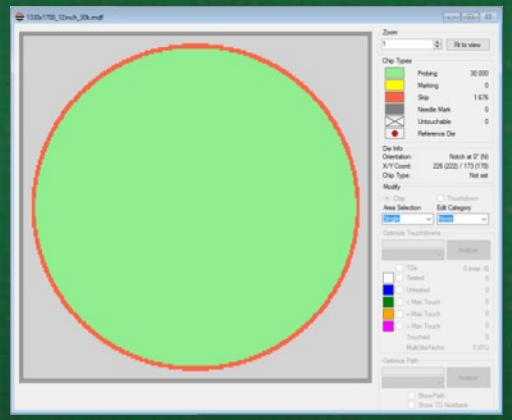
and highest multi site efficiency of 72%

Results of case study #1

Question 2 -> which multi site probe card is best (TD-optimized, DUT-count, multi site efficiency) ?

New world tester with 5k+ DUTs

12“ Wafermap A



1,33mm x 1,7mm DUT size

30.000 DUT amount

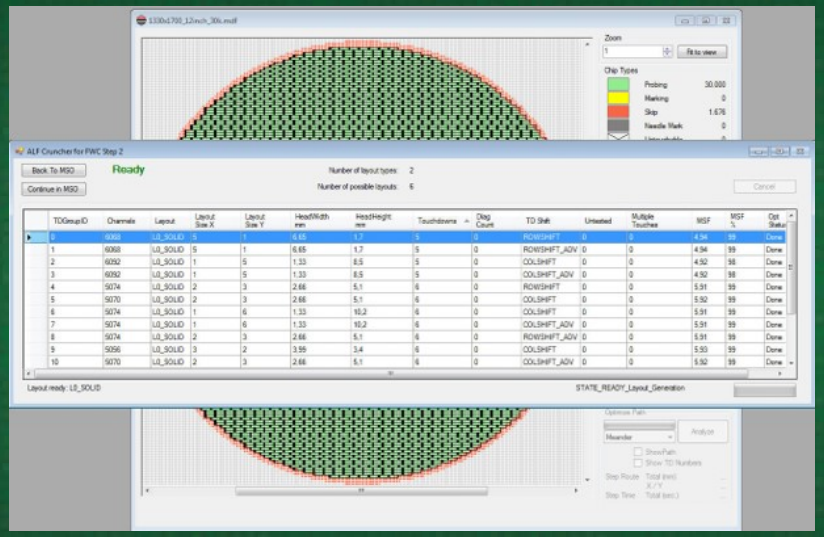
Analysis FWC mode

~ 300mm x 300mm head

5934 DUT start number

+ FWC search method

Full Wafer Contact (FWC)



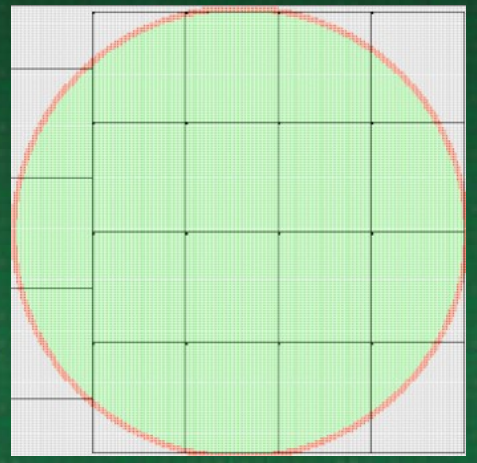
Best result = **6068 DUT** with **5 touchdowns**

in a ~ 300mm x 300mm active area

and multi site efficiency of 99%

Results of case study #1

From 2048 to 5k+ DUT tester (1,33mm x 1,7mm, Wafermap A)



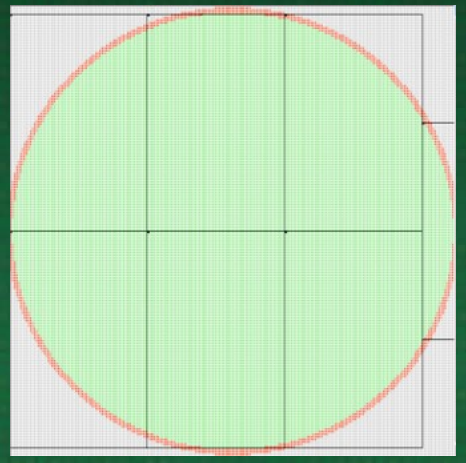
DUT OPTIMIZED

19 touchdowns

1978 DUT

43 x 46 (61,18 x 73,1mm²)

Multi site efficiency 80%



DUT OPTIMIZED

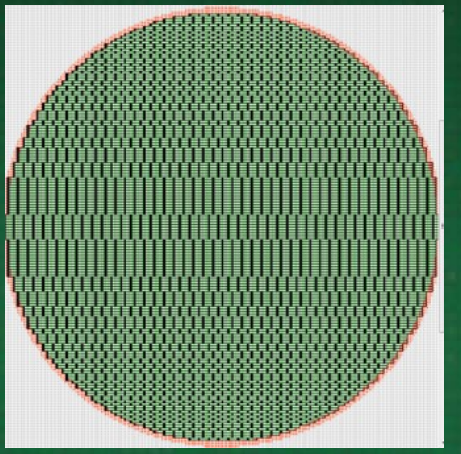
7 touchdowns (-63,1%)

5934 DUT (+200%)

69 x 86 (91,77 x 146,2mm²)

Multi site efficiency 72%

or



FULL WAFER CONTACT

5 touchdowns (-73,7%)

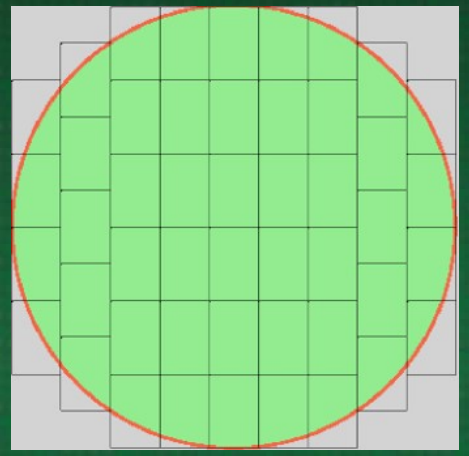
6068 DUT (+207%)

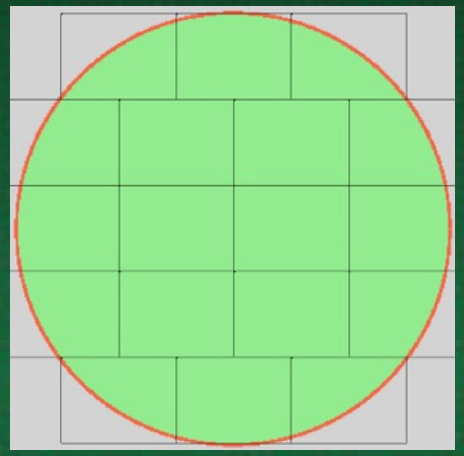
~ 300mm x 300mm active area

Multi site efficiency of 99%

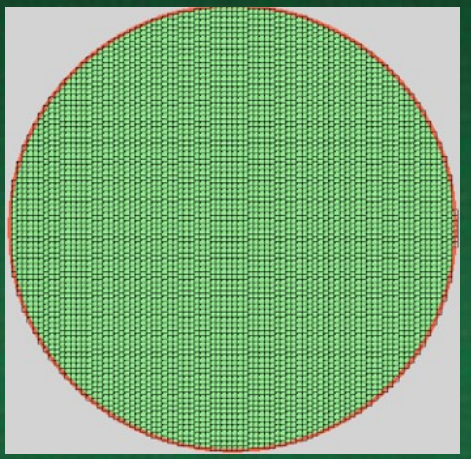
Results of case study #1

From 2048 to 5k+ DUT tester (0,9mm x 0,9mm, Wafermap B)





or



DUT OPTIMIZATION

48 touchdowns

2035 DUT

37 x 55 (33,3 x 49,5mm²)

Multi site efficiency 87%

DUT OPTIMIZATION

18 touchdowns (-62,5%)

5808 DUT (+185%)

88 x 66 (79,2 x 59,4mm²)

Multi site efficiency 81%

FULL WAFER CONTACT

16 touchdowns (-66,7%)

5014 DUT (+146%)

~ 300mm x 300mm active area

Multi site efficiency of 98%

Results of case study #1

New world tester with 5k+ DUTs

Question 3 -> what is the best cost/effective solution ?

Wafermap A – Chipcard Testing – 30k devices on one 300mm wafer – test time: 10 sec

Volume: 100000 wafer (assumption) => 3000 million devices

Cost per test hour: approx. 97 USDollar

Solutions:

- Recent World:

  1978 DUT – Wafermap A – 19 TD => 5934 beams, active area: 61,2mm x 73,1mm => test time: 5277hours

- New World:

  5934 DUT – Wafermap A – 7 TD => 17802 beams, active area: 92mm x 146mm => test time: 1944hours

  6068 DUT – Wafermap A – 5 TD => 18204 beams, active area: 300mm Full Wafer => test time: 1388hours

Results of case study #1

New world tester with 5k+ DUTs

Question 3 -> what is the best cost/effective solution ?

Assumptions for 100000 wafer !

Wafermap A

- 1978 DUT => Test costs of approx. 540.000 USDollar

- **5934 DUT => Test costs of approx. 270.000 USDollar**

- Full Wafer Contact
  with 6068 DUT => Test costs of approx. 260.000 USDollar

Results of case study #2

SOLID

MCU testing with up to 256 DUT

Question 1 -> 64 vs 128 vs 256 DUT: how much efficiency increase is possible ?

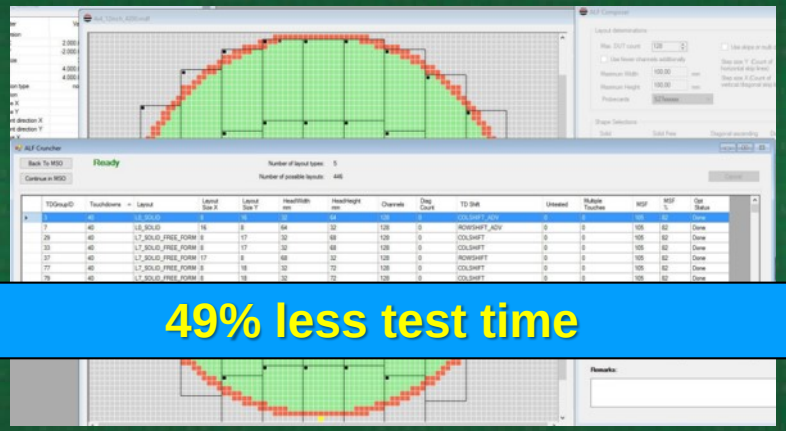
64 DUT (Wafermap C, 4x4mm²)

Best result = 78 touchdowns

SOLID Layout = 8x8 (32x32mm²)

Multi site efficiency = 84%

128 DUT (Wafermap C, 4x4mm²)



Best result = 40 touchdowns

SOLID Layout = 8x16 (32x64mm²)

Multi site efficiency = 82%

256 DUT (Wafermap C, 4x4mm²)

Best result = 22 touchdowns

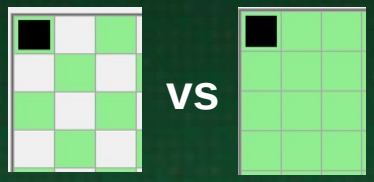
SOLID Layout = 16x16 (64x64mm²)

Multi site efficiency = 75%

Reference test time → 49% less test time → 72% less test time

Results of case study #2

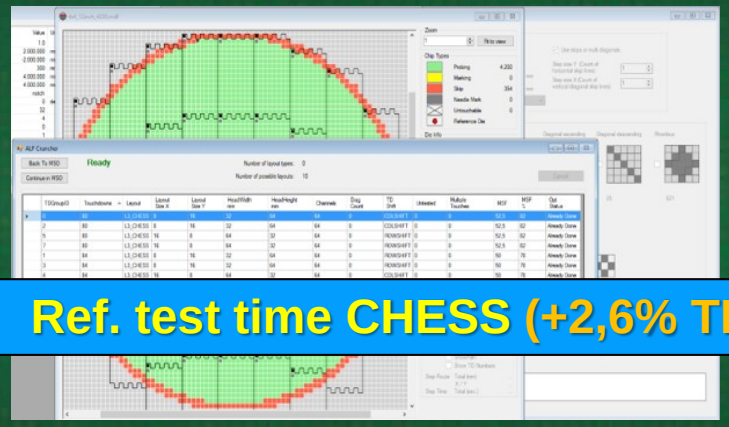
CHESS vs SOLID



MCU testing with up to 256 DUT

Question 2 -> How do necessary skip DUTs influence the overall efficiency ?

64 DUT (Wafermap C, 4x4mm²)



Ref. test time CHESS (+2,6% TD)

Best result = 80 touchdowns (+2)

CHESS Layout = 8x16 (32x64mm²)

Multi site efficiency = 82% (-2%)

128 DUT (Wafermap C, 4x4mm²)

45% less test time (+10% TD)

Best result = 44 touchdowns (+4)

CHESS Layout = 16x16 (64x64mm²)

Multi site efficiency = 75% (-7%)

256 DUT (Wafermap C, 4x4mm²)

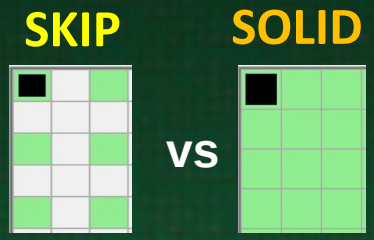
68% less test time (+18% TD)

Best result = 26 touchdowns (+4)

CHESS Layout = 16x32 (64x128mm²)

Multi site efficiency = 63% (-12%)

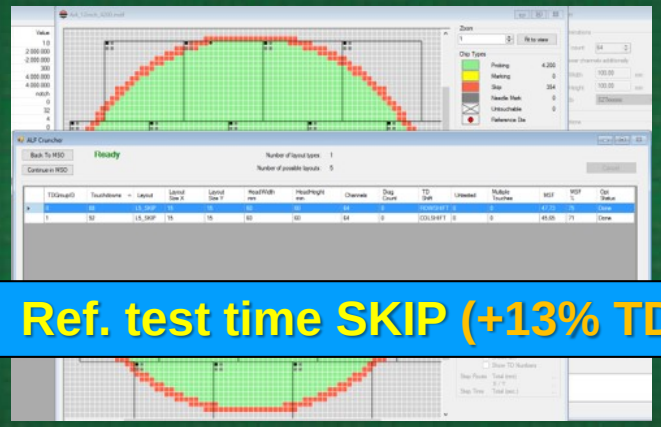
Results of case study #2



MCU testing with up to 256 DUT

Question 2 -> How do necessary skip DUTs influence the overall efficiency ?

64 DUT (Wafermap C, 4x4mm²)

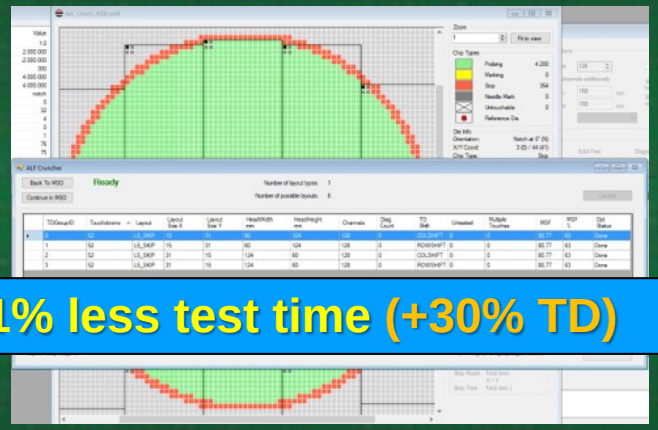


Best result = 88 touchdowns (+10)

SKIP Layout = 15x15 (60x60mm²)

Multi site efficiency = 75% (-9%)

128 DUT (Wafermap C, 4x4mm²)

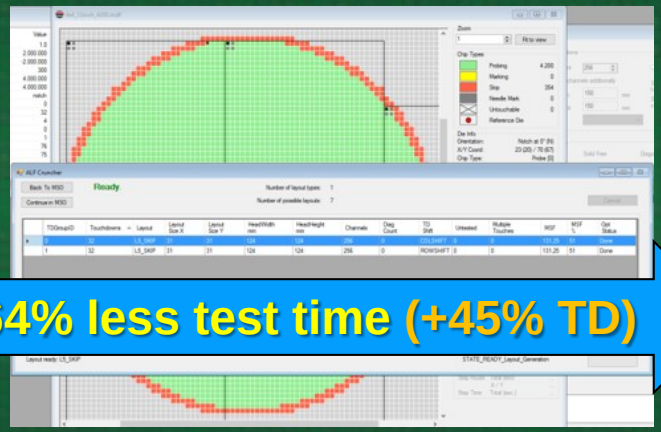


Best result = 52 touchdowns (+12)

SKIP Layout = 15x31 (60x124mm²)

Multi site efficiency = 63% (-19%)

256 DUT (Wafermap C, 4x4mm²)



Best result = 32 touchdowns (+10)

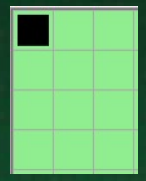
SKIP Layout = 31x31 (124x124mm²)

Multi site efficiency = 51% (-24%)

Ref. test time SKIP (+13% TD) → 41% less test time (+30% TD) → 64% less test time (+45% TD)

Results of case study #2

SOLID



MCU testing with up to 256 DUT

Question 3 -> What is the best cost/effective solution ?

Wafermap C – MCU Testing – 4200 devices on one 300mm wafer – test time: 5 minutes

Volume: 1000 wafer (assumption)

Test Cost per hour: approx. 97 USDollar

Solutions:

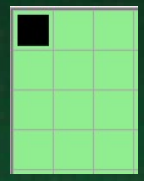
64 DUT – Wafermap C – 78 TD => 15.168 beams, active area: 32mm x 32mm => test time: 6500hours

128 DUT – Wafermap C – 40 TD => 30.336 beams, active area: 32mm x 64mm => test time: 3333,33hours

256 DUT –Wafermap C – 22 TD => 60.672 beams, active area: 64mm x 64mm => test time: 1833,33hours

Results of case study #2

SOLID



MCU testing with up to 256 DUT

Question 3 -> What is the best cost/effective solution ?

Assumptions for 1000 wafer !

Wafermap C

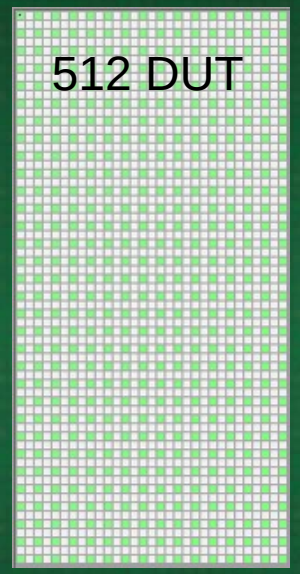
64 DUT => Test costs of approx. 700.000USDollar

128 DUT => Test costs of approx. 450.000USDollar

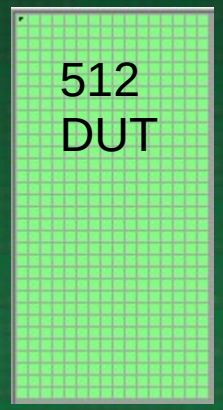
256 DUT => Test cost of approx. 400.000US Dollar

Results of case study #2

Efficiency increase by moving from SKIP to SOLID multi site (customer case)



296 TDs



266 TDs

265 TDs

Single DUT:
460 x 505 µm²

MSO Multi Site Layout Optimizer

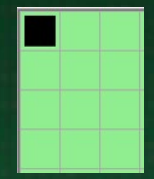
10,14 % increased efficiency

ALF

+0,33 % increased efficiency
2 less DUT

Results of case study #2

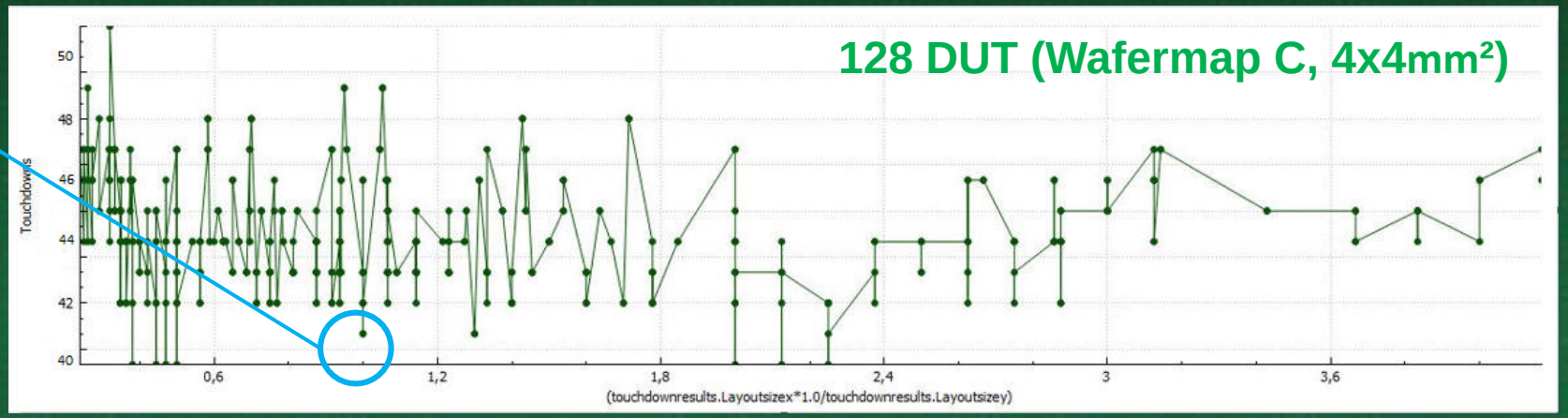
SOLID

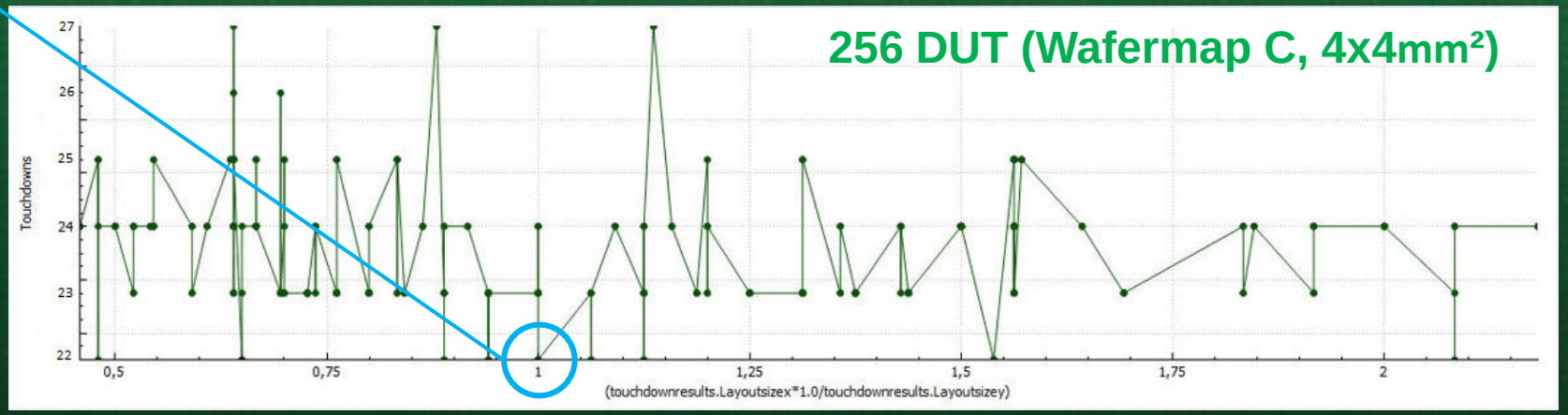


Question 4 -> square vs rectangular head size: what is the better choice?

- Square (aspect ratio = 1) is not the best touchdown result

- Square (aspect ratio = 1) equally best touchdown result like non-square variants.





Both square and rectangular must be considered being the better choice (case by case)

Summary of findings

Case study #1

- **With existing tester platform the best solution is a 80mm x 80mm head with 1978 DUT (Wafermap A) and 2035 DUT (Wafermap B).**

- **It makes sense to go for the latest tester platform and 6000 DUT. Best solution is 150mm x 150mm head with 5934 DUT (Wafermap A) and 80mm x 80mm head with 5808 DUT (Wafermap B).**

- **Full Wafer Contact is more efficient but cost of ownership needs to be considered.**

Summary of findings

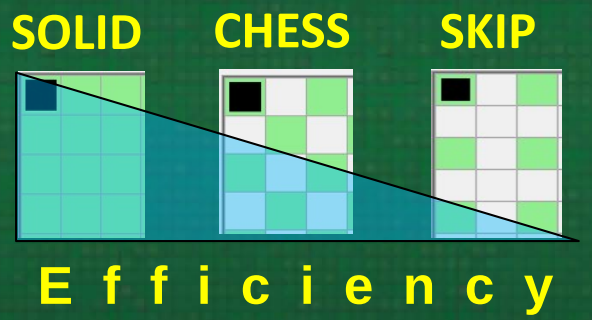
Case study #2

- **For wafermap C a 100mm x 100mm head is sufficient for 128DUT and around 30k beams.**
- **128DUT seems to be the optimum due to the fact that the test time is long and the test temperature is high (up to 180° C).**
- **Full Wafer Contact seems nearly impossible due to the test temperature of -40° C to 180° C !**

General conclusions

- **The maximum DUT ressources available do not always bring the best touchdown result in respect to multi site efficiency and touchdown amount.**

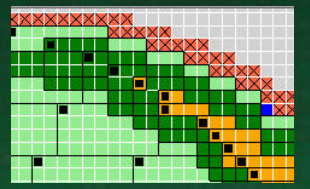
- **Enlargened tester ressources increase the test time efficiency whereas overall savings are limited by cost of ownership consideration! The increase of efficiency from higher tester ressources flattens when using CHESS layouts and even more with SKIP layouts.**



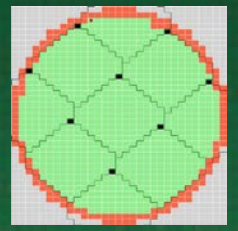
- **MSO with its Automatic Layout Finder (ALF) is a good analysis tool for a probe card vendor to find the best probe card solution for the customer.**

Potential follow-on work

- ALF analysis with wafer edge exclusion

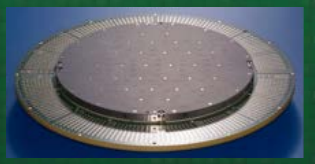


- Rhombus / Freeform and other layout shape considerations



- Squared vs. rectangular head research with more map variants

- Full Wafer Contact vs. cost of ownership



- Temperature test related optimization of probe card design (hot / cold)

Acknowledgements

Teradyne
Joseph Ha, Product Manager

Advantest
Ulrich Schoettmer, Solution Product Manager

SPA Software Entwicklungs GmbH
Alexander Pollak, Software Engineer

SPA Software Entwicklungs GmbH
Uwe Raps, Software Engineer

Thank you for your attention !