SW Test Workshop
Semiconductor Wafer Test Workshop

Simulating Electrical Performance of Probe Cards to Enable them to Work "Right out of the Box"

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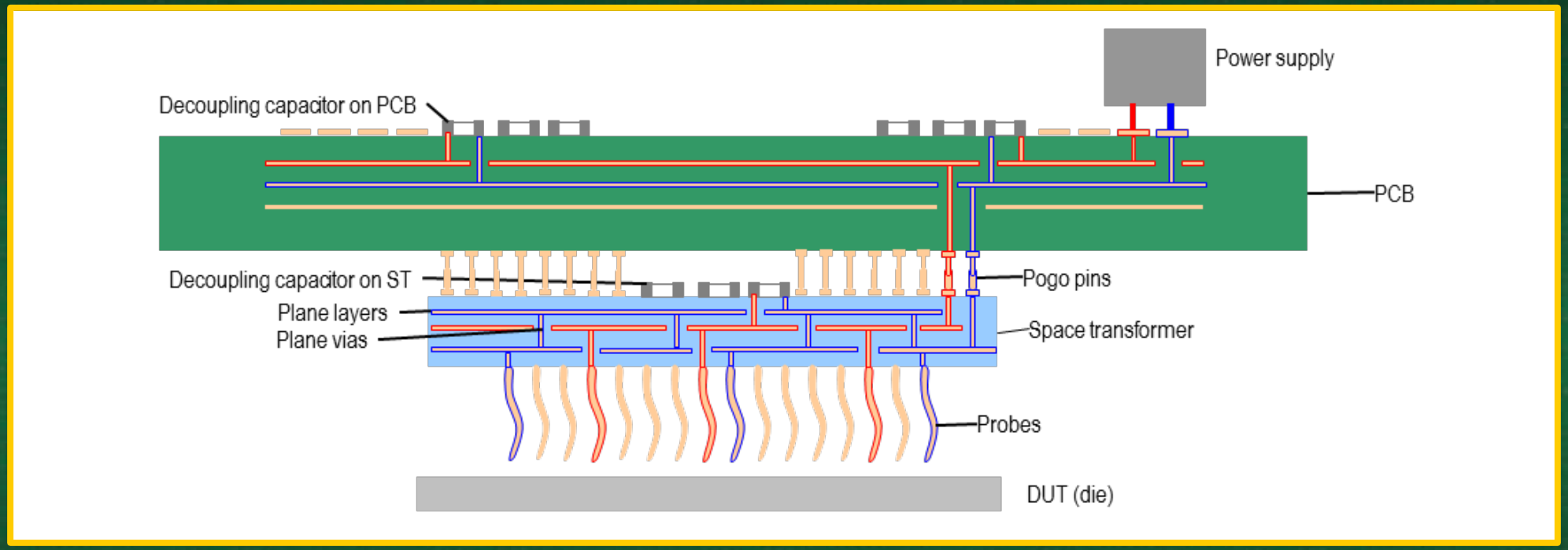
Overview

- Introduction
- Need for SI/PI simulations for probe-cards
- SI/PI Analysis methods for probe-cards
- S-parameters Measurement, Simulation & Correlation
- Summary

Anatomy of a Probe Card (What does an Electrical Engineer see?)



"A complex electro-mechanical system with passive electrical components"

Need for SI/PI Simulations

- Due to reducing design cycles it is essential to make sure cards perform right out of the box ➔ accurate simulations are a step towards achieving this goal !!
- Automotive applications require high currents hence are more susceptible to higher IR drop & increased power supply noise.
- Probe cards no longer just serve as DC connection interface but are evolving according to industry needs hence SI/PI simulation methodology also needs to evolve accordingly.

SI/PI Analysis Items for Probe Cards

- DC Resistance estimation
- DC IR drop summary
- RLC extraction
- Decoupling capacitor placement distance estimation
- PDN analysis strategy
- S-parameter simulation, measurement & correlation

DC IR Drop Analysis

- **Tools used**
  - ANSYS SIwave or Keysight ADS SI/PI pro
- **Information needed to do such an analysis**
  - Voltage of PWR Supply
  - Peak DC current draw from a PWR Supply
  - Allowed DC IR drop (most cases 0.5-5%)

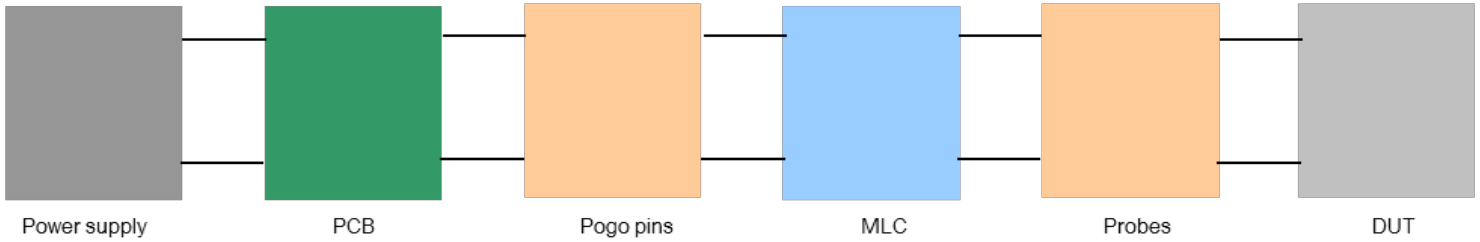
DC Path Resistance Estimation

- DC IR drop depends on full path resistance
- $R_{probe\text{-}card} = R_{PCB} + R_{MLC} + R_{probes} + R_{cres}$

Probe-card contribution

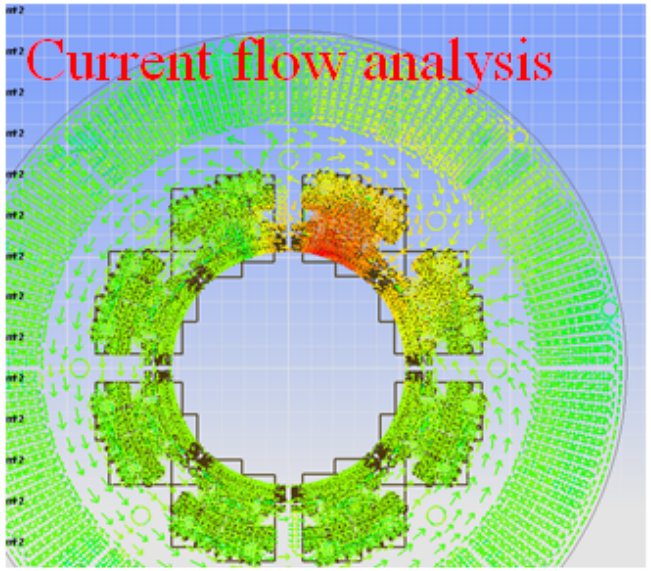
wafer contribution

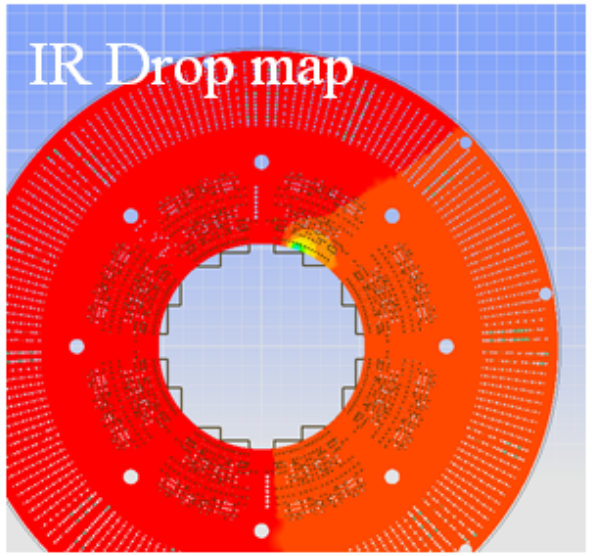
- $R_{DC\text{-}PATH} = R_{PCB} + R_{MLC} + R_{probes}$



DC IR Drop Analysis

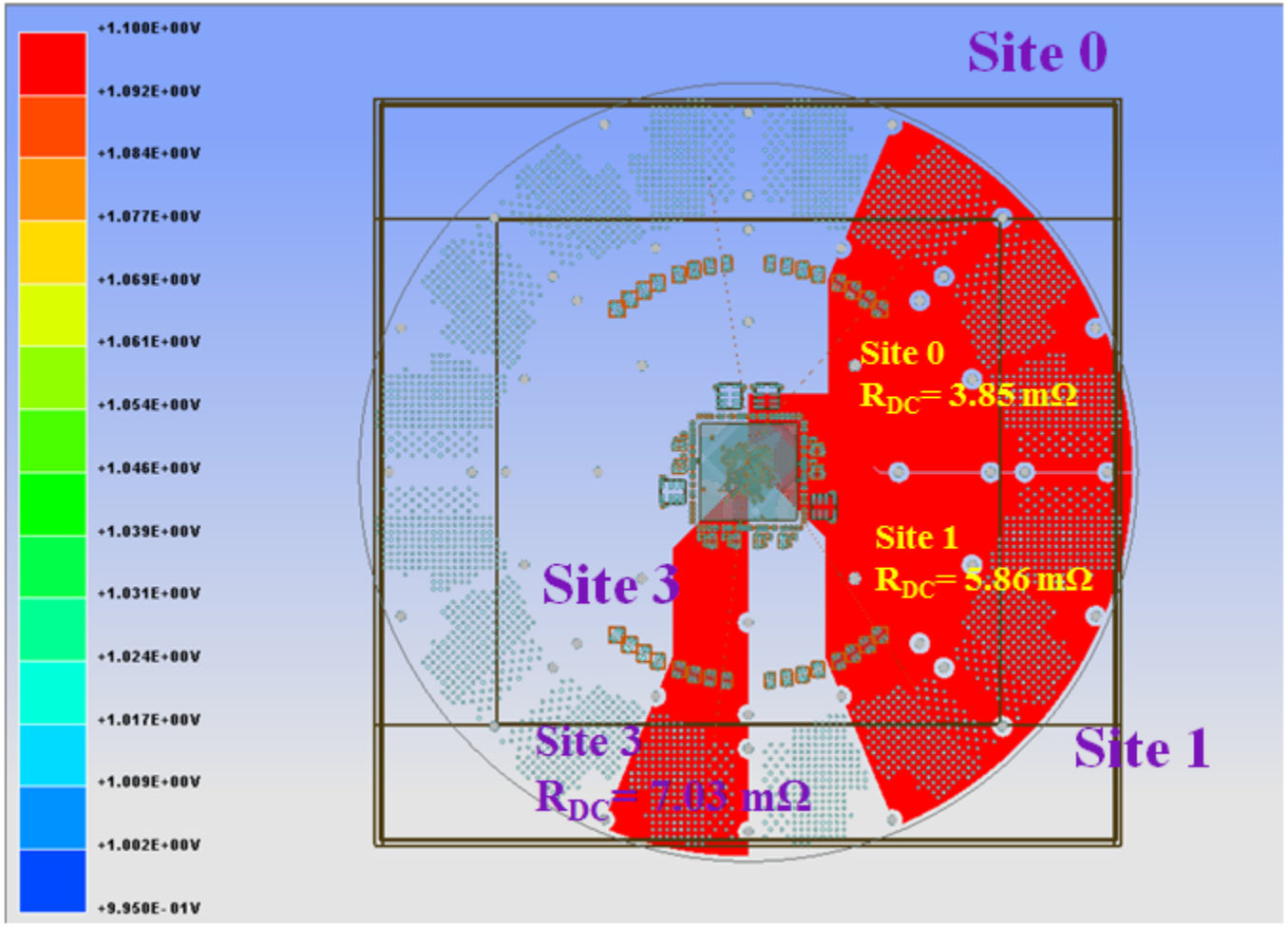
- Once DC resistance is determined using simulations, IR drop can be calculated with Ohm's law.
- $DC\ IR\ drop = Rdc\ .I_{max}$
- An IR drop of 0.5%-5% of the nominal voltage is tolerated depending on the total system-level margin allowed for proper device functionality and sense line position.





DC IR Drop Analysis: PCB

PWR = VDD1P0



DC IR Drop

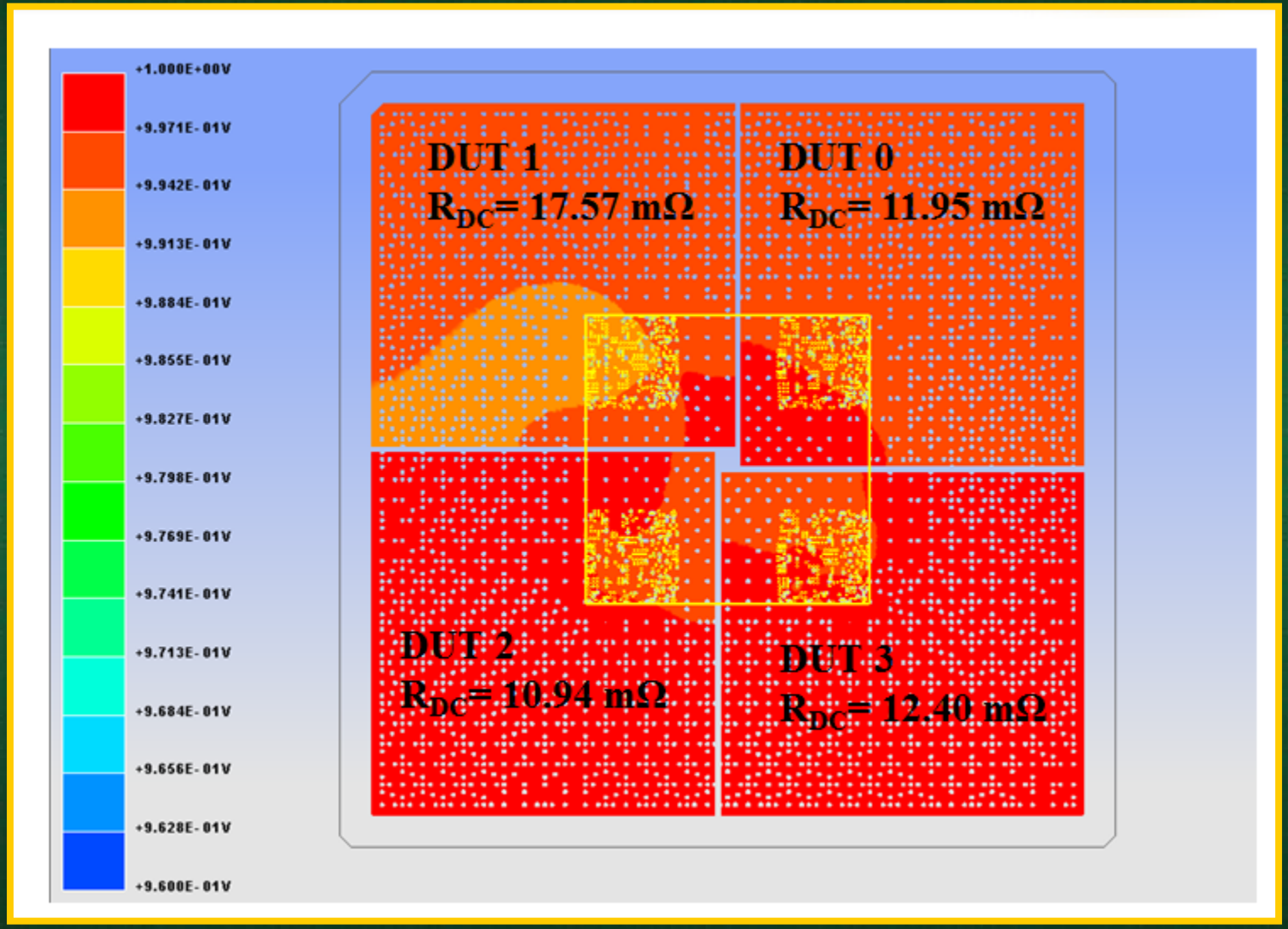
Site 0 : 1.52 mV

Site 1 : 2.34 mV

Site 3 : 2.81 mV

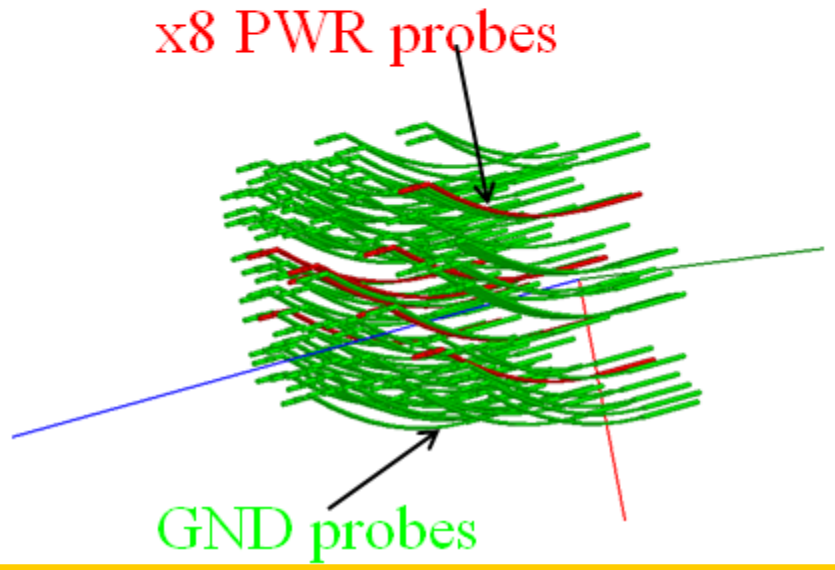
I= 0.4 mA

DC IR Drop Analysis : MLC (Space Transformer)



DC IR Drop Analysis : Probes

- Probe diameter = 3.0 mils
- R_{DC_probe} = 0.16414 Ω
- Each site has 8 probes ; R ~ 0.02 Ohm ➔ 20 mΩ



DC IR Drop Analysis

Power Plane Name		PCB contribution (mΩ)	MLC contribution (mΩ)	Probe Contribution (mΩ) *8 each site	Total Probe-card DC resistance (mΩ)	DC IR Drop due to probe-card $\Delta V = I_{DC} \times R_{DC}$ (mV)
VDD1V0_GRP3	DUT 0	3.85	11.95	20	35.8	14.32
	DUT 1	5.86	17.57	20	43.43	17.37
	DUT 2	5.09	10.94	20	36.03	14.41
	DUT 3	7.03	12.40	20	39.43	15.77
Estimating % contribution PCB/Total = % PCB MLC/Total = % MLC Probe/Total = % Probe						
% contribution	DUT 0	10.75	33.37	55.86		
	DUT 1	13.49	40.45	46.05		
	DUT 2	14.12	30.36	55.50		
	DUT 3	17.82	31.48	50.72		

Target DC Resistance

- Achieving low DC path resistance and meeting target impedance is critical.
  - Analyze full path $DC\ IR\ drop = Rdc\ .I_{max}$ and minimize R_{DC}
  - R_{DC} = Voltage_rail * (% tolerance) / I_{MAX}
  - R_{VDD1P0}(target) = 1.0^{V}*0.05/(0.4mA) = 125 mΩ

- RDUT0 = 35 mΩ
- RDUT1 = 43 mΩ
- RDUT2 = 36 mΩ
- RDUT3 = 39 mΩ

<< Target DC resistance 125 mΩ

- **For best results "R_{PATH} + Cres < $R_{DC\text{-}target}$"**

DC IR Drop Summary

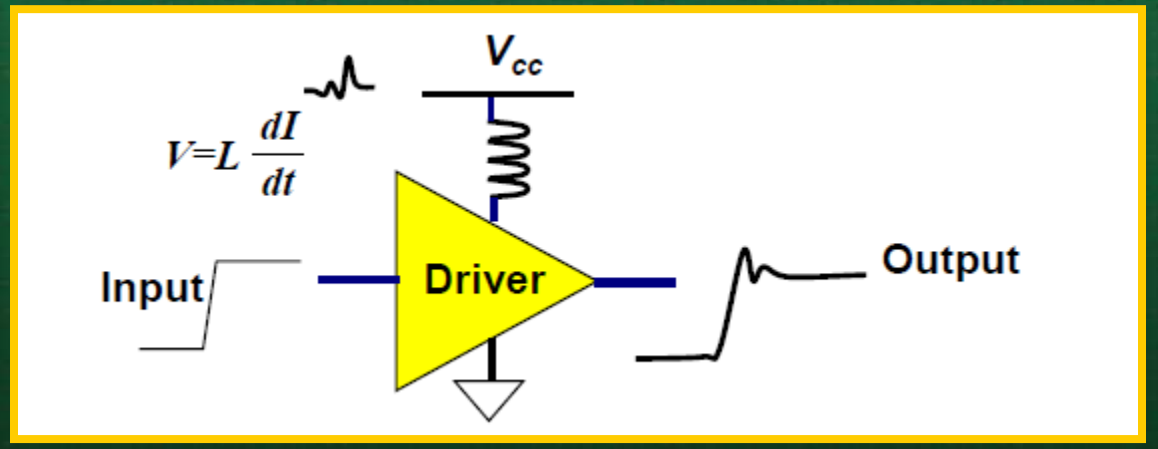
- Estimate contribution from PCB
- Estimate contribution from probes
- Estimate contribution of space-transformer
- Information needed
  - PCB DC resistance (either estimate or use SIwave)
  - Number of probes for a PWR Supply
  - Size of probes (diameter)
  - Probe material and its resistance.
  - Determine whether or not DC IR drop targets are met or not.

DC IR Drop Summary Report

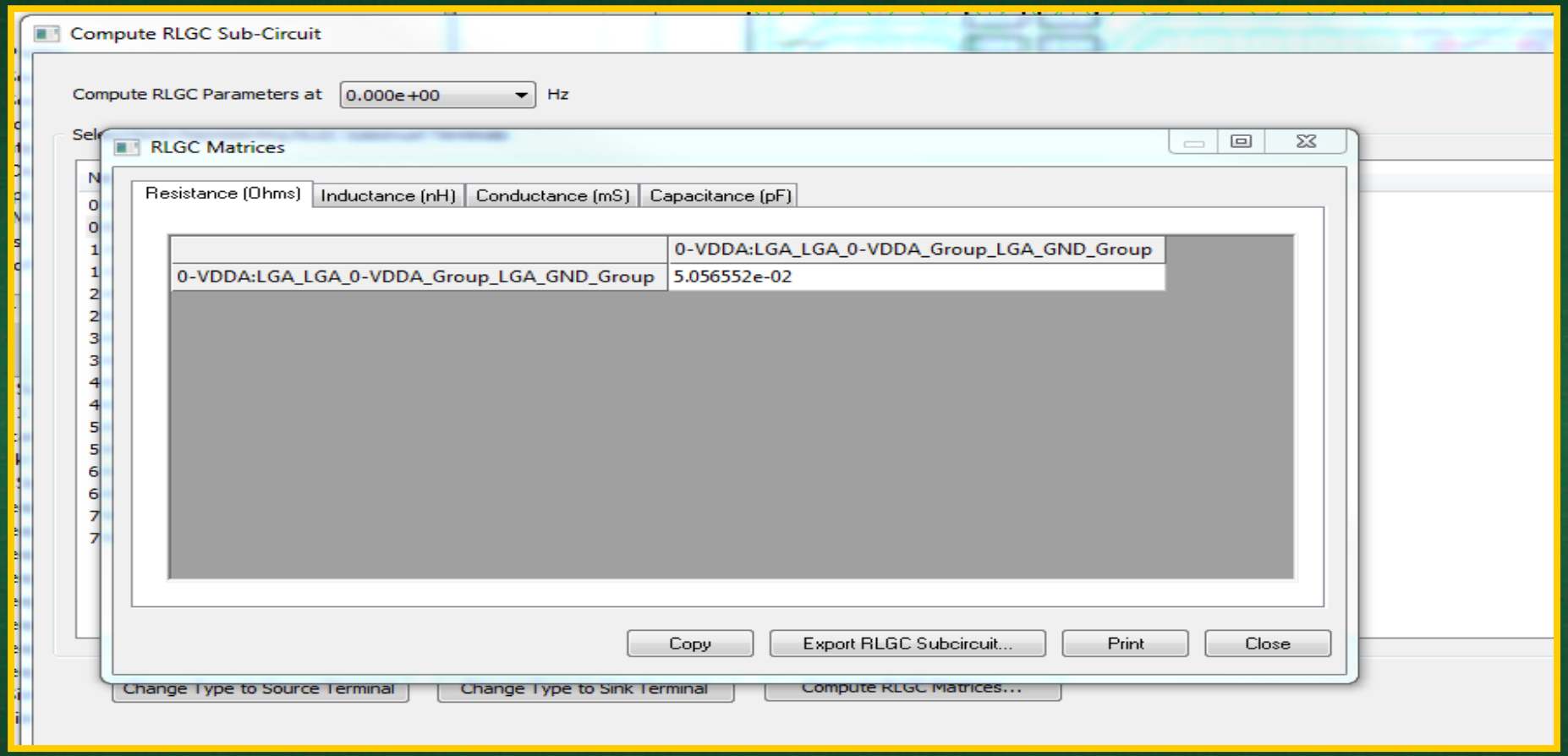
A	B	C	D	E	F	G	H	I	J	K	L	M
Supply name	Supply voltage	Max current supply (mA)	MLC LGA Pads	No. of PWR probes	DUT	MLC DC Resistance (Ohm)	PCB resistance estimated(Ohm)	Probe resistance estimated(Ohm)	Probe-card Total Resistance (Ohm)	IR drop (mV)	below 20mV (yes/no)	Comments
VDDA	4.2V	340	4	10	0	0.0505	0.01	0.0275	0.088	29.92	no	device design limitation,
					1	0.0501			0.0876	29.784	no	not enough VDDA pads, probes
					2	0.0502			0.0877	29.818	no	
					3	0.051			0.0885	30.09	no	
					4	0.0426			0.0801	27.234	no	
					5	0.0436			0.0811	27.574	no	
					6	0.0446			0.0821	27.914	no	
					7	0.0451			0.0826	28.084	no	
VDD	2.8	170	3	7	0	0.075	0.01	0.0393	0.1243	21.131	no	limitation due to number of probe
					1	0.0813			0.1306	22.202	no	less LGA pads
					2	0.0836			0.1329	22.593	no	
					3	0.0824			0.1317	22.389	no	
					4	0.09			0.1393	23.681	no	
					5	0.11			0.1593	27.081	no	
					6	0.104			0.1533	26.061	no	
					7	0.108			0.1573	26.741	no	
VDDD	3.3	20	1	2	0	0.208	0.01	0.1375	0.3555	7.11	yes	
					1	0.236			0.3835	7.67	yes	
					2	0.219			0.3665	7.33	yes	
					3	0.173			0.3205	6.41	yes	
					4	0.206			0.3535	7.07	yes	
					5	0.222			0.3695	7.39	yes	
					6	0.216			0.3635	7.27	yes	
					7	0.17			0.3175	6.35	yes	
V1V2	1.2	40	1	2	0	0.193	0.01	0.1375	0.3405	13.62	yes	
					1	0.251			0.3985	15.94	yes	
					2	0.277			0.4245	16.98	yes	
					3	0.231			0.3785	15.14	yes	
					4	0.193			0.3405	13.62	yes	
					5	0.255			0.4025	16.1	yes	
					6	0.282			0.4295	17.18	yes	
					7	0.228			0.3755	15.02	yes	

RLC Extraction

- **Tools used**
  - ANSYS SIwave
- **Instructions**
  - Setup ports on PWR supply with impedance = 0.1 Ohm
  - Extract S-parameters from DC to 1GHz
  - Extract R,L,C values at 100 MHz



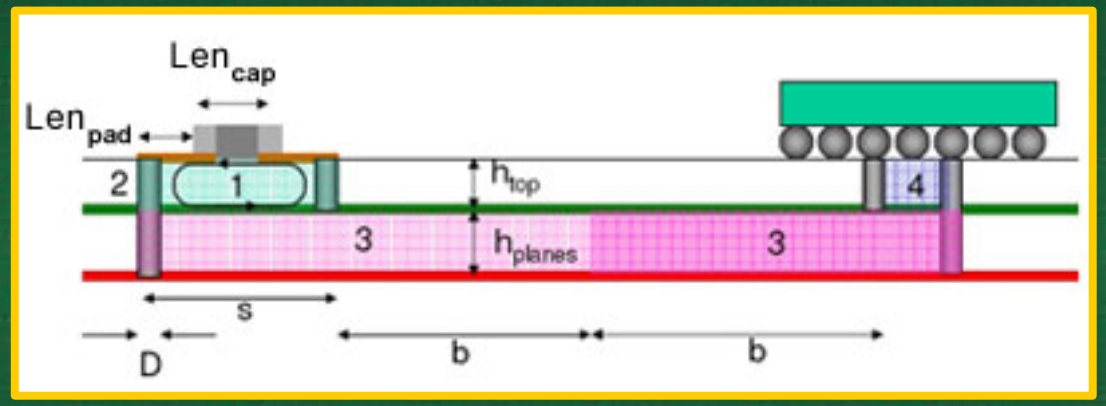
Compute RLGC for a PS



DC resistance can be estimated at 0 Hz
L,C can be estimated @ 100 MHz

Decoupling Capacitor Distance Estimation

- **Determine if location of decap mounting is close enough to DUT**
- **Determine loop-inductance of capacitors**



$$fres = \frac{1}{2\pi\sqrt{(Ldecap * Cdecap)}}$$

$$\lambda = \frac{c}{fres * \sqrt{\epsilon r}}$$

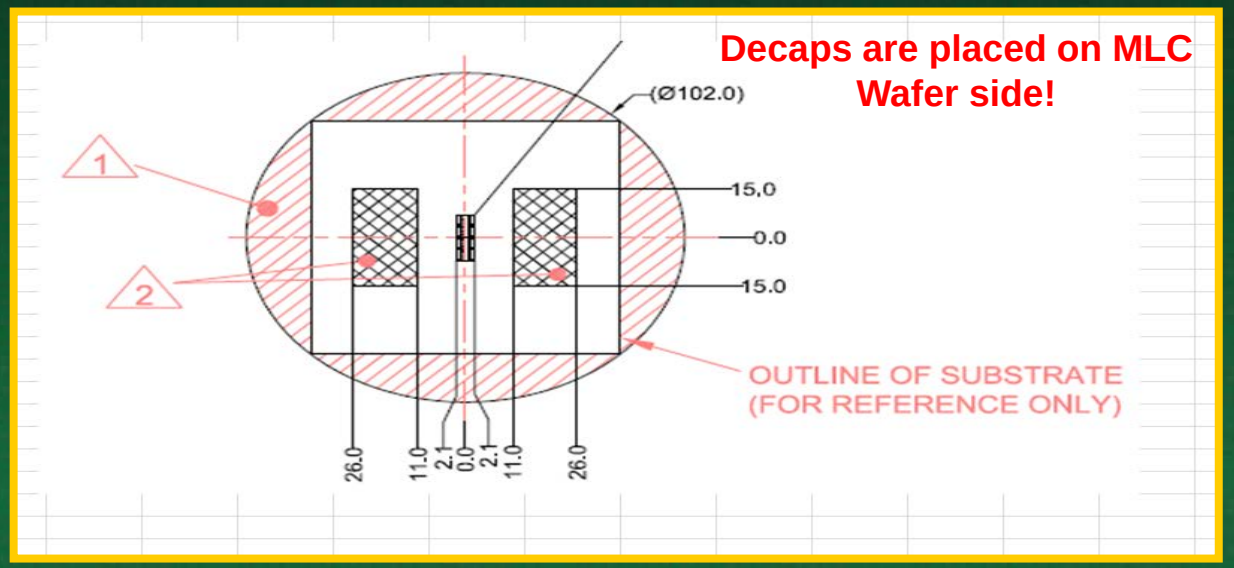
Lmnt = Ltrace + Lvia; Ldecap = Lmnt + Lpackage

Using mounting inductance and capacitor package inductance ➔ Resonant Frequency of a decap is determined

"To be effective decap needs to be placed within 1/40th of resonant wavelength*"

*Become a Decoupling Capacitor Network Guru, Part 2 (www.eetimes.com)

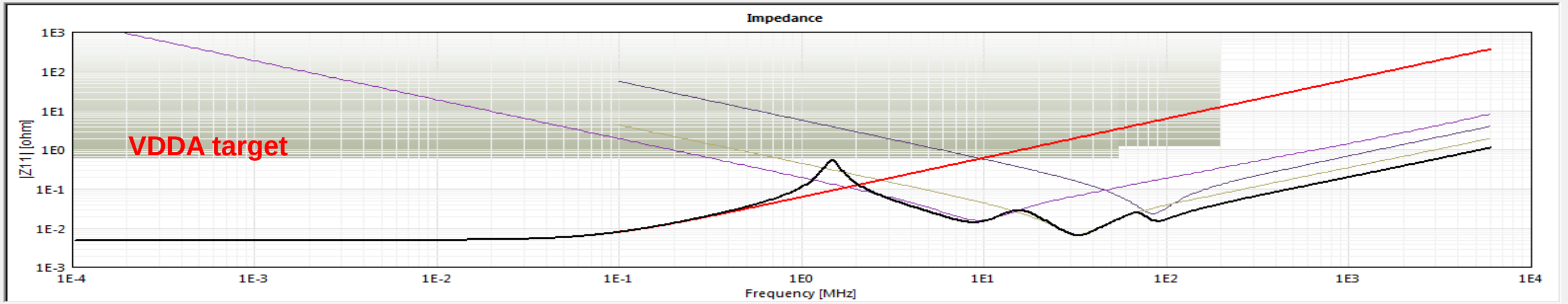
Decoupling Placement for Critical PWR Supplies



Capacitor	Capacitance Value (µF)	Resonant Frequency (MHz)	(λ/40) (placement distance to be less than λ/40)	Is placement distance OK ?
GRM033C81C104KE14D	0.1	38.04	62 mm	YES
GRM033C81A105ME05D	1	11.81	202 mm	YES
GRM033R71E103ME15	0.01	115.67	20.71 mm	YES

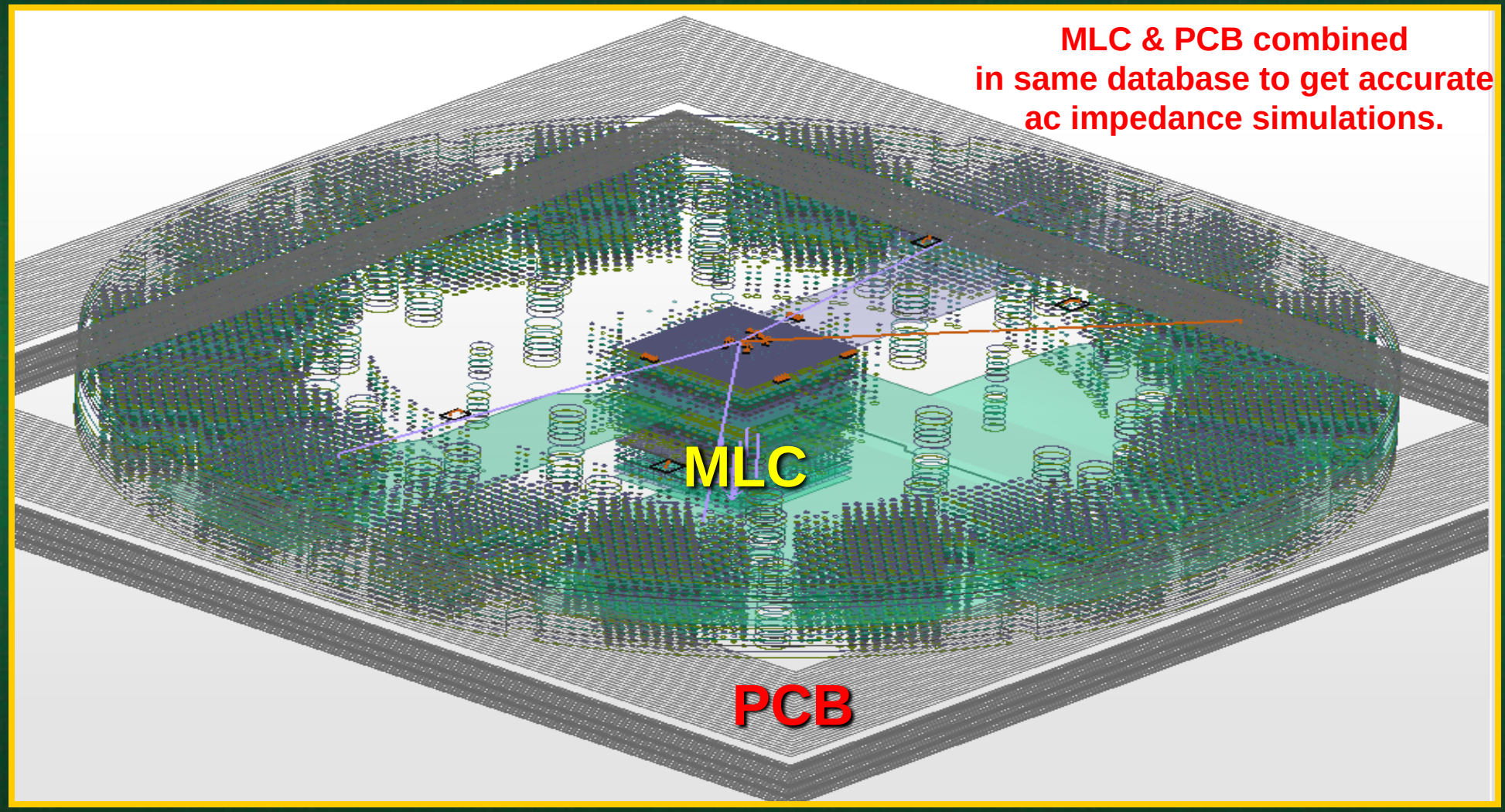
Estimating Required Decoupling Capacitance

Capacitor Library Browser

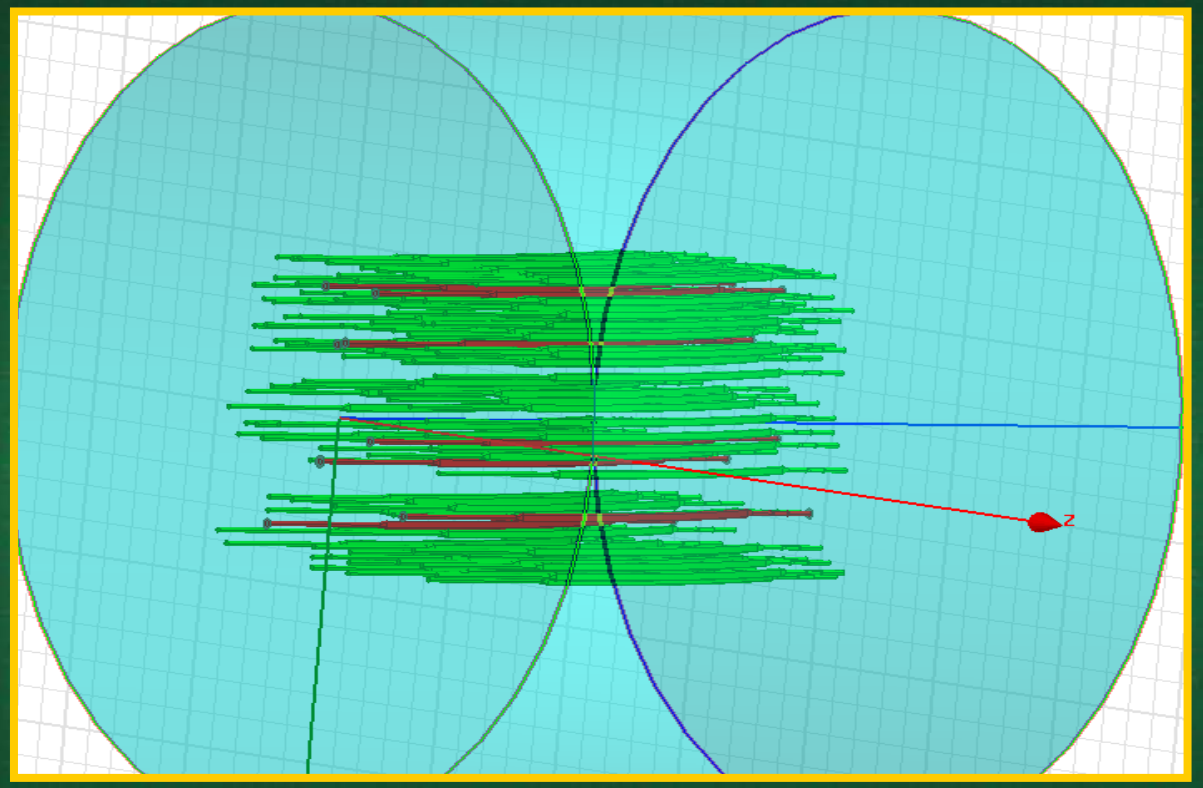


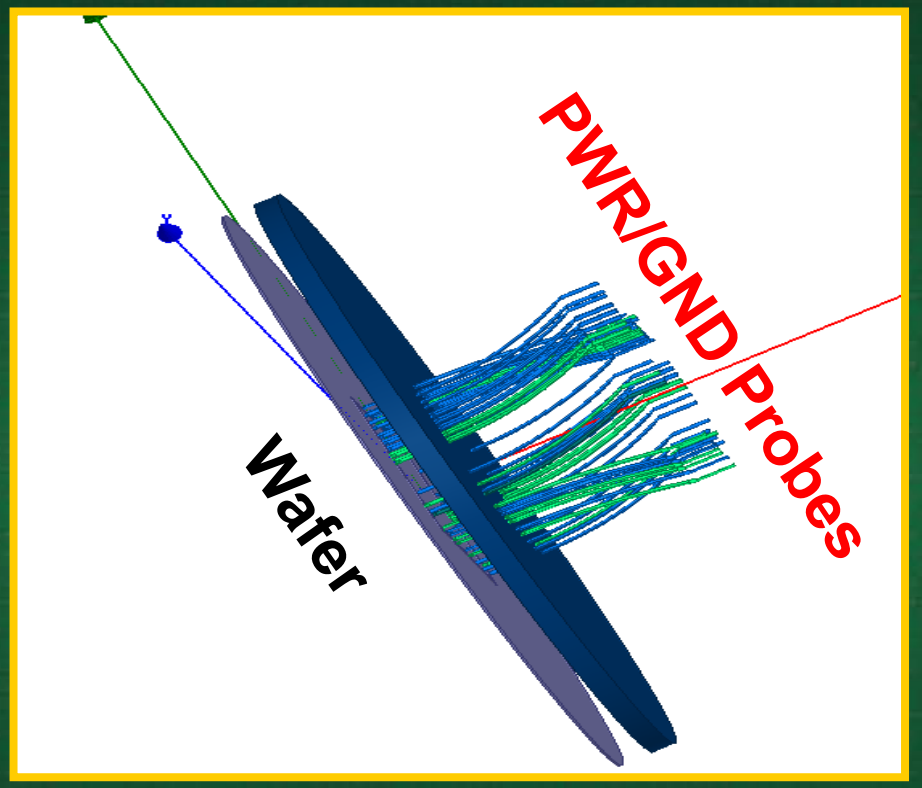
Vendor	Series	Part Name	Plot	Value (F)	# Acti...	EIA Size	Price	L_mnt (H)	R_mnt (ohms)	SRF (Hz)	S_min (dB)	ESR (ohms)	ESL (H)
Murata	GRM03	GRM033C81C104KE14	☑	1E-07	5	0201	0	1E-10	0.001	3.86457E+07	-69.1626	0.0347917	1.69605E-10
Murata	GRM03	GRM033R71E103KE14	☑	1E-08	3	0201	0	1E-10	0.001	9.92644E+07	-62.7637	0.0723518	2.57071E-10
Murata	GRM03	GRM033C80J105ME05	☑	1E-06	1	0201	0	1E-10	0.001	1.10361E+07	-76.2572	0.0153814	2.07975E-10
Murata	GRM03	GRM0332C1E271GA01	☐	2.7E-10	0	0201	0	1E-10	0.001	5.75544E+08	-58.1999	0.118707	2.83217E-10
Murata	GRM03	GRM0332C1E271JA01	☐	2.7E-10	0	0201	0	1E-10	0.001	5.75544E+08	-58.1999	0.118707	2.83217E-10
Murata	GRM03	GRM0332C1E331GA01	☐	3.3E-10	0	0201	0	1E-10	0.001	5.31221E+08	-58.4202	0.114097	2.72004E-10
Murata	GRM03	GRM0332C1E331JA01	☐	3.3E-10	0	0201	0	1E-10	0.001	5.31221E+08	-58.4202	0.114097	2.72004E-10
Murata	GRM03	GRM0332C1E391GA01	☐	3.9E-10	0	0201	0	1E-10	0.001	4.86643E+08	-59.1541	0.106636	2.74255E-10

PDN Analysis Strategy



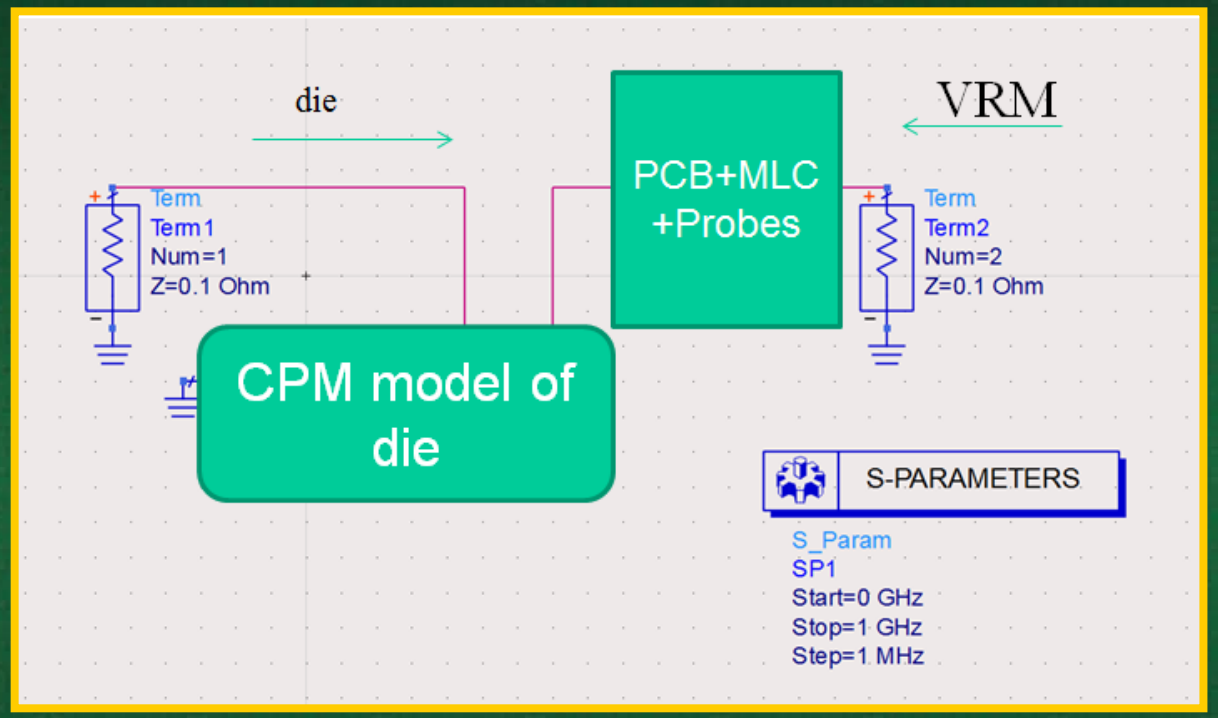
HFSS Analysis of Actual Probe Arrangement

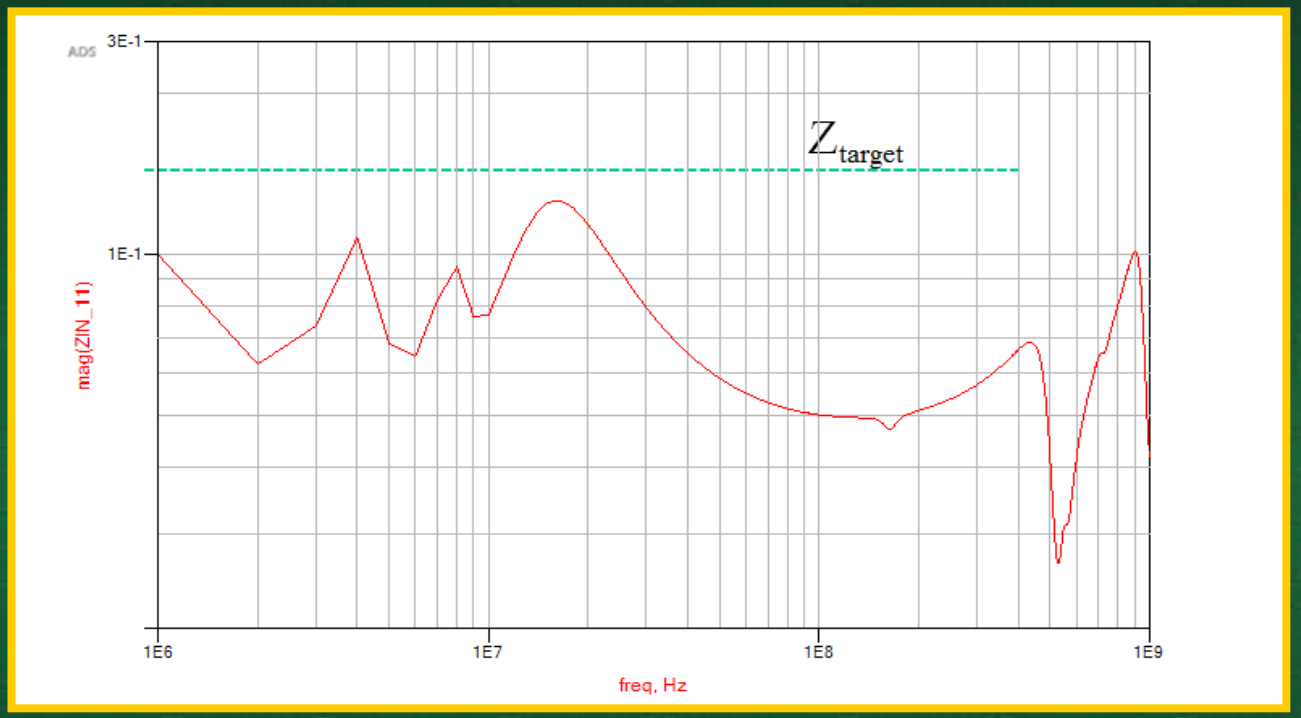




Actual probe layout is simulated in HFSS.
This will show any weakness in PDN

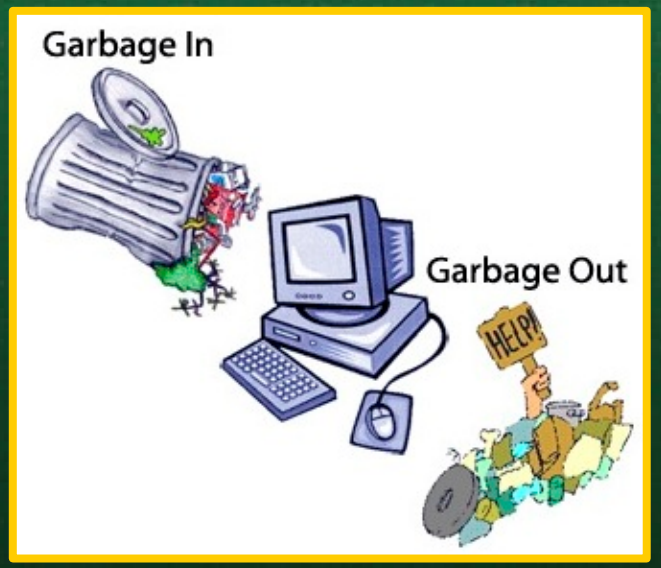
Building Full Channel for PDN (Including Die)





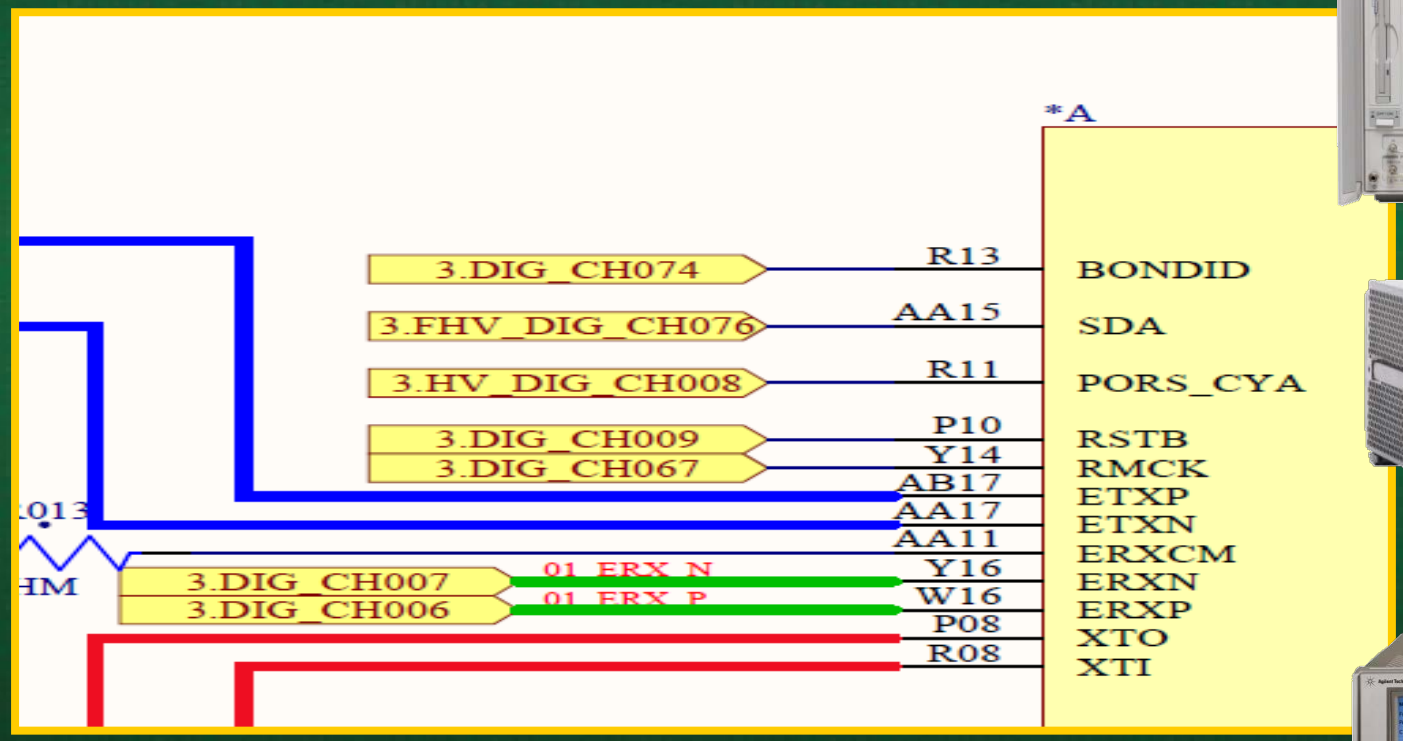
Correlating Simulations with Measurements

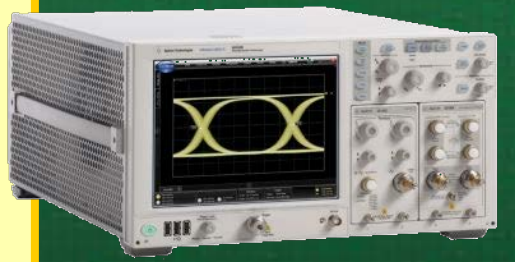
- **Simulations are prone to errors & can give wrong results…..**
  - Always know what will be the expected outcome from a simulation
- **Measurements are only as accurate as tools/setup/user…….**
  - VNA/TDR measurements can be tedious and time-consuming
- **Correlating Simulation with Measurements is important**
  - Saves time and resources
  - Confidence in simulations and measurements



S-parameters Measurements, Simulations & Correlation

- To measure electrical performance (3 dB bandwidth) of a differential pair on a Probe Card Assembly.
- The selected signals for measurement are (naming convention as per tester channel)
- 3.DIG_CH007
- 3.DIG_CH006





Measurement Setup

- VNA (HP 8720D 50 MHz to 20 GHz)
- 1250 µm Cascade Microtech probe
- 250 µm Cascade Microtech probe
- Calibration substrate
- Cables & other accessories
- Lab measurements : 50 MHz to 10.5 GHz

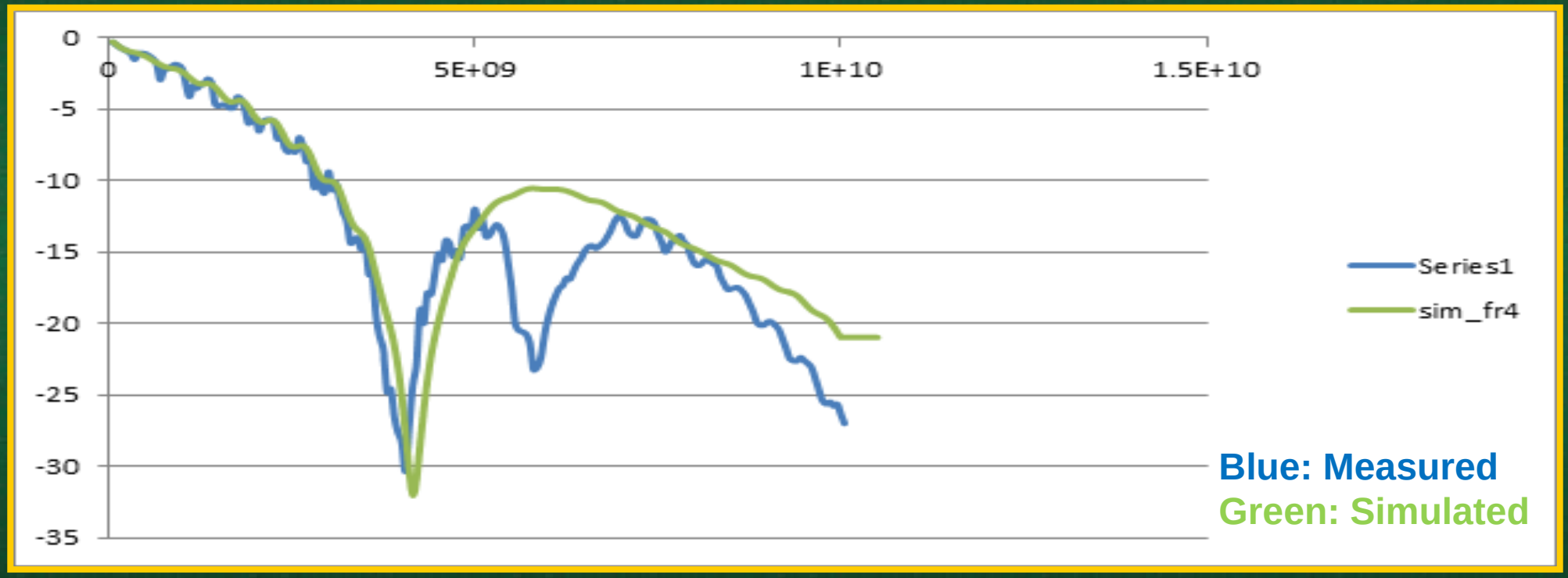
PCB Measurements

3.DIG_CH007

3.DIG_CH006

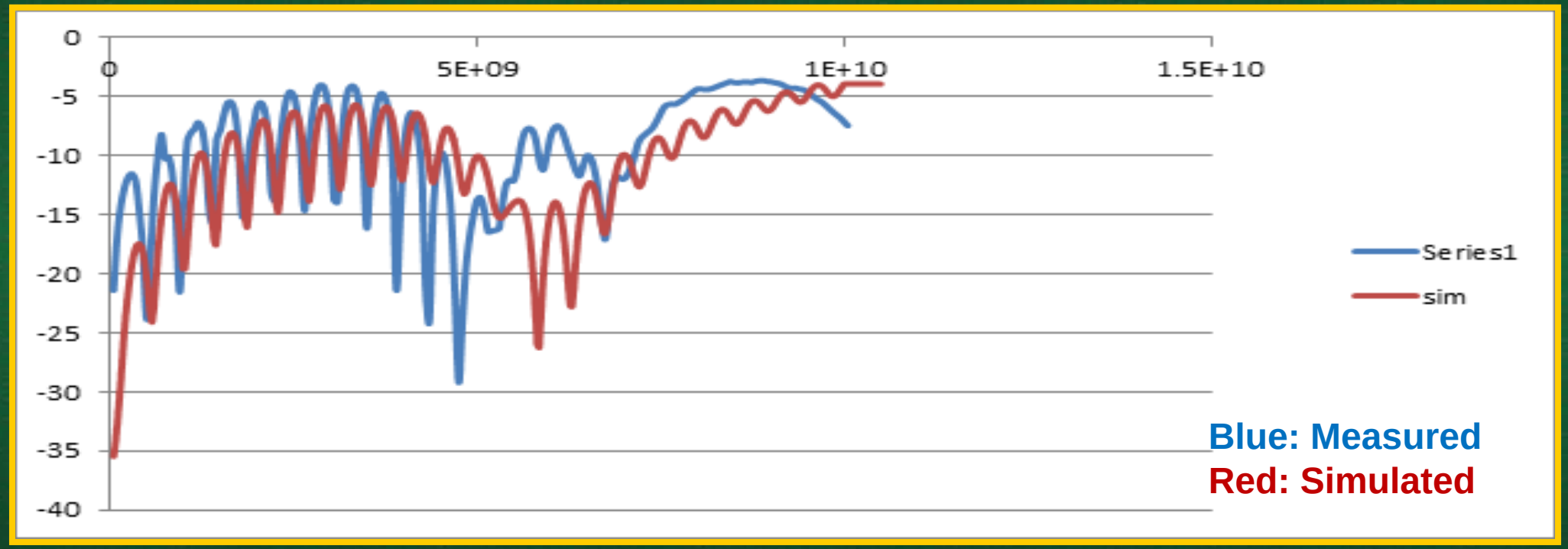
PCB S-parameter Correlation

Measurement Correlates well with Simulations



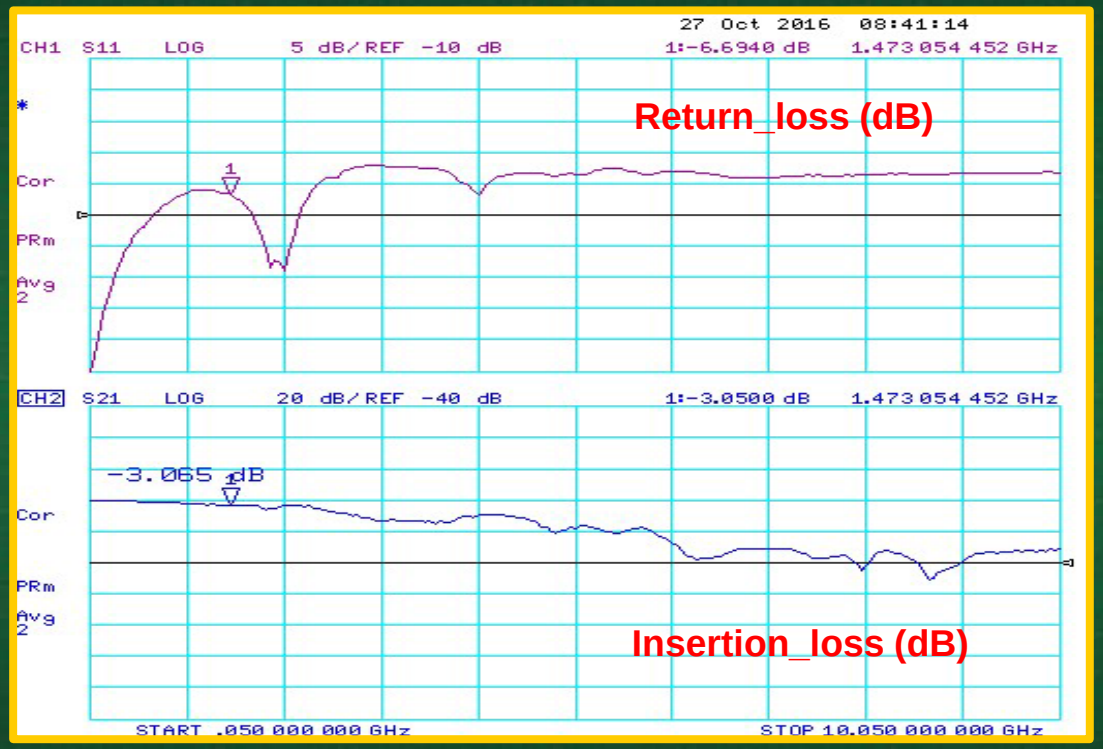
PCB S-parameter Correlation

Return_loss Measured/Simulated for ERXP

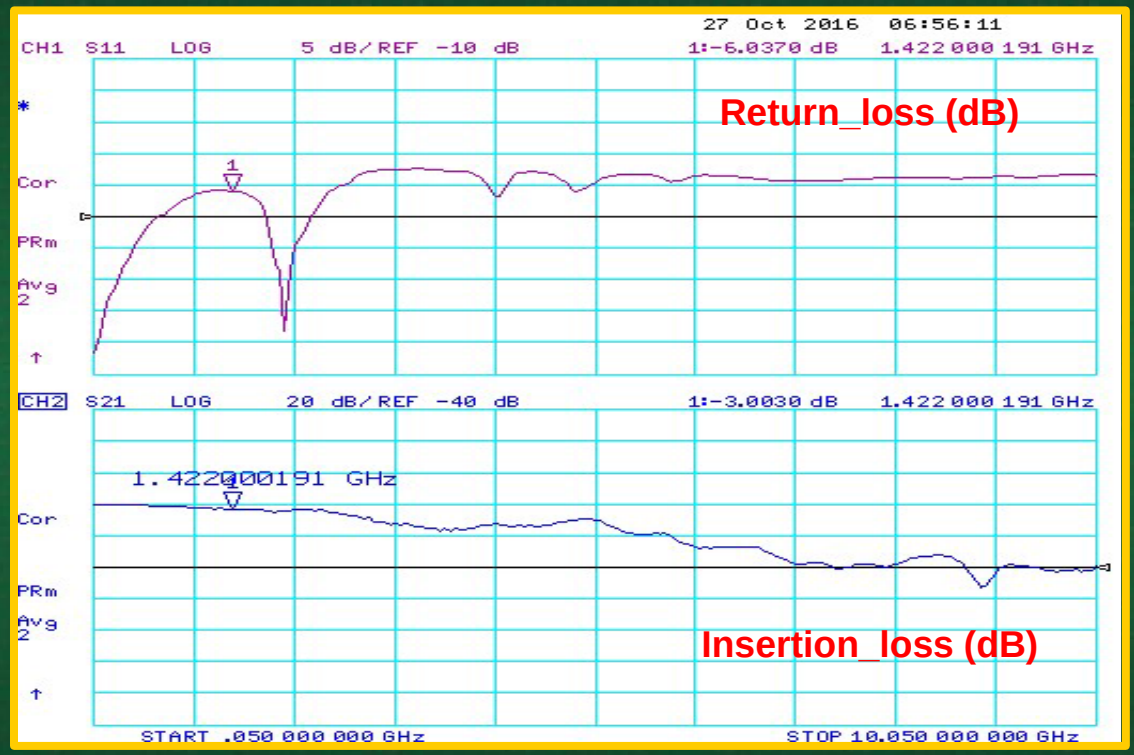


Space Transformer Measurements

3.DIG_CH007



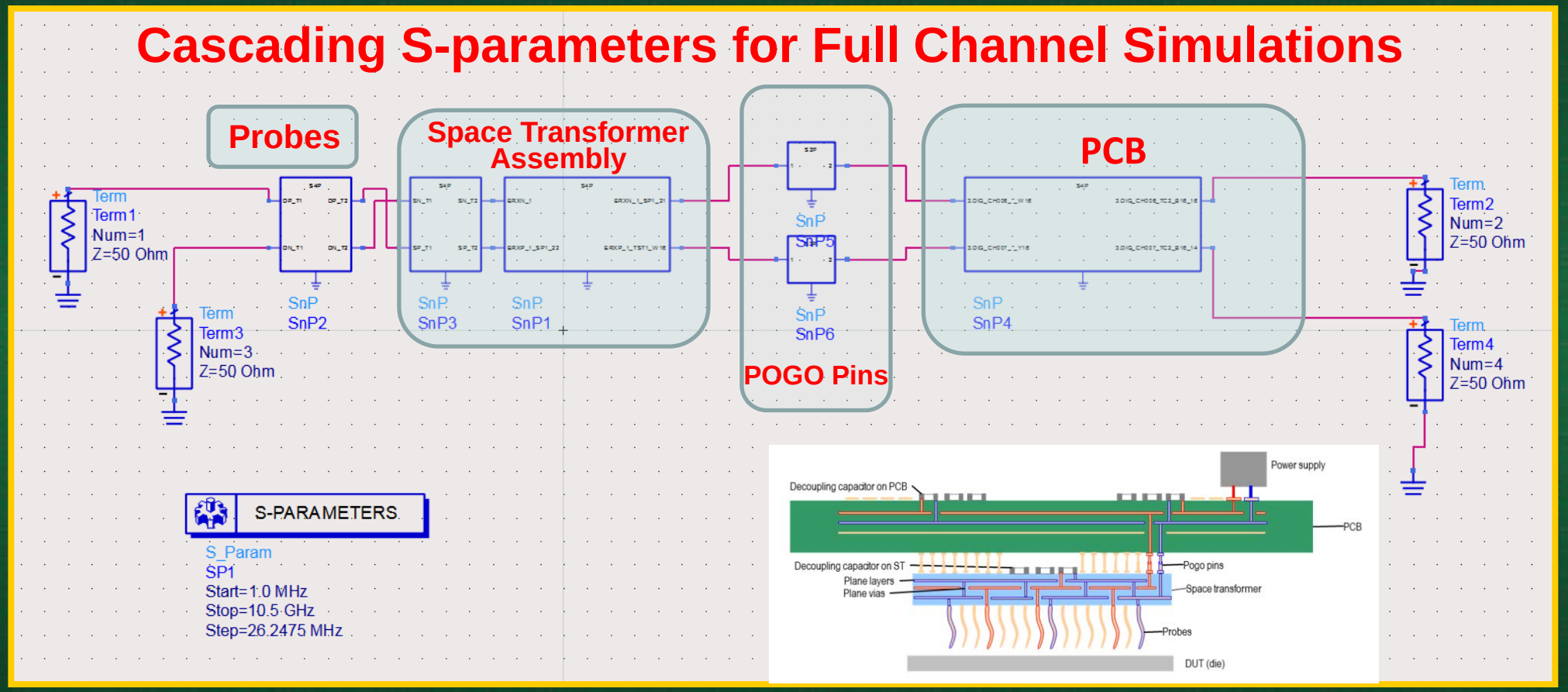
3.DIG_CH006



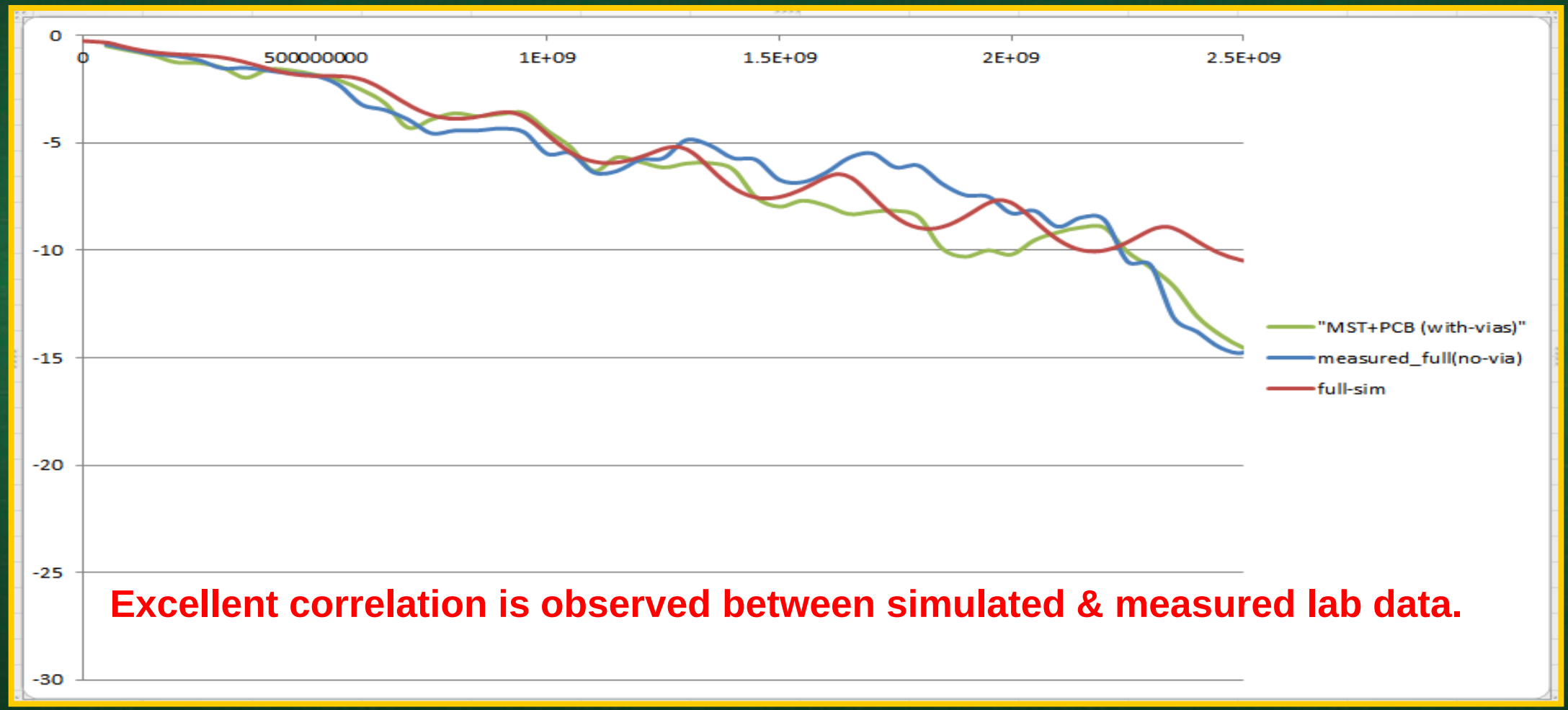
Full Channel Measurements

3.DIG_CH007 or ERXN

Full Channel Simulations vs Measurements Correlation



Full Channel Simulations/Measurement Correlation



Summary

- **Early & accurate simulation is key to improve electrical performance of probe cards.**
- **Accurate simulation results are obtained for controlled impedance structures in probe cards.**
- **Simulations correlate well with laboratory measurements.**
- **PCB insertion losses are dominant loss factor (roughly 50% of losses can be attributed to PCB routes); extra care should be taken during PCB routing.**
  - ❖ Reduce route lengths for critical signals
  - ❖ PCB stack-up should be optimized to reduce stub lengths on critical signals
  - ❖ For higher 3dB bandwidths low loss dielectric should be chosen

- ❖ **SI/PI co-simulation is necessary for designing high performance probe cards.**
- ❖ **Accurate simulations help reduce probe-card design time & this simulation methodology can be reused on various probe-cards.**

References

- **Principles of Power Integrity for PDN Design (1st Edition)**
  - Larry Smith & Eric Bogatin
  - Prentice Hall
- **Signal & Power Integrity Simplified (2nd Edition)**
  - Eric Bogatin
  - Prentice Hall
- **Board Design Resource Center (www.altera.com)**
- **Tools**
  - ANSYS HFSS, SIwave and Keysight ADS & SI/PI pro