SW Test Workshop
Semiconductor Wafer Test Workshop

HBM fine pitch micro pillar grid array probing evaluation

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Overview

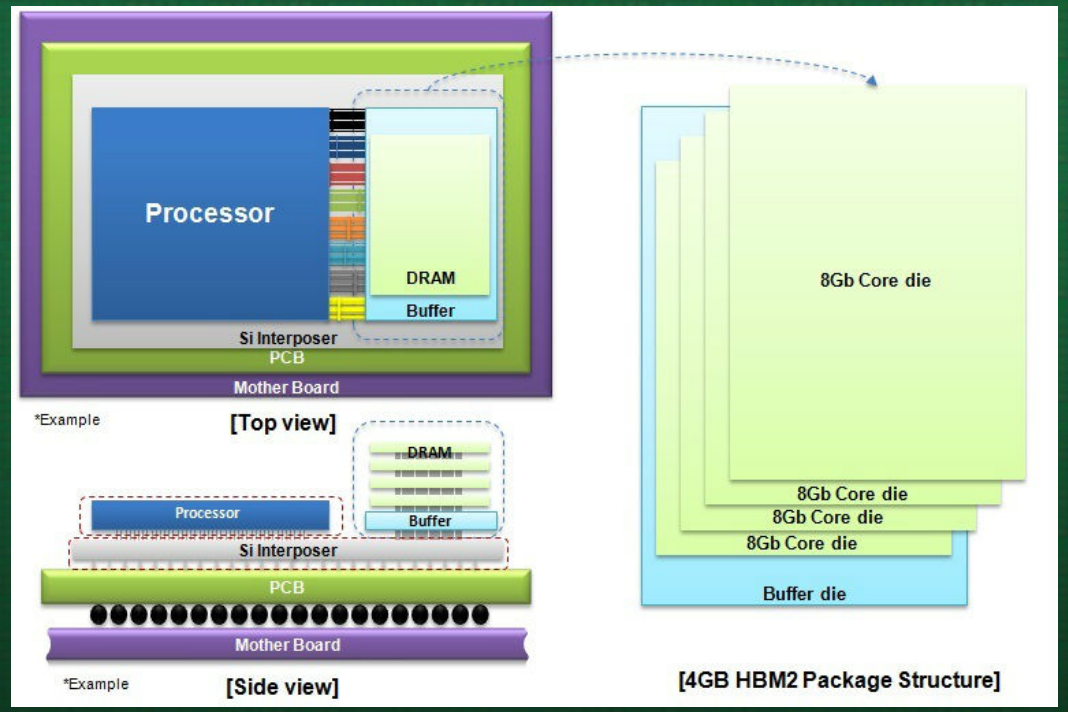
- Introduction
- HBM product description
- Technoprobe TPEG™ MEMS T50 probing solution
- HBM Probe Card (MPGA Contactor) description
- Testing wafers description
- Evaluation results
- Conclusions and next steps

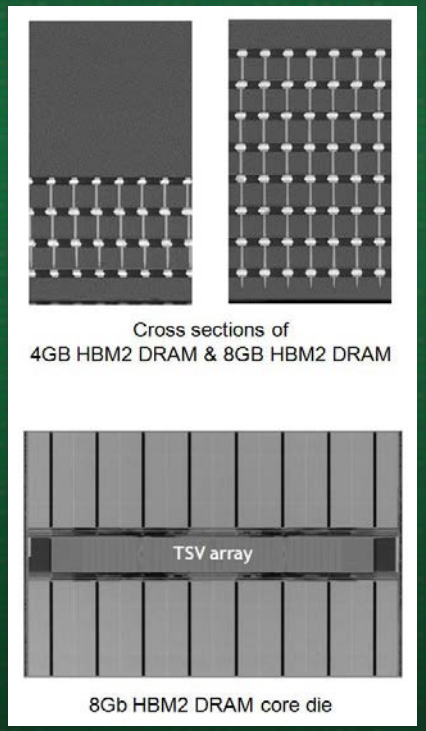
Introduction

- Samsung Electronics has announced the world first mass production of HBM2 in 2016.
- Technoprobe developed a specific probing solution for this application based on TPEG™ MEMS T50 probe technology and on high density MLO solution.
- Development and characterization of the full solution has been completely evaluated jointly with Samsung Electronics. Now Samsung Electronics is ready for bump testing with this solution.
- In this paper a description of the device requirements and Technoprobe probing solution will be presented and also characterization data will be provided and discussed in details

HBM2 product description

- **This state of the art 3D-stacked DRAM uses TSV technology and has grid array of 4942 microbumps at 55um pitch as its signal terminal.**
  - Until now, there was no proper solution for bump probing such a fine pitch and high density as well in the market.

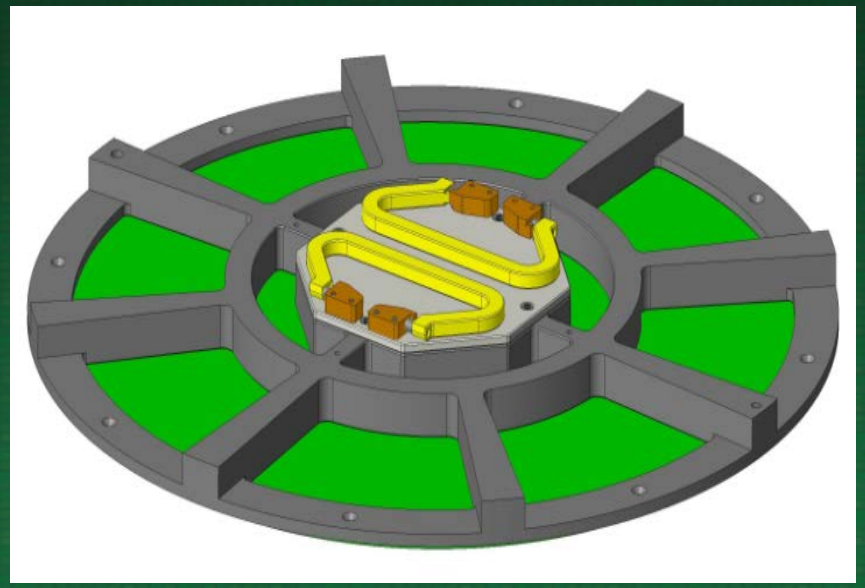




Technoprobe TPEG™ MEMS T50 probing solution

PARAMETER	TPEG™ MEMS T50
Needle diameter	1.25 mils equivalent
Tip shape	Flat
X, Y alignment accuracy and Z planarity	X,Y: ± 7 µm; Z plan: Δ 20 µm
Min pitch and configuration	50 µm Full Array
Pin Current (CCC)	350 mA (HC alloy)

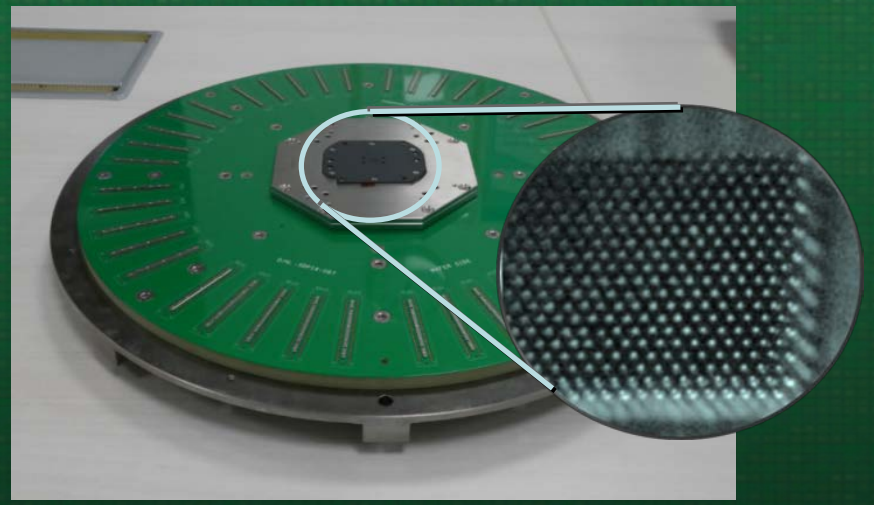
Fully populated MPGA Contactor Structure

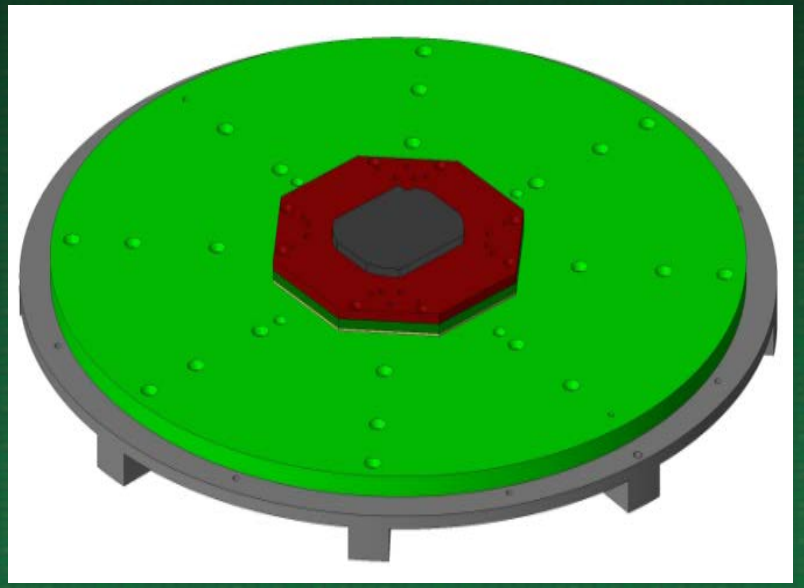


Tester Side View

MLO (Multi-Layer Organic) ST

Pitch converting 55→400 ㎛





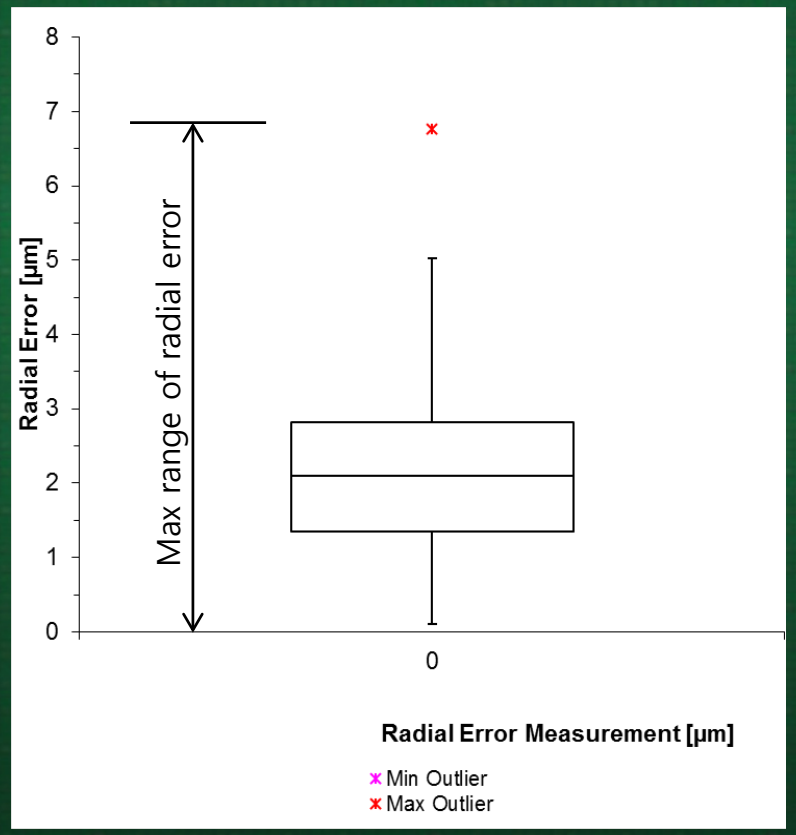
Wafer Side View

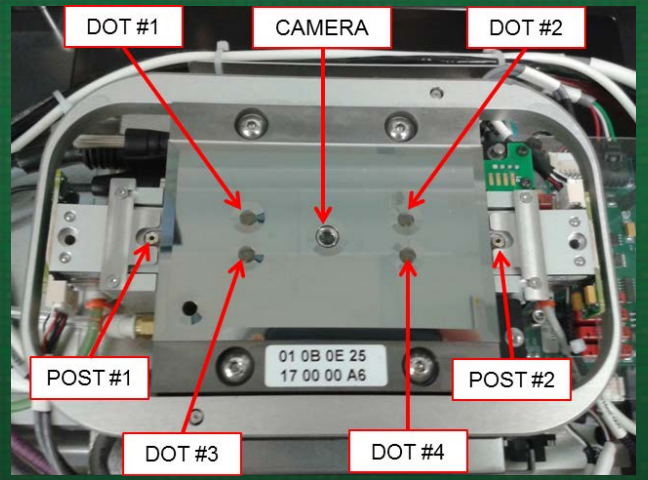
Evaluation Results Summary

#	Items	Method	Spec	Result	
1	**Alignment Error**	Measuring the radial alignment(X-Y) error on PRVX4	< 8µm	< 7µm	OK
2	**Contact Resistance**	Force V – Measure I method after remove internal path resistance	< 1Ω	< 0.3Ω	OK
3	**Planarity**	Measuring full loading planarity using conductive check plate on PRVX4	Δ20um	Δ9um	OK
4	**Probe Mark Area**	Measuring the PM area using Confocal Microscope at various OD(50,75,100um)	< 30%	< 20%	OK
5	**Height loss**	Measuring the bump height using CAMTEK Eagle-I at various OD(50,75,100um)	< 3µm	< 1µm	OK
6	**Current Carrying Capability (CCC)**	Measuring the CCC using ISMI '09	Max. 100mA	Max. 360 mA	OK
7	**Cleaning**	Measuring the Cres every 1K TD Compare between No cleaning and cleaning at 75um OD	-	Need to clean each 100 TD	-

Alignment Error

- **Measuring X-Y Alignment of needles using Vision method for all pins (Nominal pitch 55um)**
  - Calculate the alignment error using Radial Alignment Error between ideal position and real position
  - Imaging process using PRVX4 check plate with 10um OD (All needles scan)
  - Measuring result : Max 7um ➔ Spec in(< 8µm)

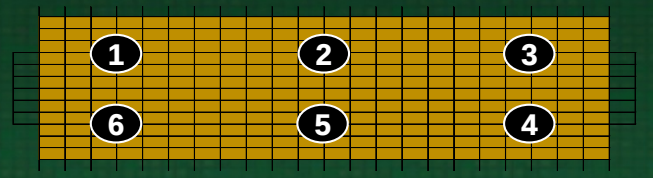


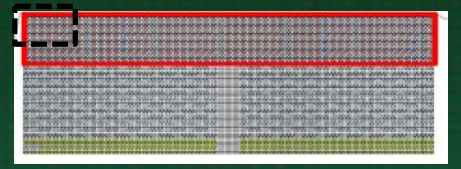


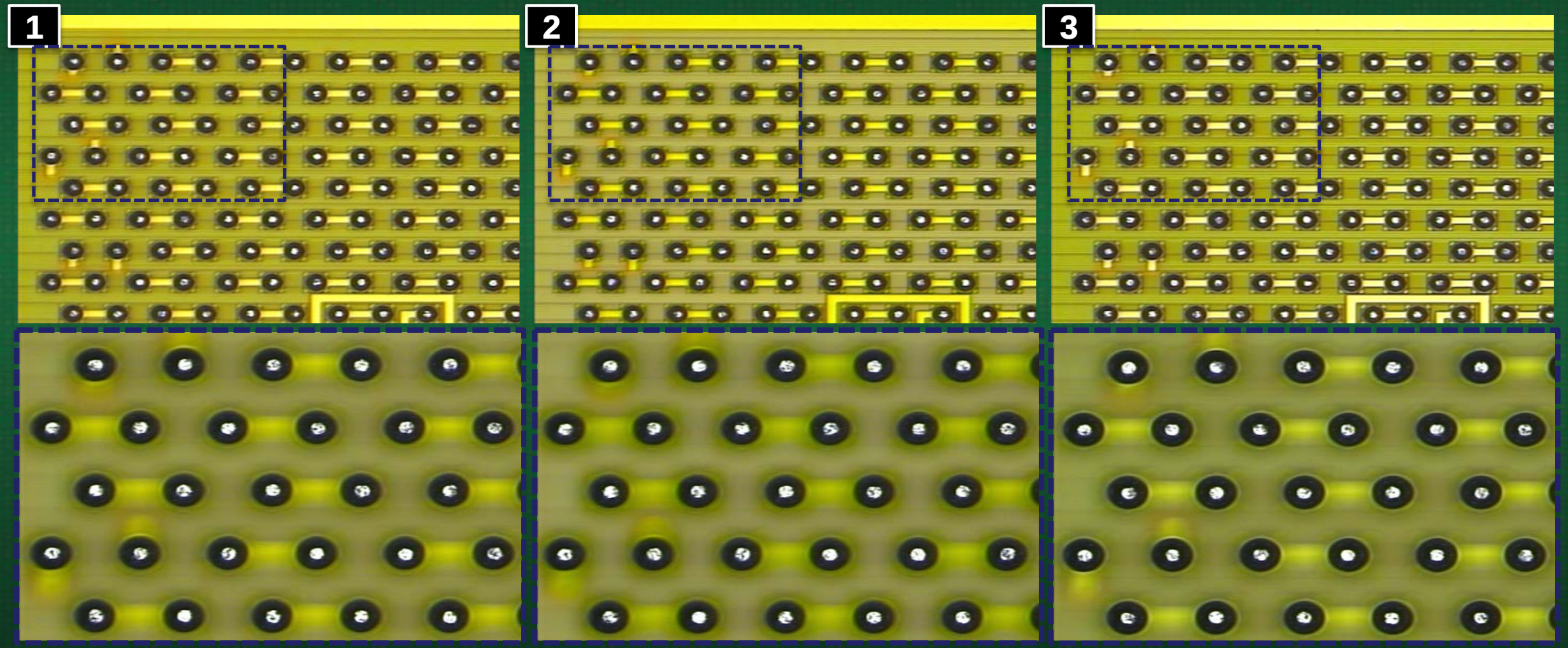
PRVX4 check plate

Alignment Image @ OD 75um

- Prober camera is used to inspect the probe marks through the wafer

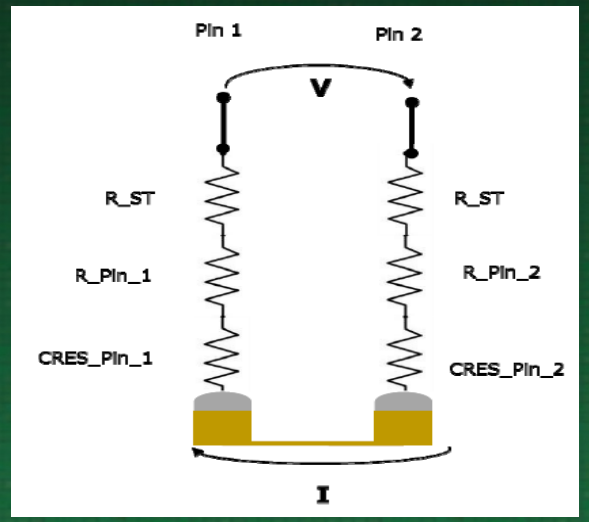






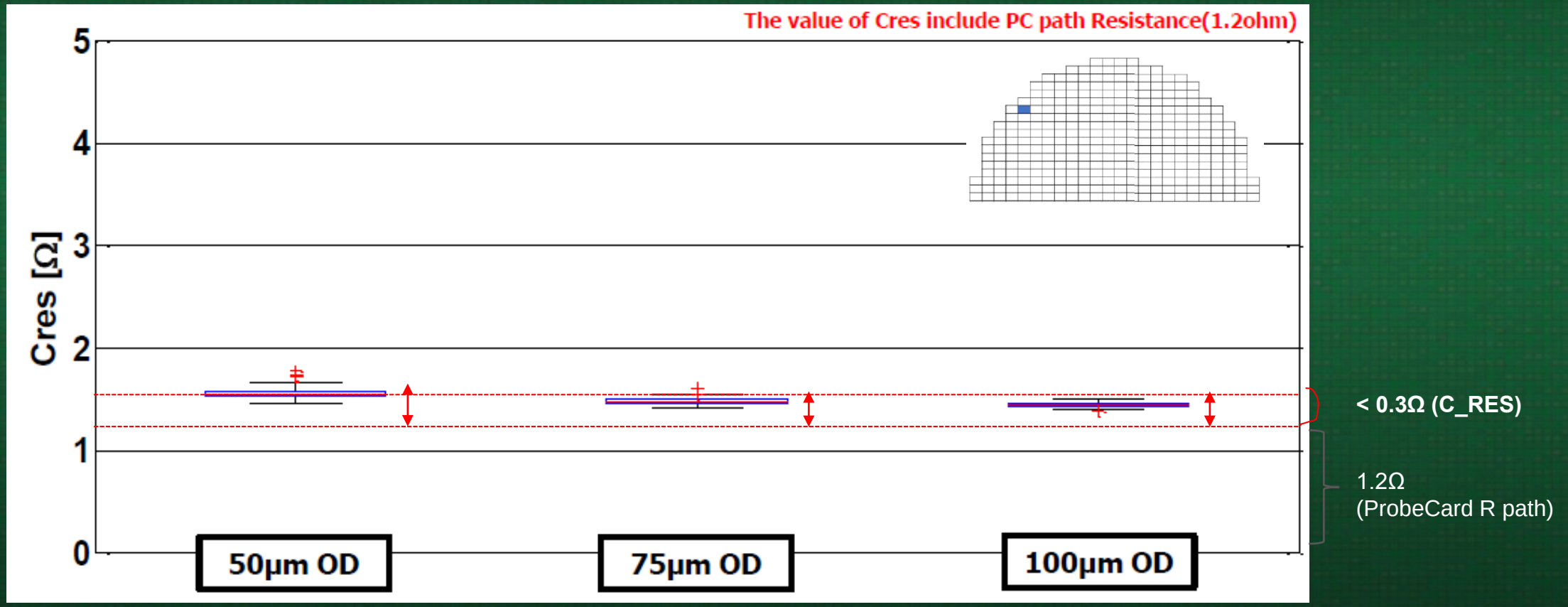
Contact Resistance (CRES) Setup

- **Contact Resistance (C_RES) Measuring Method**
  - Force V = 10 mV , Measure I (Clamp I = 50 mA)
  - 48 pins measured (24 pairs)
  - R probe = 0.5x R Pair = 0.5 x (V/I)
  - Plot of 24 C_RES values for each touchdown
- **H/W setup**
  - Wired space transformer PC
  - Measuring PC Path Resistance
  - In this setup, Path Resistance (PCB Pattern + WST + probe) : 1.2Ω
- **Measuring results**
  - Spec in for OD 50~100 µm
  - Max Cres = 0.3 Ω (Spec = under 2Ω)



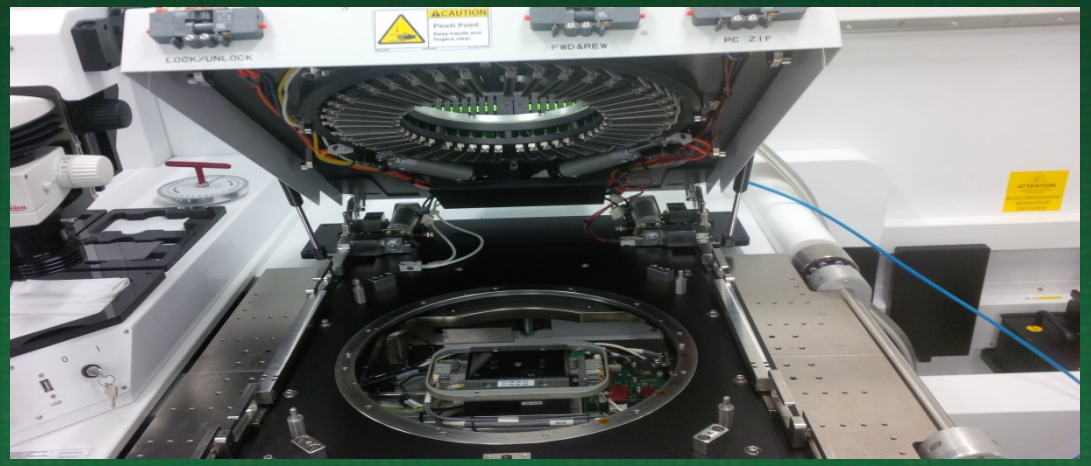
Contact Resistance (CRES) Results

- **Contact Resistance @ different Ods**
  - Measuring Result : Spec in for OD 50~100um
  - Max Cres = 0.3Ω - (Spec = under 2Ω)

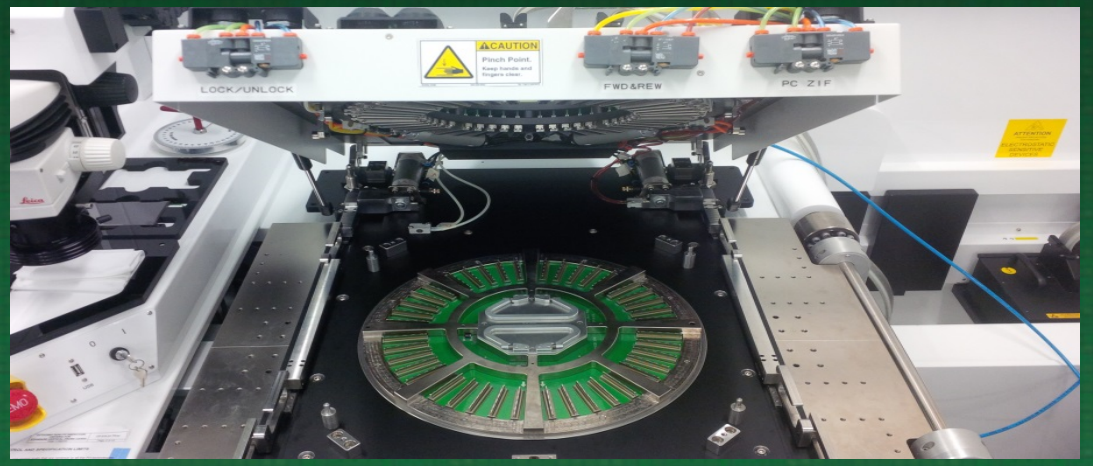


PRVX4 Setup

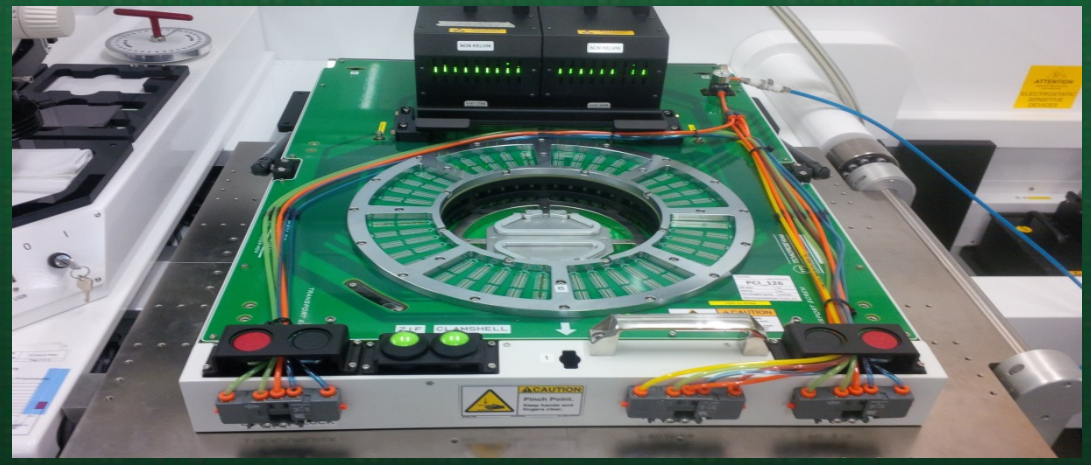
Motherboard (MB) docked on PRVX4



Probe card loaded on MB



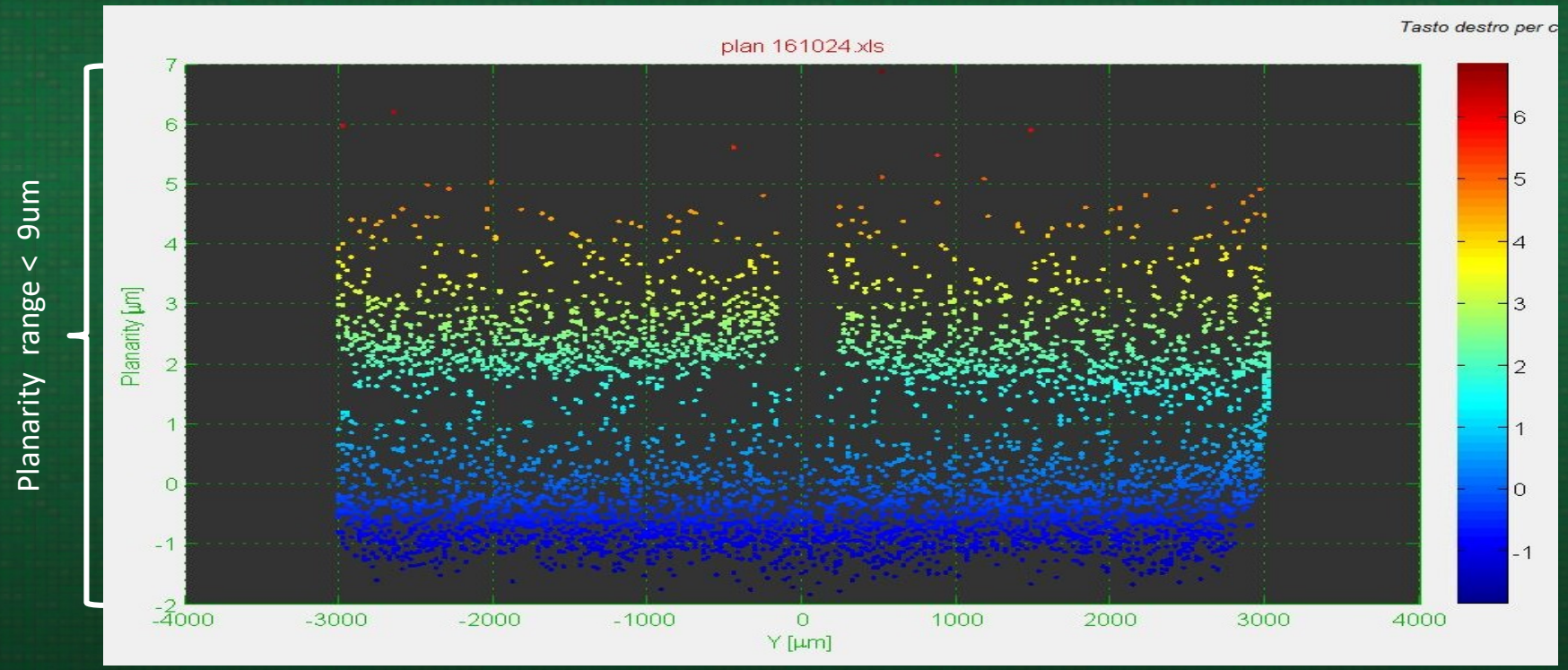
MB and PC under test



PrecisionWoRx VX4
- Standard Certification system for P/card
- Outgoing test with PRVX4 for all P/Card

Unloaded Planarity

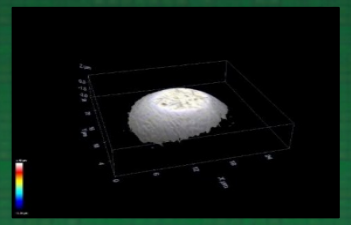
- Unloaded planarity is found using a conductive post, loading one probe at a time
- Electrically non-connected pins are tested mechanically, measuring the Z-quote corresponding to a given mechanical reaction force applied by the post needle
- Testing conditions : Testing voltage : 5V, Maximum testing over travel : 100 µm
- Measuring Result : Max Δ = 9 µm - Spec in (Δ 20 µm)



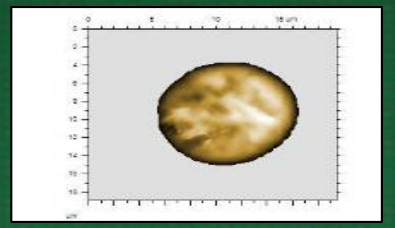
Probe Mark Area

- **Made 4942 full probe pin populated Probe Head, Measured Cres using Daisy Chain Wafer**
  - Probe marks area inspection via confocal microscope at different OD = 50, 75, 100um
  - Each die 30 µbumps are inspected. Confocal microscope is used to obtain a 3D image of bump top surface
  - Measuring Result : Max 20% - Spec in (≤30%)

OD	Average PM area	SD	MIN	MAX
50µm	14.4%	1.1%	12.6%	16.7%
75µm	16.6%	1.0%	14.7%	19.2%
100µm	17.9%	1.3%	15.8%	20.3%

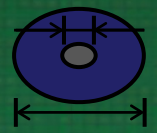


Confocal Microscope 3D image



Bump slicing to calculate probe mark area

Probe Mark Area = $(a/A)^2$



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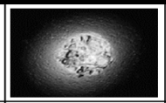
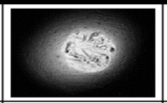
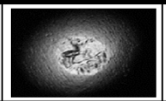
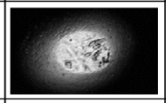
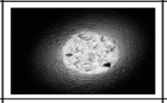
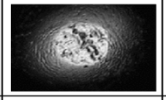
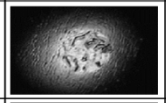
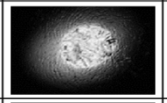
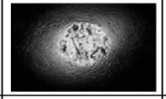
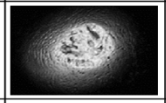
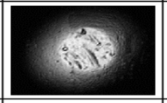
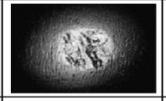
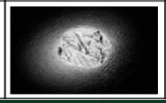
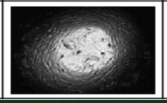
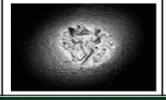
Bump n°1		15.5 %	Bump n°6		16.1 %	Bump n°11		16.1 %
Bump n°2		15.9 %	Bump n°7		16.0 %	Bump n°12		16.9 %
Bump n°3		15.9 %	Bump n°8		16.6 %	Bump n°13		16.3 %
Bump n°4		17.1 %	Bump n°9		15.9 %	Bump n°14		16.8 %
Bump n°5		16.3 %	Bump n°10		17.2 %	Bump n°15		17.0 %

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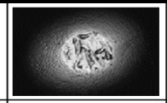
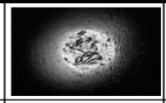
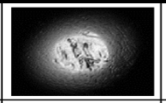
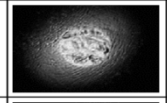
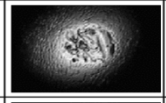
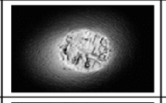
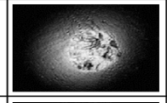
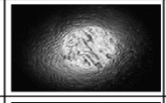
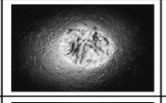
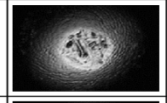
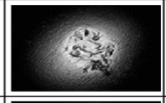
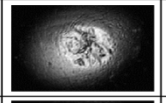
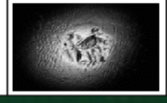
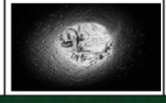
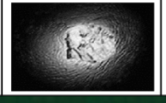
Bump n°16		16.3 %	Bump n°21		16.9 %	Bump n°26		15.0 %
Bump n°17		14.7 %	Bump n°22		18.2 %	Bump n°27		16.9 %
Bump n°18		15.7 %	Bump n°23		18.8 %	Bump n°28		16.9 %
Bump n°19		17.4 %	Bump n°24		19.2 %	Bump n°29		16.1 %
Bump n°20		16.2 %	Bump n°25		17.0 %	Bump n°30		18.1 %

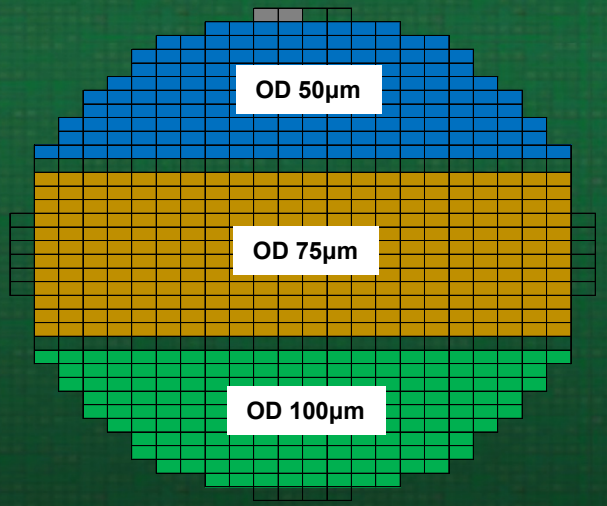
Probe Mark Images @ OD 75um

Height Loss

Measure Bump height before and after Probing

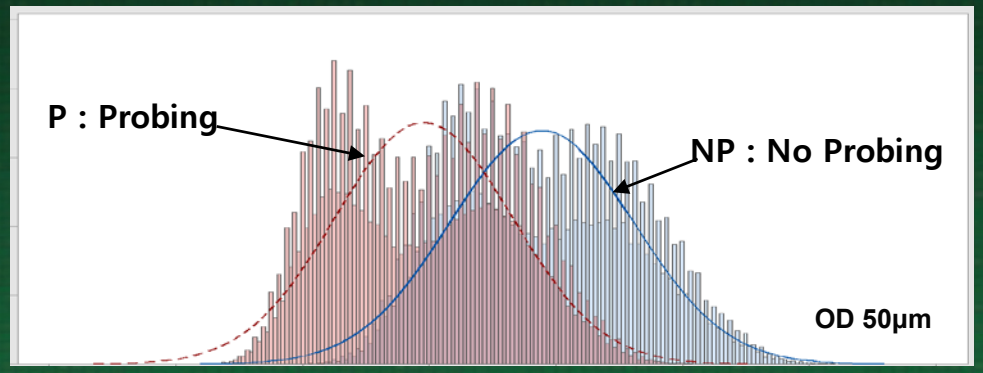
- Compare Bump Height @ different OD
- Sample size: 20dies (98,840bumps)
- Measuring Equipment : CAMTEK / Eagle-I
- Max under 1um → Spec In (≤3um)

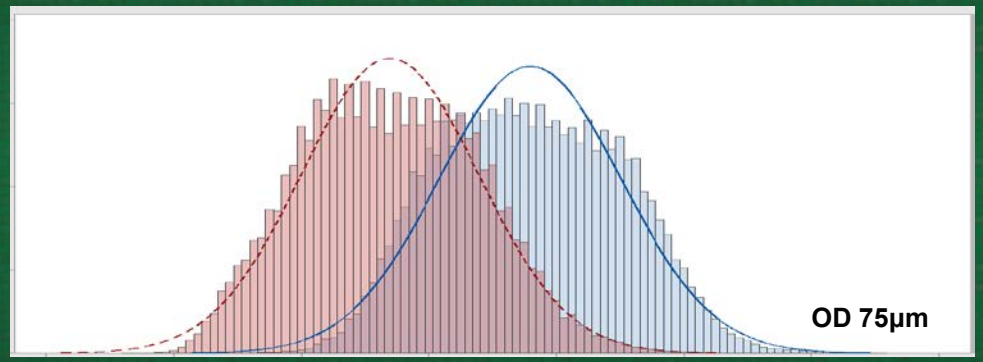
※ **3 Zones : 50,75,100um** (Typical OD[1] : 75um)

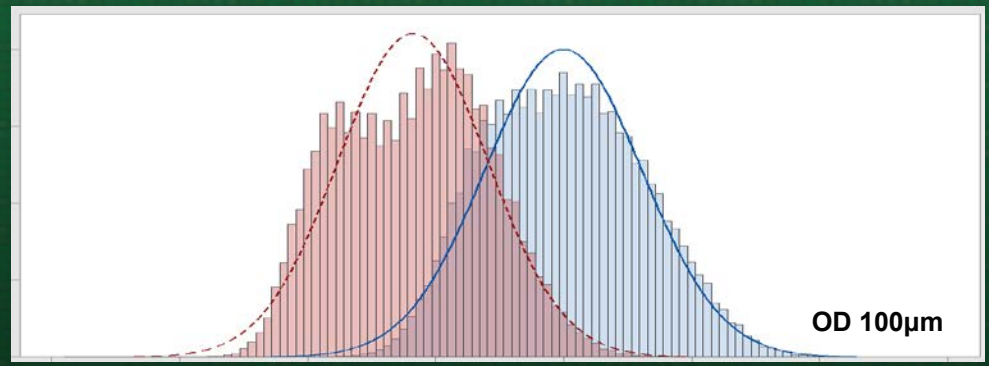


unit : μm

OD	Height Loss	Average	
		NP	P
50	0.75	38.32	37.57
75	0.88	38.24	37.36
100	0.94	38.40	37.46



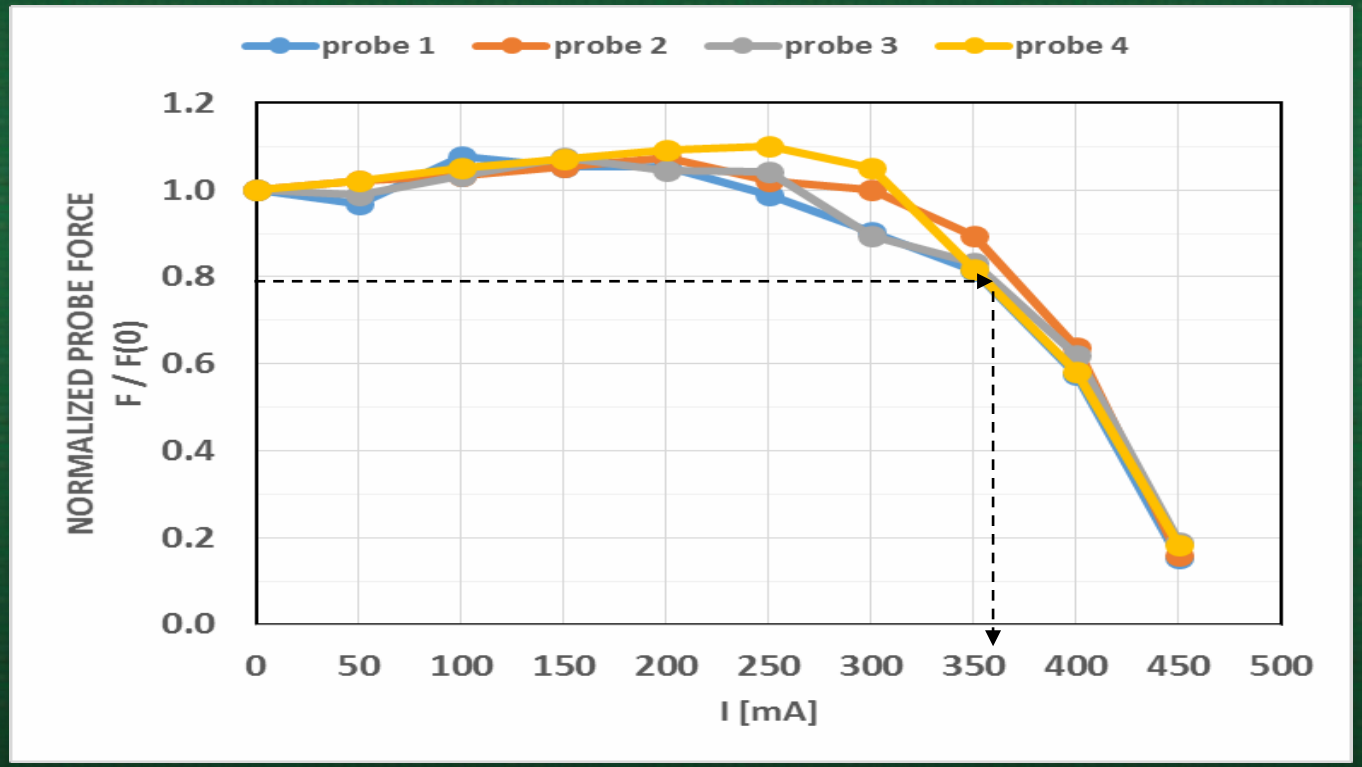




Current Carrying Capability (CCC)

Standard Method : ISMI (‘09)

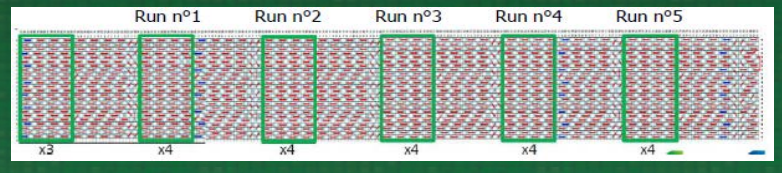
– In this PH 4 needles are measured: CCC(mean) = 360 mA

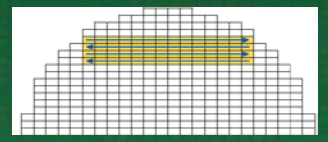


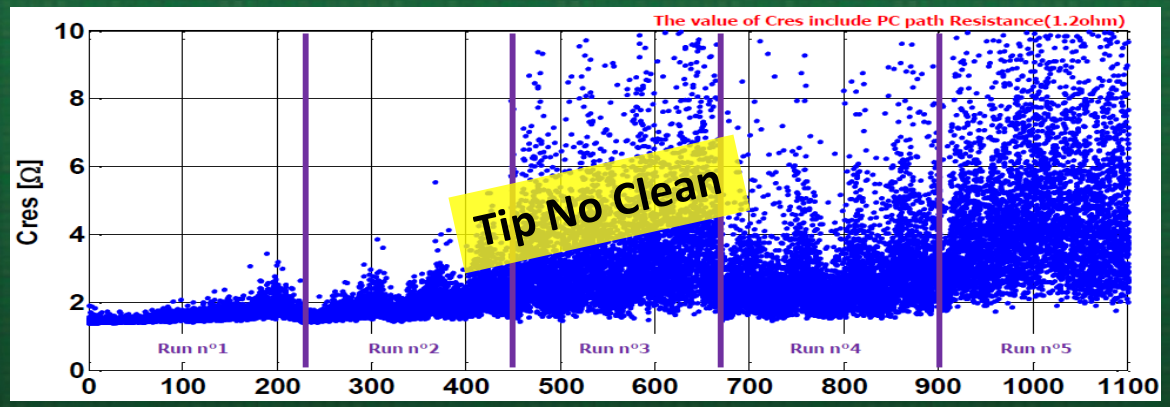
Cleaning

☐ **Contact resistance variance during TDs without cleaning**

- Total 1120 TDs @ 75um OD , Measuring 24 C_RES every TD
- 5 Times measuring(224 TD) using parts of Daisy Chain wafer
- C_RES discontinuity ➔ Because of Die Realignment.



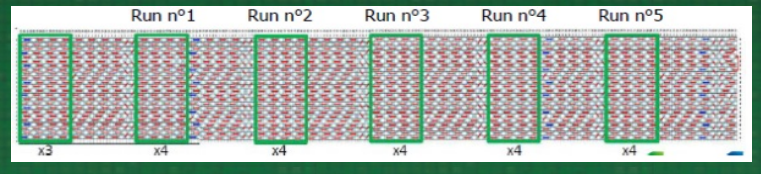


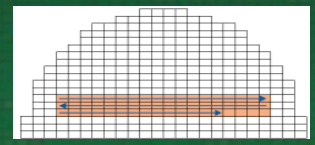


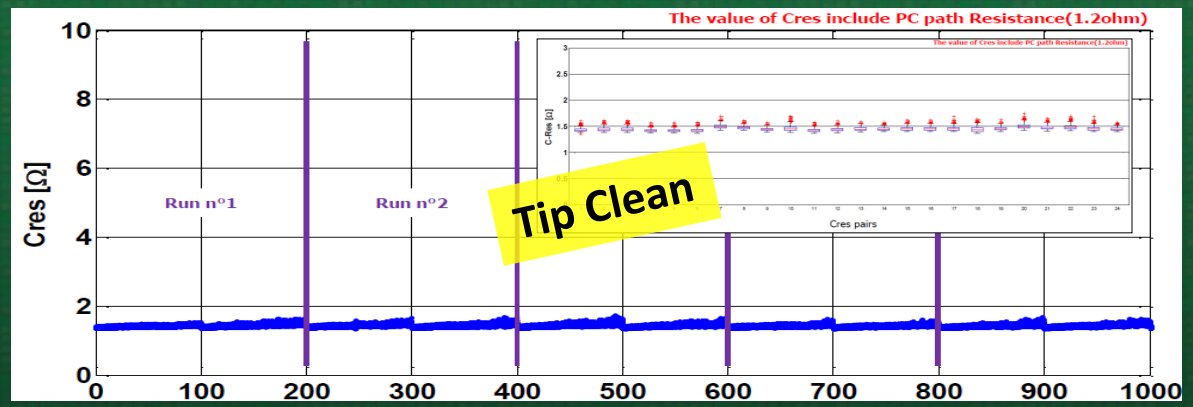
✓ **Consistently increase Cres with more TD**

☐ **Contact resistance variance during TDs with cleaning**

- Total 1120 TDs @ 75um OD , Measuring 24 C_RES every TD
- 5 Times measuring(224 TD) using parts of Daisy Chain wafer
- **Probe tip Cleaning : each 100TD:** 3M pink paper, X-Y movement (30 μm L pattern), Cleaning OD: 30 μm







✓ **Could keep the Stable Cres with claning**

Conclusions and Further Study

- **We proved HBM package test (DC/functional) is possible probing directly all micro bumps**
- **Fine Pitch 55um package has no conventional socket solution**

  Probing solution is a good alternative such a fine pitch package

- **Next steps**
  - Multi parallel and high speed should be improved for mass production
  - High yield, high density, fine pitch space transformer solution needed
  - Probe mark's effects on soldering processing in 2.5D package need to be evaluated

Thanks for your Support !

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