Hybrid MEMS Probe Design to Maximize Electrical & Mechanical Wafer Test Performance

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Agenda

- Overview
- Challenge
- Approach-Optimized Solution
- Trade-off Analysis
- Implementation/Design Challenges
- Issues/Next Steps
- Summary
Overview

- Industry leading minimum CuPillar pitch is currently at 70 -100um

- Drivers for Pitch Scaling are:
  - Scaling : Die Area
  - Increased functionality -> Higher IO’s count
  - Power Integrity  -> Higher Vdd/Vss bump count
  - Package limitations ( routing / number of layers)

- Increased device performance and manufacturing tests require probes with higher current carrying capability.

The paper will review the Hybrid technology that meets and exceeds the above requirements.
Challenge

**Electrical Requirements of Manufacturing test:**
- Probes with high MAC (Maximum Allowable Current)
  - To support operating and transient currents under Dynamic Voltage Stress Test
- Low Inductance to minimize voltage transients

**Mechanical Requirements**
- Minimum Pitch (70um to 100um)
- Probe compliance
  - Large Deflection range to absorb large bump and space transformer co-planarity
- High Bump Count

*Challenge is to meet all the above requirements with one probe technology per design*
Dynamic Voltage Stress Test

- A test at elevated voltage to eliminate early-life failures.
- Typically performed at 1.4x to 1.7x typical voltage.
- Devices that fail this test often generate large current surges through a subset of VDD/VSS probes before the initiation of power supply current clamps.
- Probe card requirement: High MAC (Maximum Allowable Current)
Burn events due to High Current flowing through the Probes

Deformed Probes due to current exceeding MAC

Deformed Probes exhibit planarity change
MAC Concept

Confirmation of MAC concept, Stable Probe Tip Planarity after 35k MAC pulses

- No change to probe tip’s planarity during the performed 35k MAC (742mA) pulses
- Each pulse 1min-on/1sec-off
- 75um probe deflection
Approach-Optimized Solution

FFI Hybrid Technology

• Dual-probe design with composite (multi-material) probe structure
  – Hybrid technology to use different cross-section probes for different pitches
  – Independent optimization of power, ground, and I/O probes
  – Use finer pitch probe as needed for IO’s on perimeter of the die and larger pitch probes for power/ground bumps for the core area of the chip
  – Satisfy multiple requirements, while “de-constraining” from a single-probe design
Approach-Example

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Tips Comparison

100um Pitch Probe

80um pitch probe
# Trade-Off

## Probe Length, *Pitch*, *MAC*, *Inductance* & *Deflection*

<table>
<thead>
<tr>
<th>Probe Length</th>
<th>Pitch</th>
<th>MAC</th>
<th>Inductance</th>
<th>Deflection</th>
</tr>
</thead>
<tbody>
<tr>
<td>Short Probe</td>
<td>80um</td>
<td>Low MAC</td>
<td>Lowest Inductance (high Frequency)</td>
<td>Small Deflection range (unable to absorb large co-planarity)</td>
</tr>
<tr>
<td>Medium Probe</td>
<td>80um</td>
<td>MAC higher than Short and Long slender Probe but less than 100um pitch Medium Probe</td>
<td>Adequate Deflection range</td>
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</tr>
<tr>
<td>Medium Probe</td>
<td>100um</td>
<td>Higher MAC</td>
<td></td>
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</tr>
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</tbody>
</table>
Trade-Off
Probe Length, Probe Cross-Section, Pitch, MAC & Inductance

Probes designed to have 100um compliance
Trade-Off
Probe Max Deflection and Spring Constant vs. Probe Length
@80um compatible Cross-Section

Max Deflection and Spring Constant vs. Probe Length
X-section remains the same

Production Range

Max Deflection (um), Spring Constant(200xG/um)
Trade-Off
Lifetime and Pitch vs. Probe Length

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Implementation/Design Challenges

• One principal probe design to achieve function/reliability at different pitches
• Probe Head design optimization to attach distal end of two different probes on substrate
• Universal performance:
  – OT, Stress field, assembly, cleaning, maintenance, wear rate
• Cleaning protocols for hybrid designs in production environment.
  – Optimized cleaning recipes to maintain best current carrying capability while maintaining long product lifetime.
Issues & Next Steps

• **Initial evaluation:**
  – Potential issue with Hybrid approach is the non-uniform wear rate between different cross-section probes

• **Next step is to evaluate the updated approach and verify the uniform wear rate with customer**

• **Launch the Hybrid Technology in production environment**

• **Scale the Hybrid technology at various pitches allowing multiple (>2) probe technologies**
  – Include larger pitch probes to have higher MAC benefit
Summary

• **Achievement of mutually exclusive requirements on a single probe card**
  – 1Amp/probe in sub-100µm array configuration benefit from a Multi-Probe (each with multi-composite layers) design
  – High speed I/O performance
  – Adequate compliance

• **Validation of probe tip cleaning protocols for lifetime wear rate for Hybrid Probe Card**
Thank You