SW Test Workshop
Semiconductor Wafer Test Workshop

Improved ON-resistance Measurement at Wafer Probe using a "DARUMA" stage

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June 4-7, 2017

Overview

- **Background**
  - Trend of MOSFET
  - Transition of low ON resistance ($Rds_{(on)}$) products
- **Present situation**
  - Measurement by Standard stage
  - Matter of concern
  - Suspected root cause
- **Solution**
  - DARUMA
  - Overview of DARUMA Chuck
  - Advantage of DARUMA Chuck etc.
- **Verification**
  - Measurement by “DARUMA”
  - Comparison with standard stage
  - Simulation
- **Conclusion**

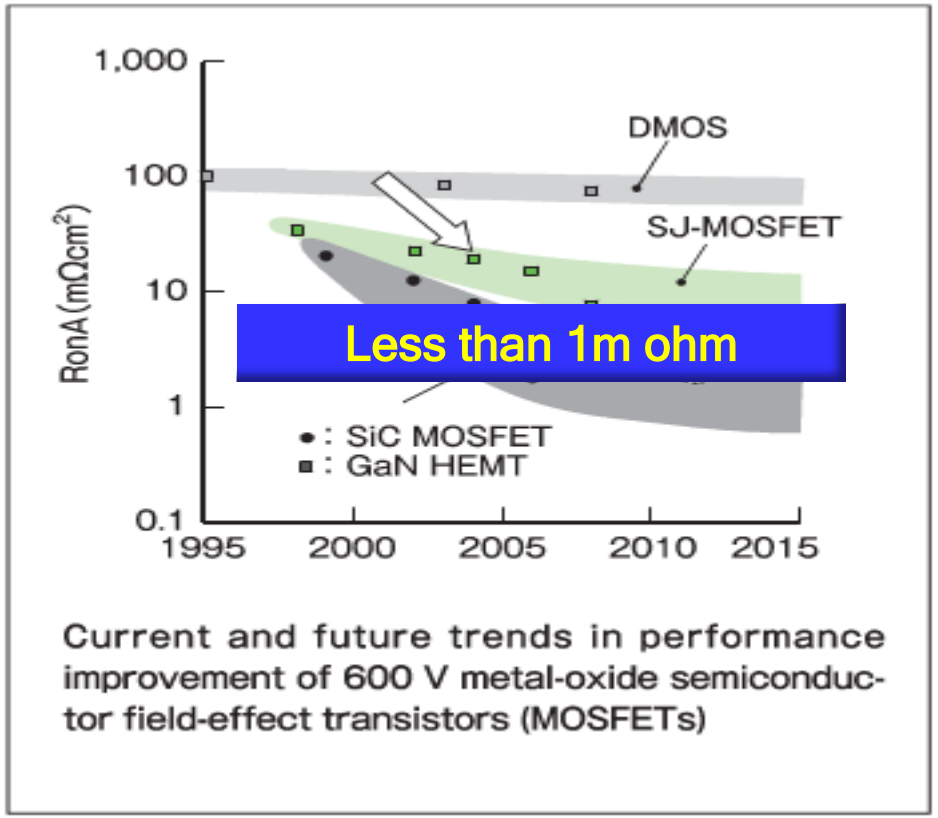
Trends of MOSFET

- **Application and Criteria**
  - Load switch for DC Supply-unit in server
    - Low On-Resistance ($Rds_{(on)}$)
    - Low Thermal Resistance (Rθjc, etc.)
    - Wide Safe Operating Area (SOA)
  - Switching device for switched-mode power supply (SMPS)
    - Low $Rds_{(on)}$
    - Low Gate Charge (Qg)
  - Motor control
    - Low Reverse Recovery Time (trr)

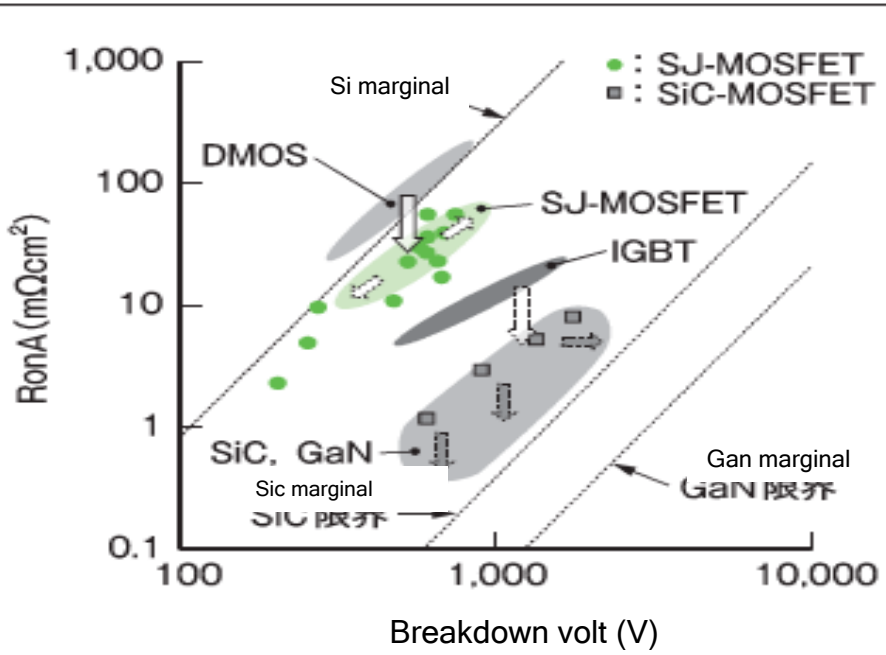
Trends of MOSFET

- **Purpose vs Representative Characteristics**
  - Energy savings ⇒ Low On-Resistance
    (Low loss)
  - Fast switching ⇒ Low gate Capacitance
    (High speed)
  - High reliability ⇒ Wide Safe Operating Area,
    (High performance) High breakdown resistance
  - Miniaturization ⇒ Enhancement of Heat-resisting property
    (Small packaging)

Transition of low ON resistor products



Current and future trends in performance improvement of 600 V metal-oxide semiconductor field-effect transistors (MOSFETs)

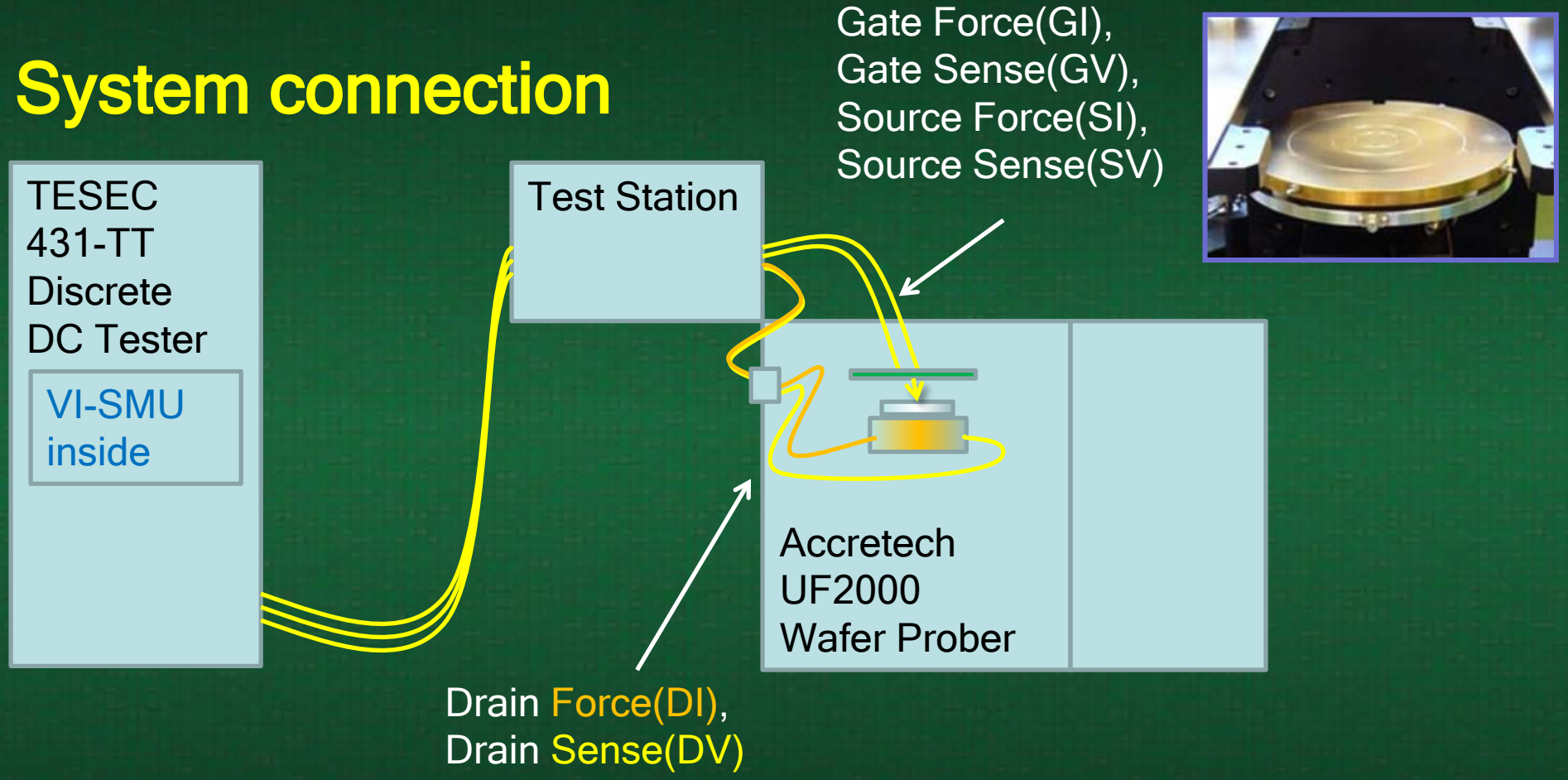


Dependence of power device on-resistance on voltage rating

Graphs from *Toshiba Review* Vol.65No.1 (2010)

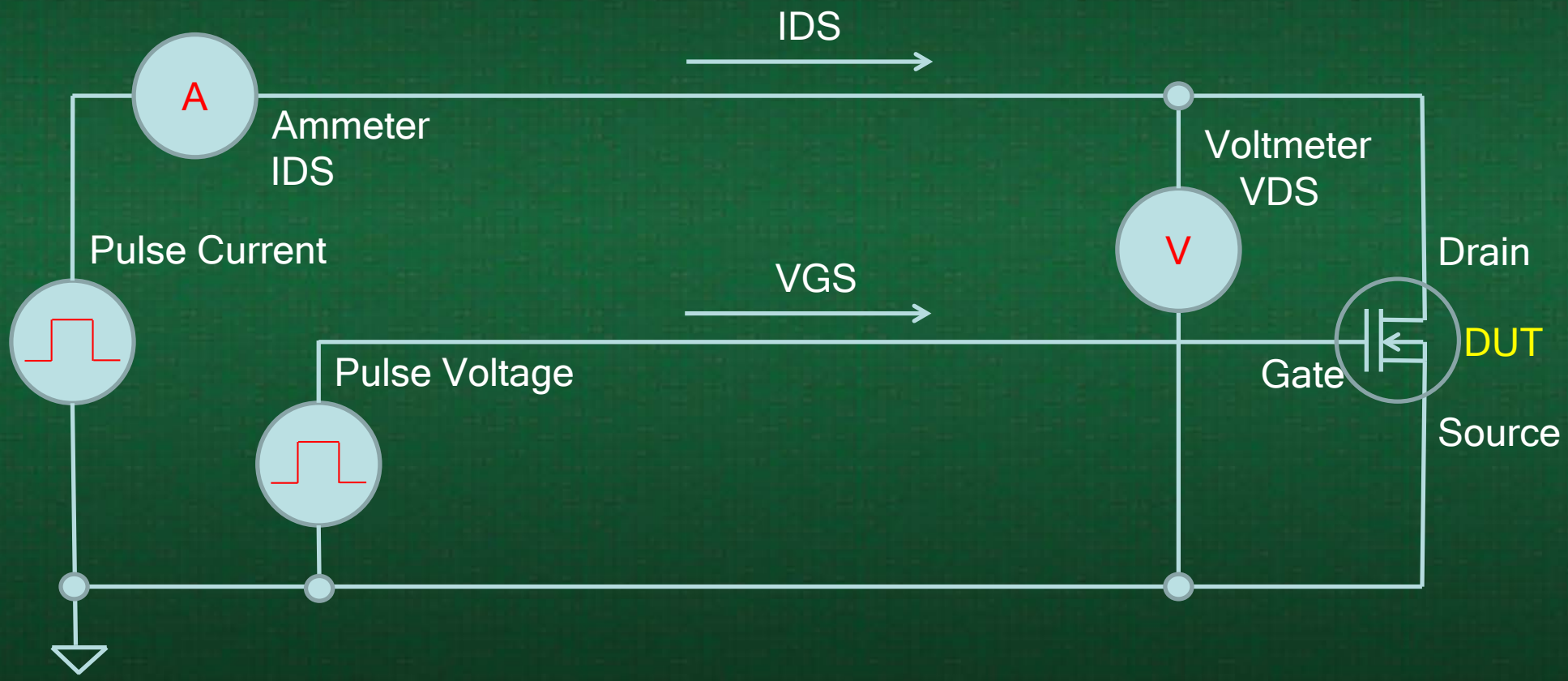
Present situation

- Standard System connection



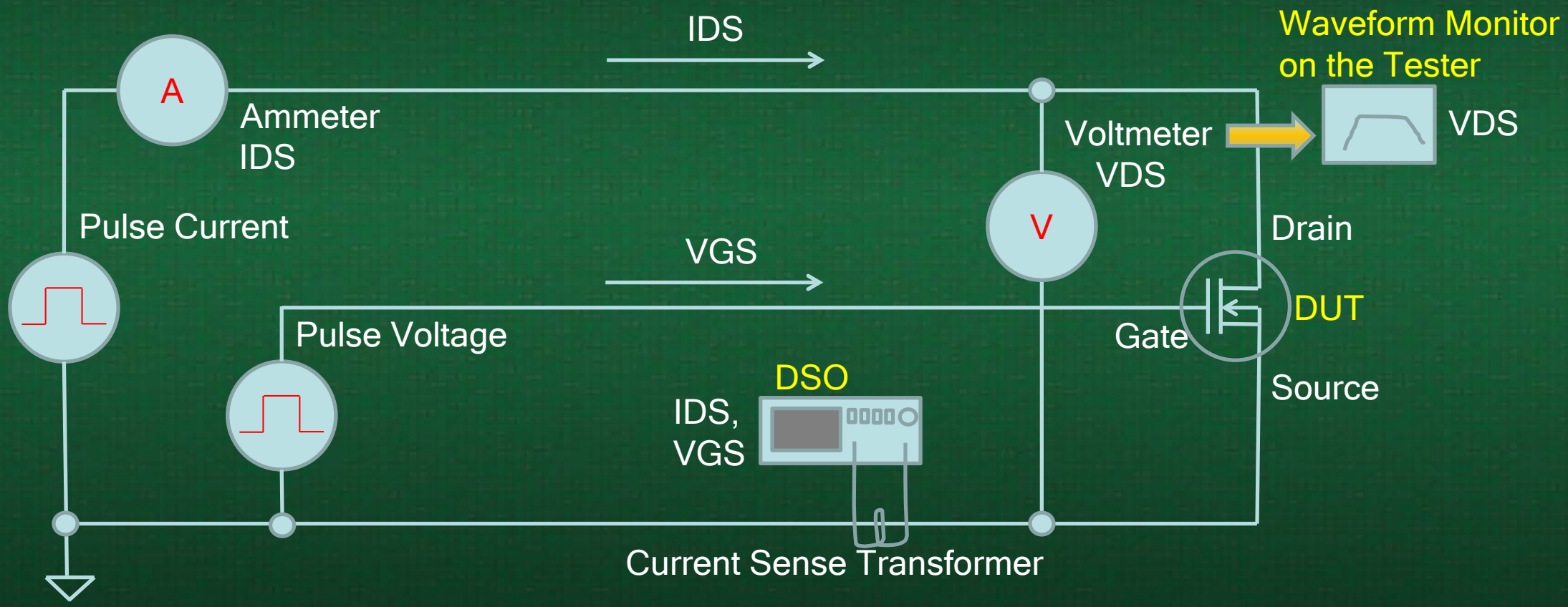
Present situation

- **Simplified Schematics for $Rds_{(on)}$ testing at wafer probe**



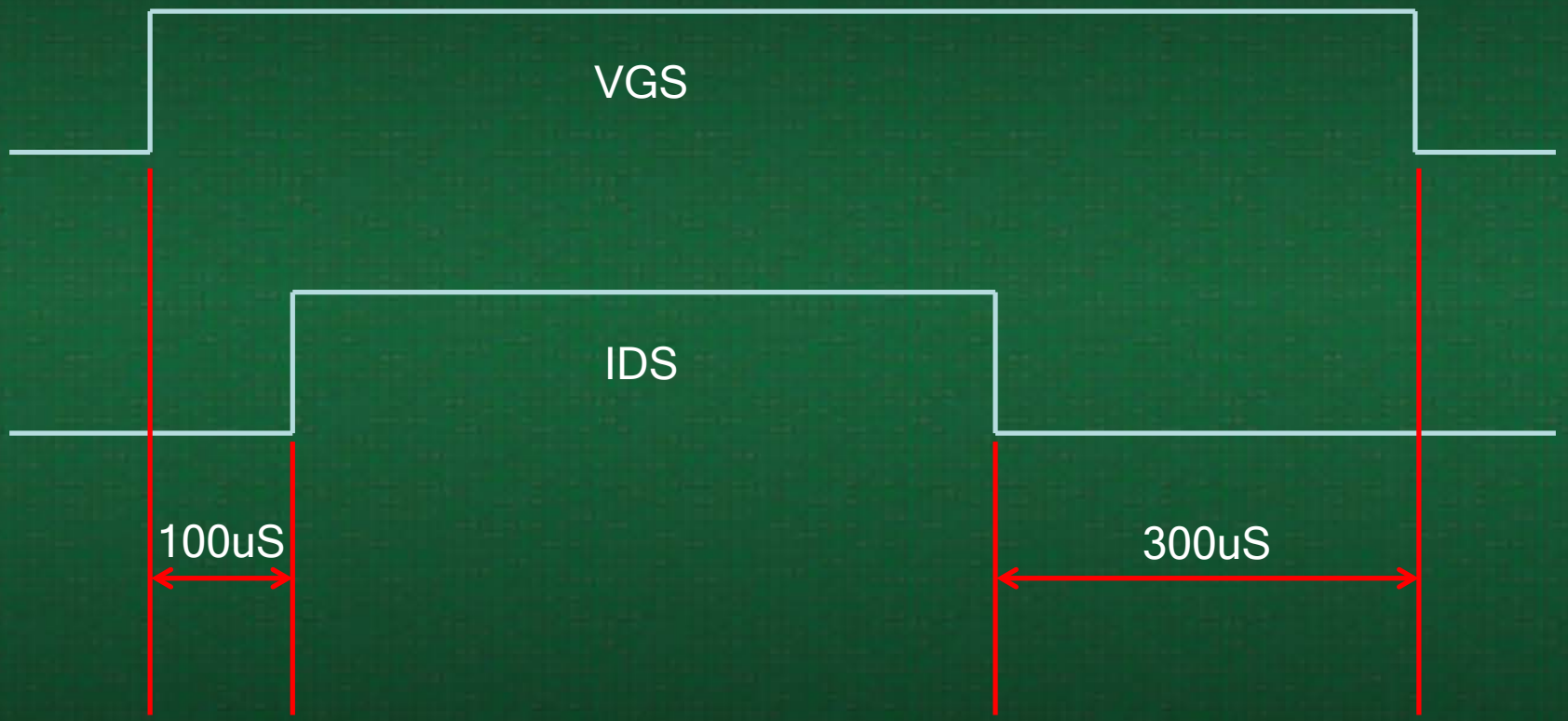
Present situation

- **Simplified Schematics for $Rds_{(on)}$ to check waveform**



Present situation

- Timing chart

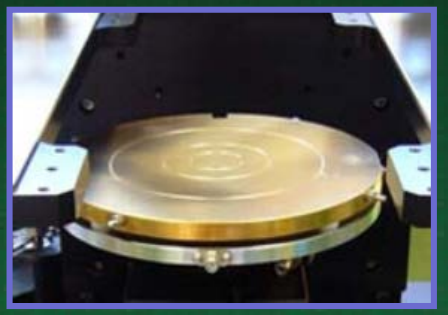


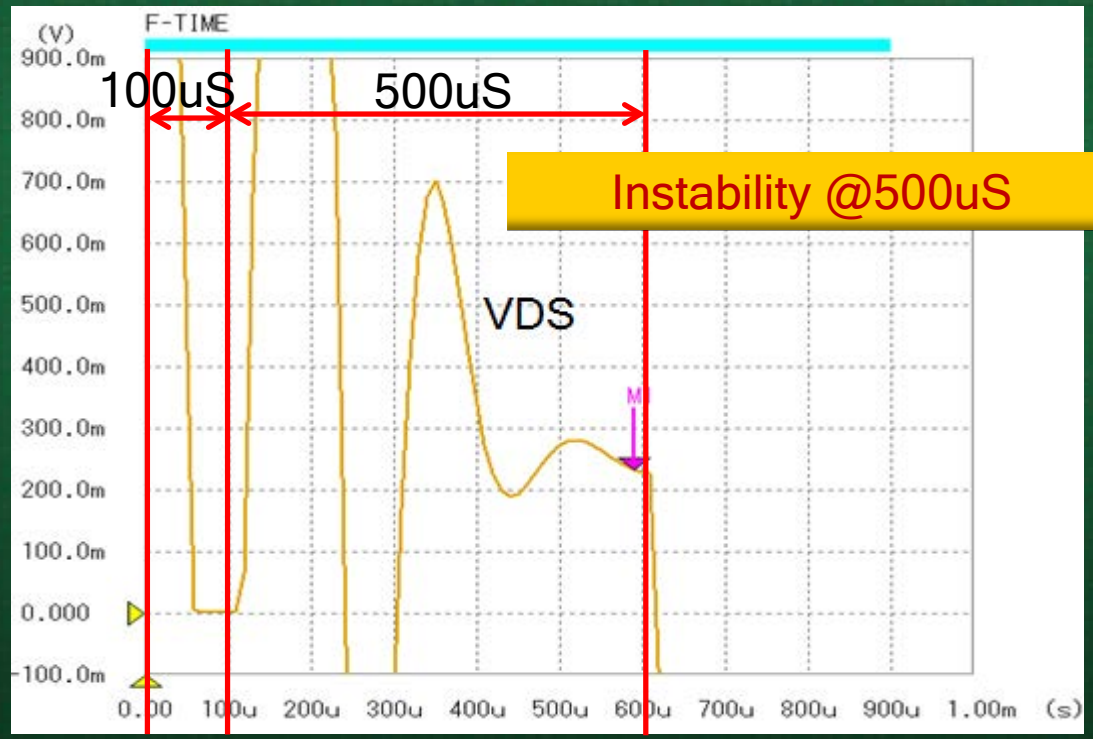
Present situation

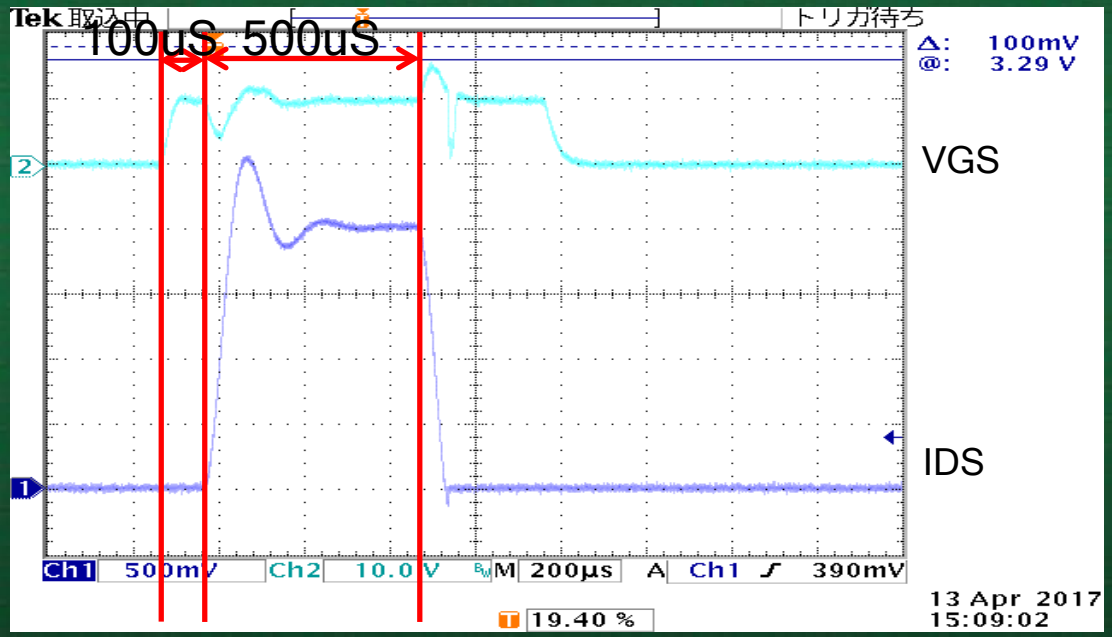
[Measurement result-1]

Test condition : $Rds_{(on)}$, IDS=200A, Test time=500uS

Stage type : Standard





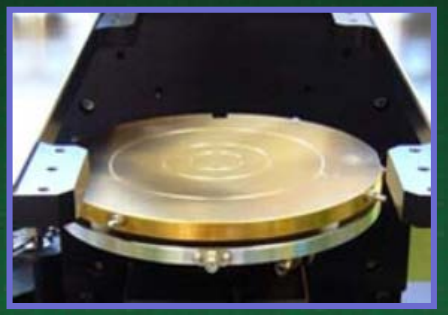


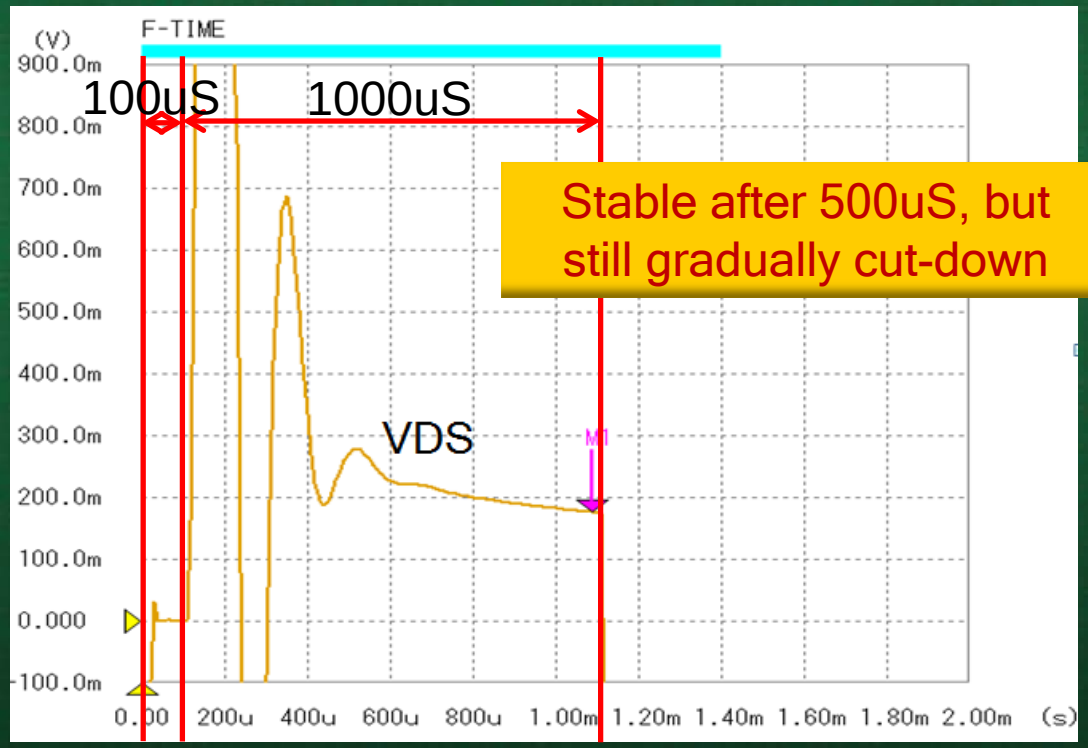
Present situation

[Measurement result-2]

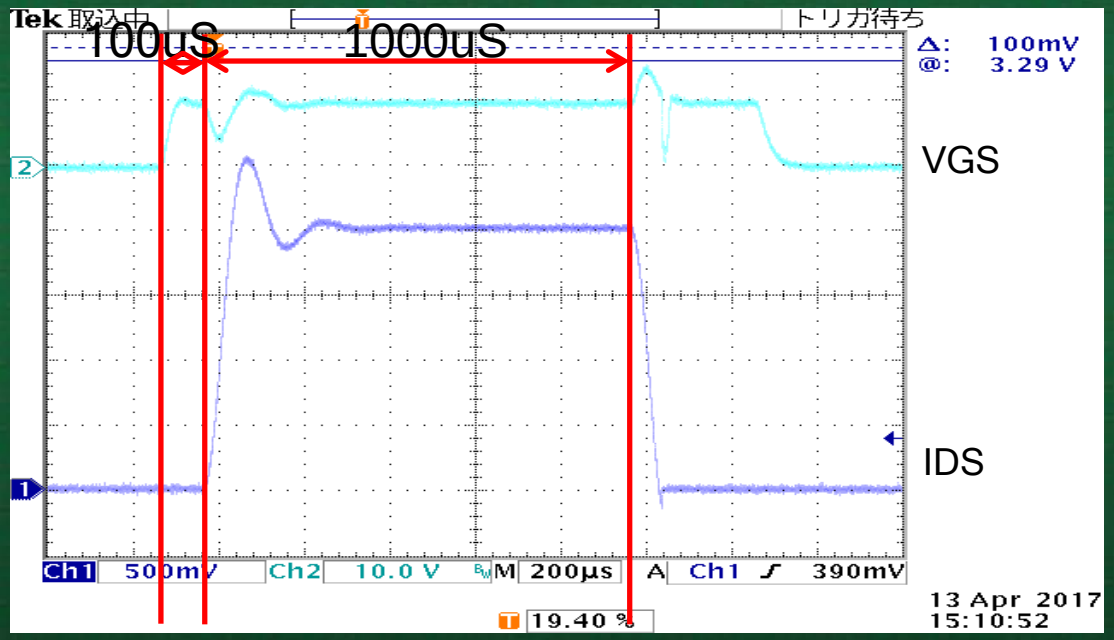
Test condition : $Rds_{(on)}$, IDS=200A, Test time=1000uS

Stage type : Standard





Stable after 500uS, but still gradually cut-down



Matters of concern

Measurement waveform is unstable
(Need longer test time to be stabilize)

Increases Forcing time of test current

Increases temperature of the tested device

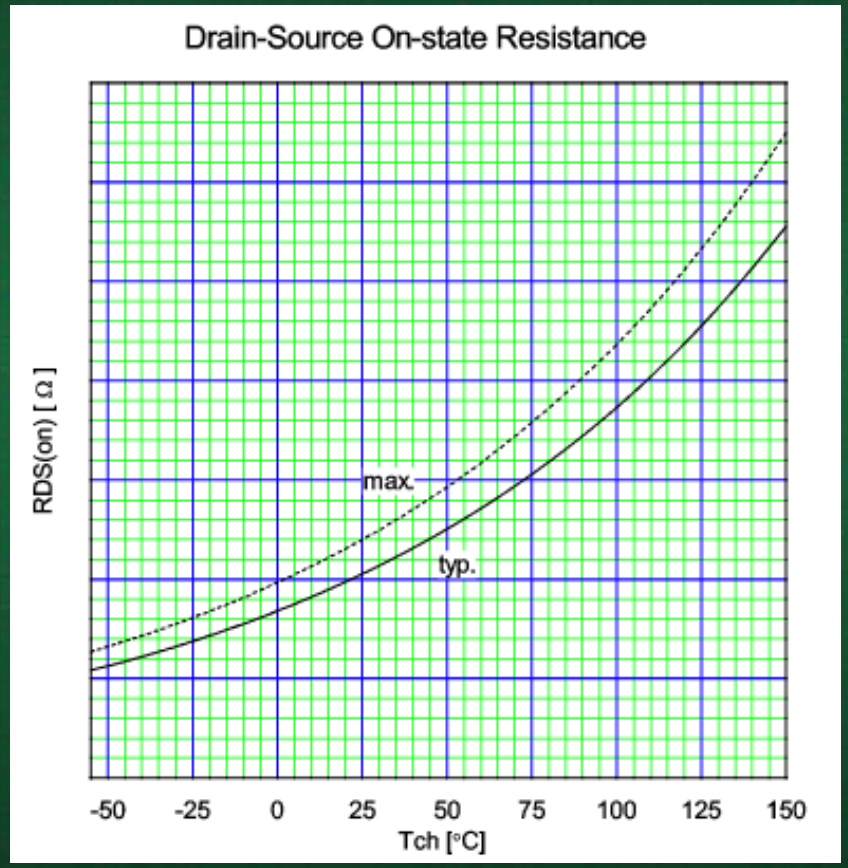
Decreases the test accuracy and production quality

Matters of concern

ON resistance vs Channel temperature

- **Ideal test environment (Temperature)**
  - Exists when the channel(Junction) and case (package) temp are the same.
  - Requires "Very short pulse" during on-resistance test to achieve temperature parity between Junction and Case
  - Characteristic of MOSFETs, the on-resistance will rise as the device temp is increased in an attempt to protect the device itself (as the resistance increases, the current decreases)
  - Therefore, when testing $Rds_{(on)}$, controlling the temperature rise is critical to measurement stability.
  - To control the temp during test,

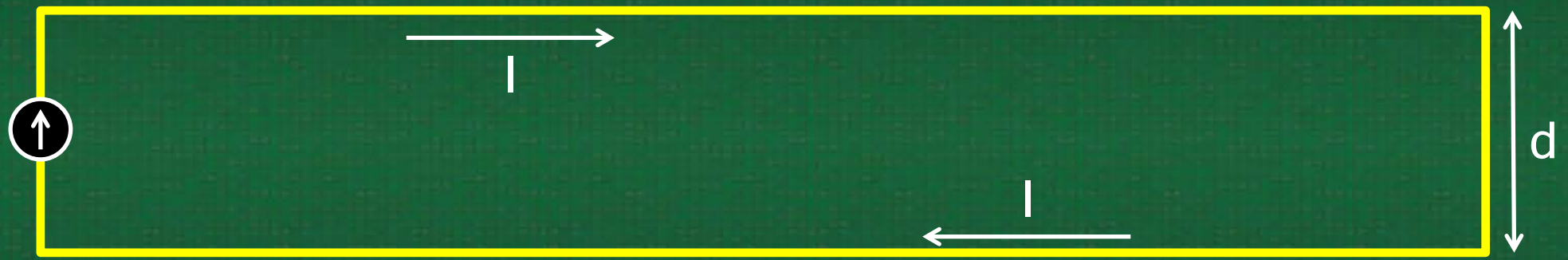
    "minimize the test time"



From *Fuji Electric AN-079 Rev.1.1*

Expected root cause

- **Ls (Stray Inductance)**
  - Self inductance of wire loop (round trip)



Diameter of the wire to be ‘2a’,

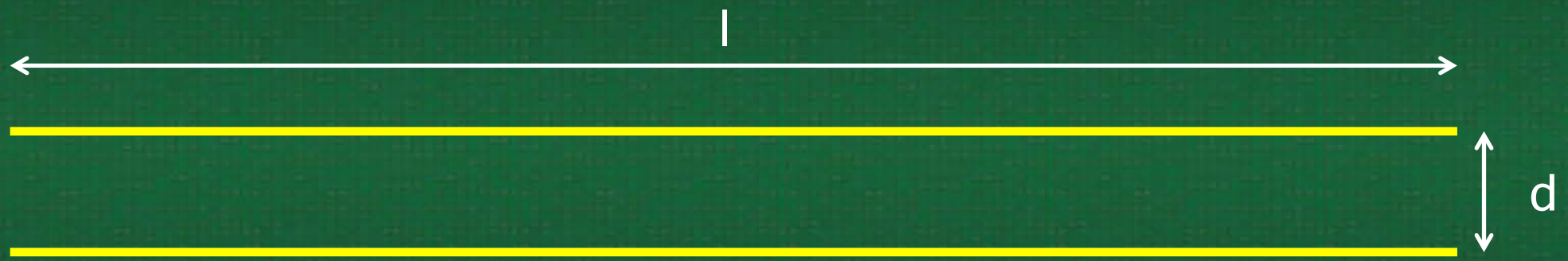
When the current is uniformly distributed in the electric wire,

and the conductor is nonmagnetic.

L = 4 * log(d/a) * 10^-7 [H/m]

Expected root cause

- **Ls (Stray Inductance)**
  - Mutual inductance between parallel wires



Pair of parallel wires,

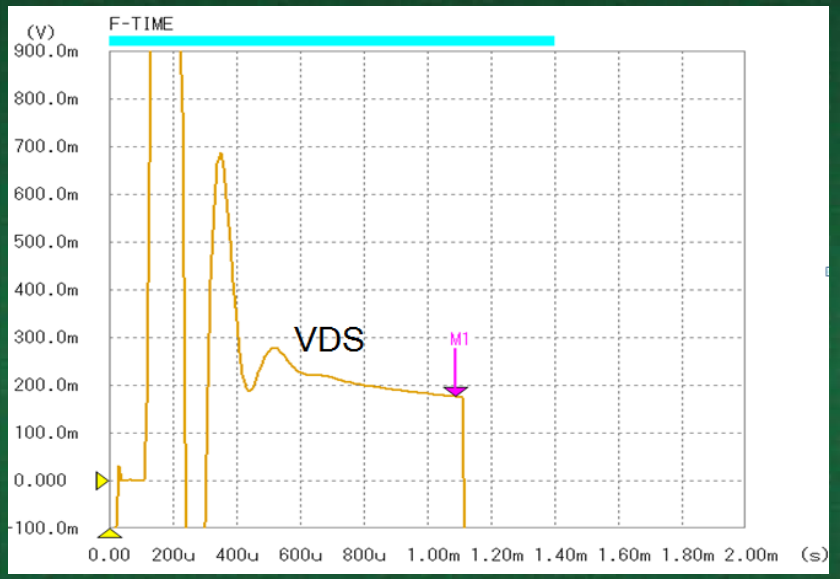
When l >> d , and in the air atmosphere.

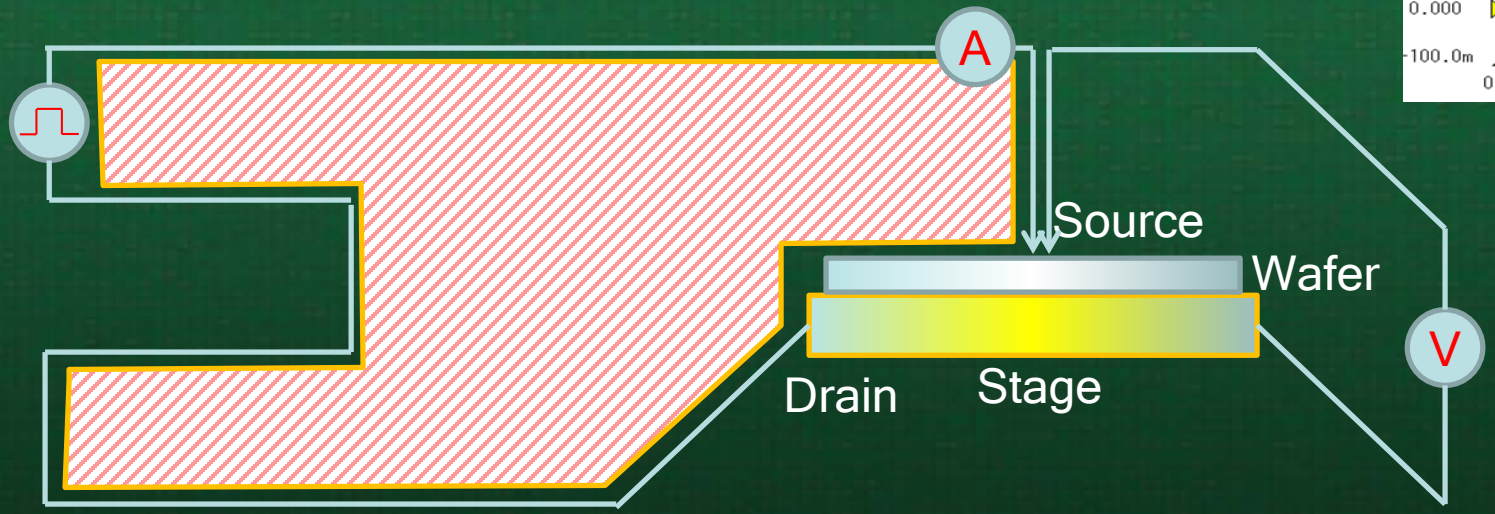
M = 2 * l * (log(2 * l / d) -1) * 10^-7 [H]

Expected root cause

- **VDS waveform is NOT stable.**

- Influence of the Stray Inductance (Ls) of the wiring between DUT and source & measurement circuits.
- Ls increases as the wire loop increases.

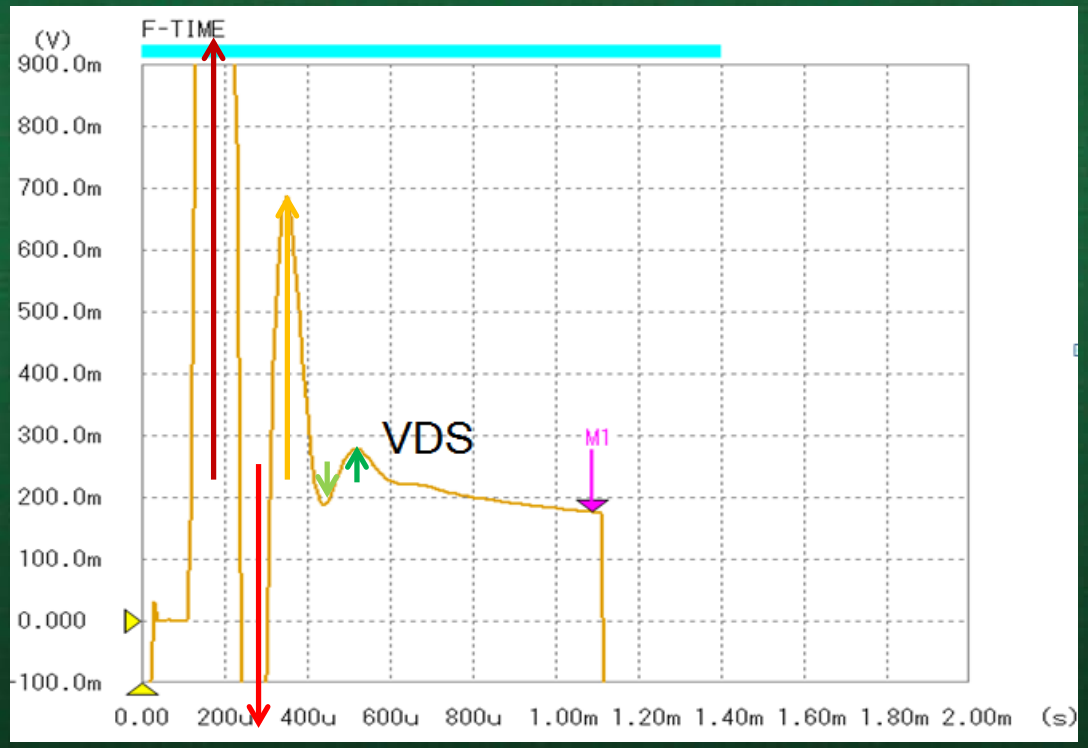


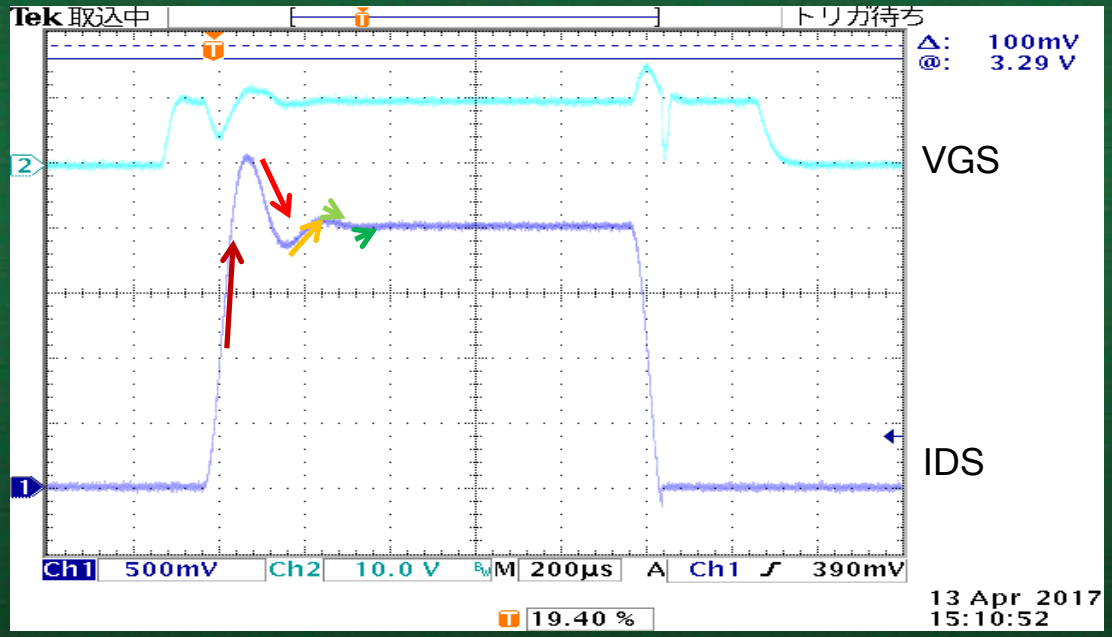


Expected root cause

- **The cause of the VDS “Spiking” is in Ls.**

  $\Delta V = Ls(di/dt)$



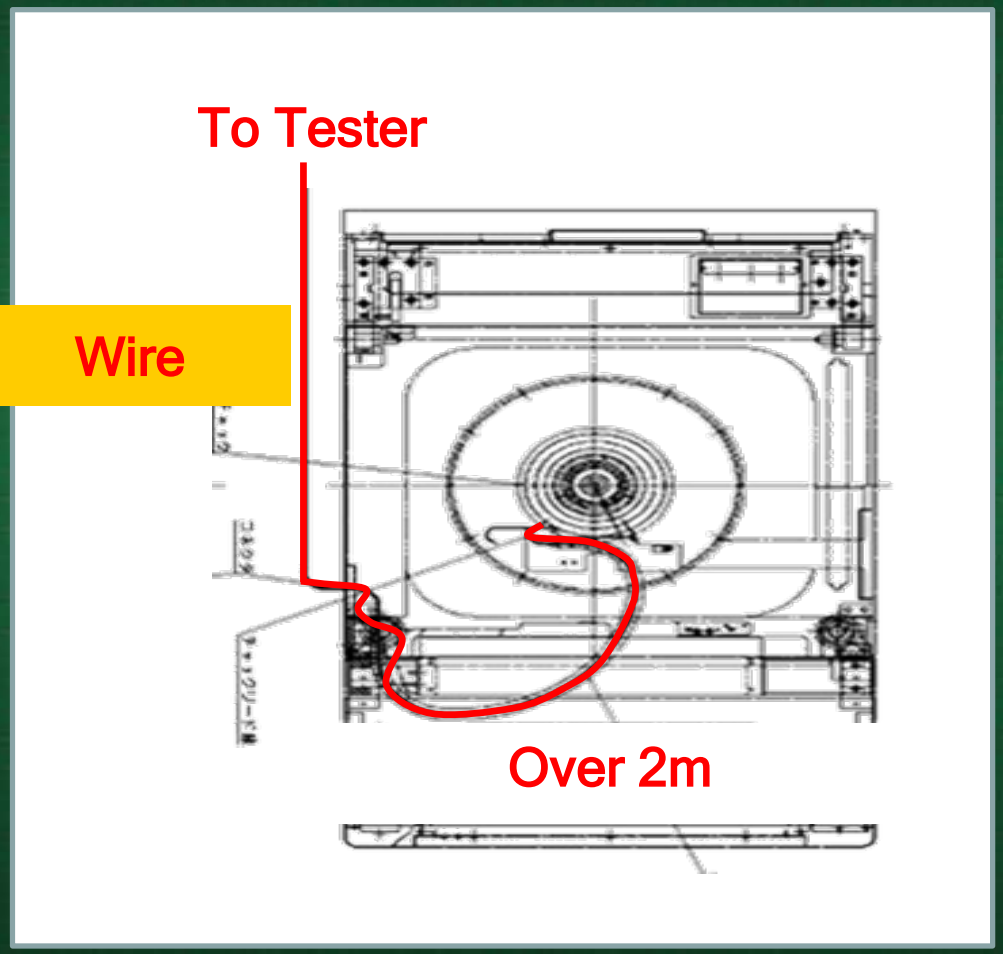


“DARUMA”

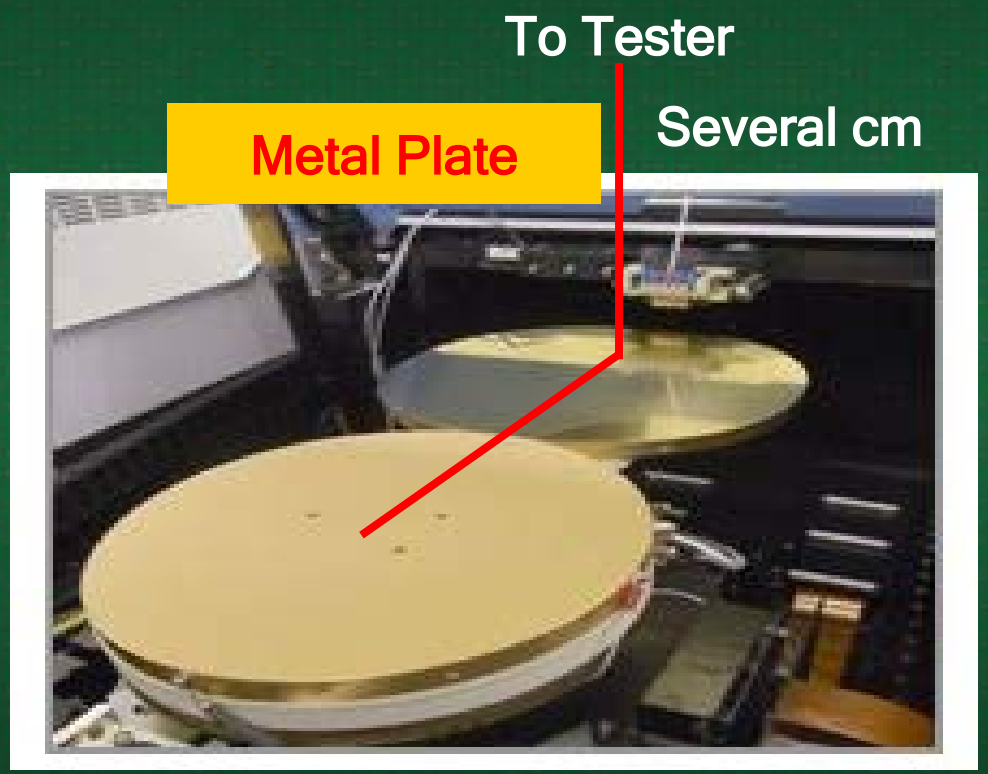
- The Daruma doll, is a hollow, round, Japanese traditional doll modeled after Bodhidharma (Dharma), the founder of the Zen sect of Buddhism. Daruma has a design that is rich in symbolism and is regarded more as a talisman of good luck to the Japanese.
- When purchased, the eyes are white so a person can decide on a goal or wish and paint one eye in. Once the goal is achieved, the second eye is filled in.

Overview of DARUMA Chuck (1)

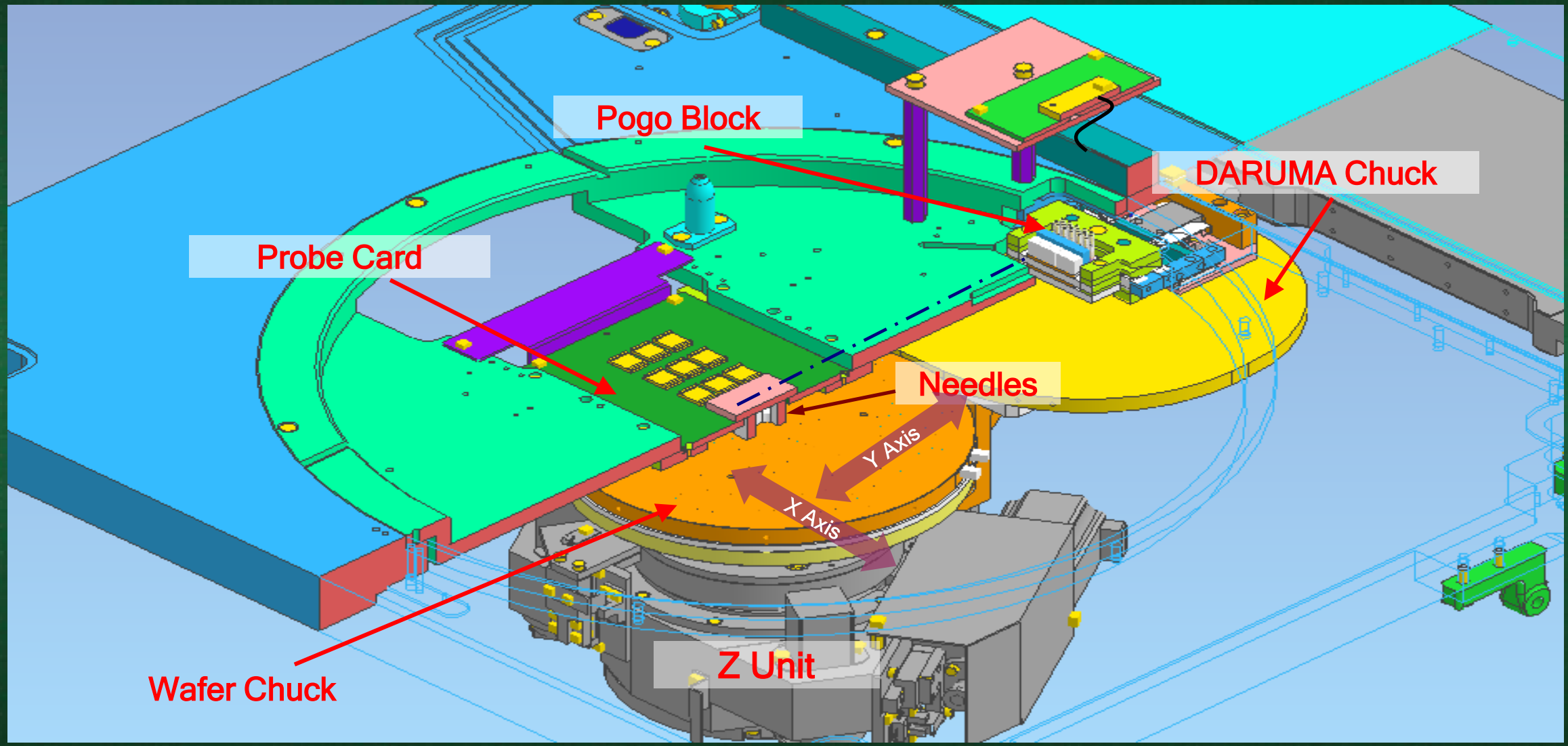
Standard connection



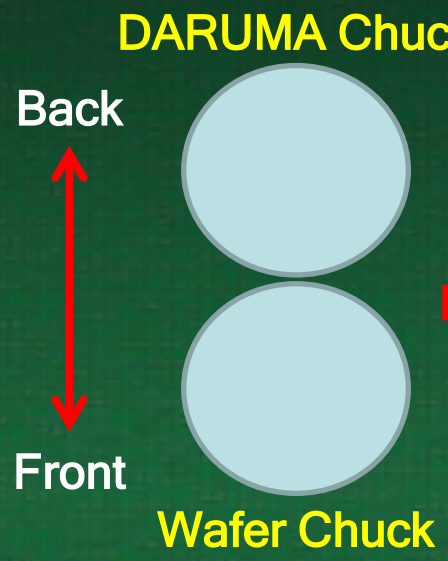
DARUMA connection

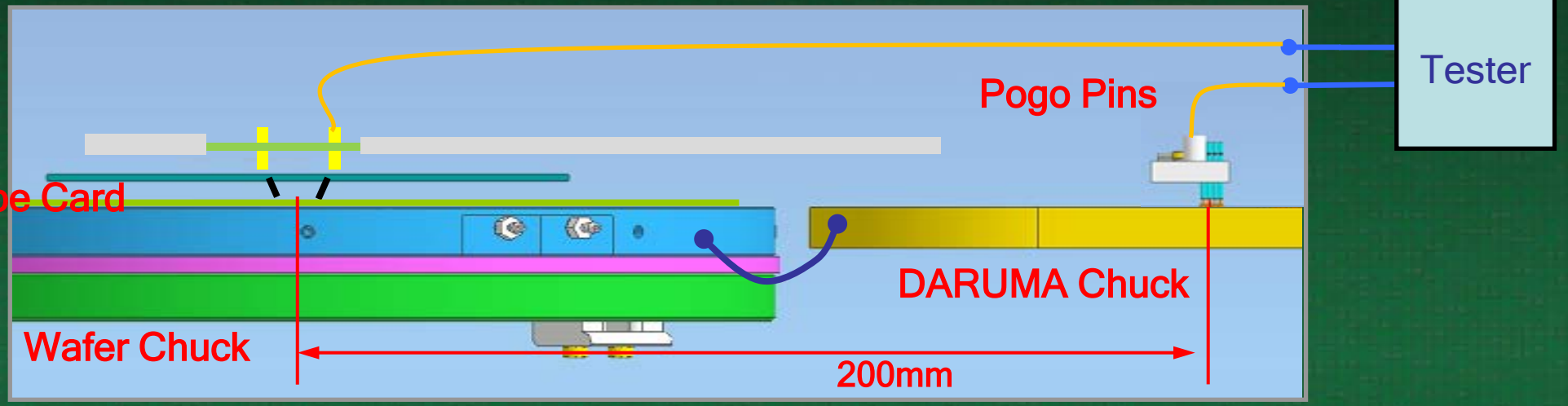


Overview of DARUMA Chuck (2)

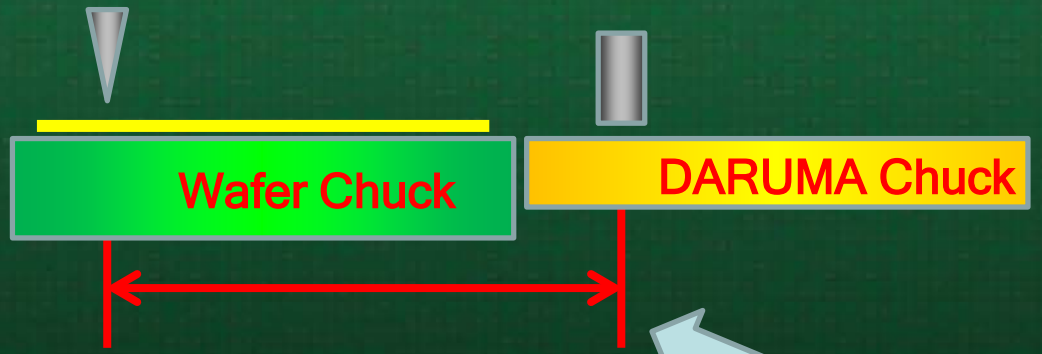


Advantage of DARUMA Chuck

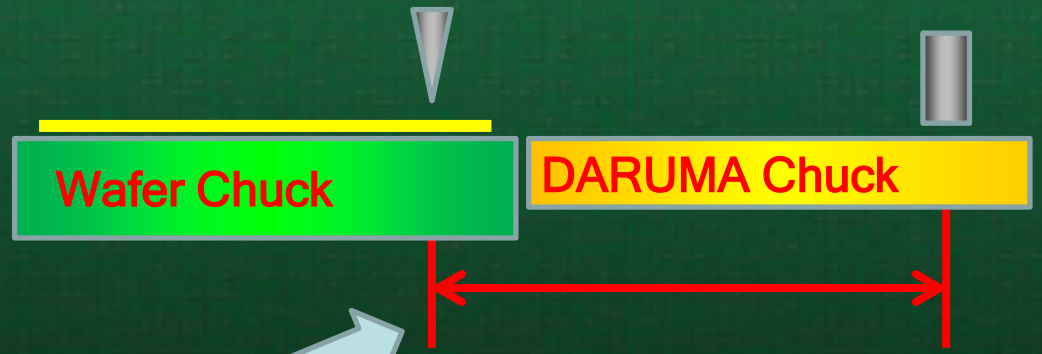




@ Front side of wafer

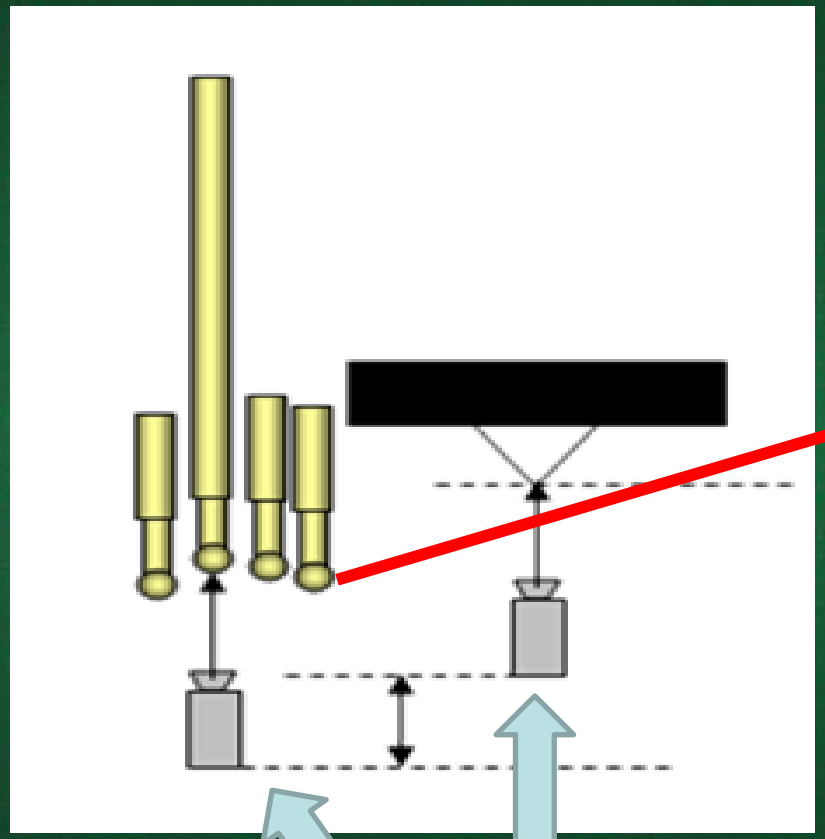


@ Back side of wafer

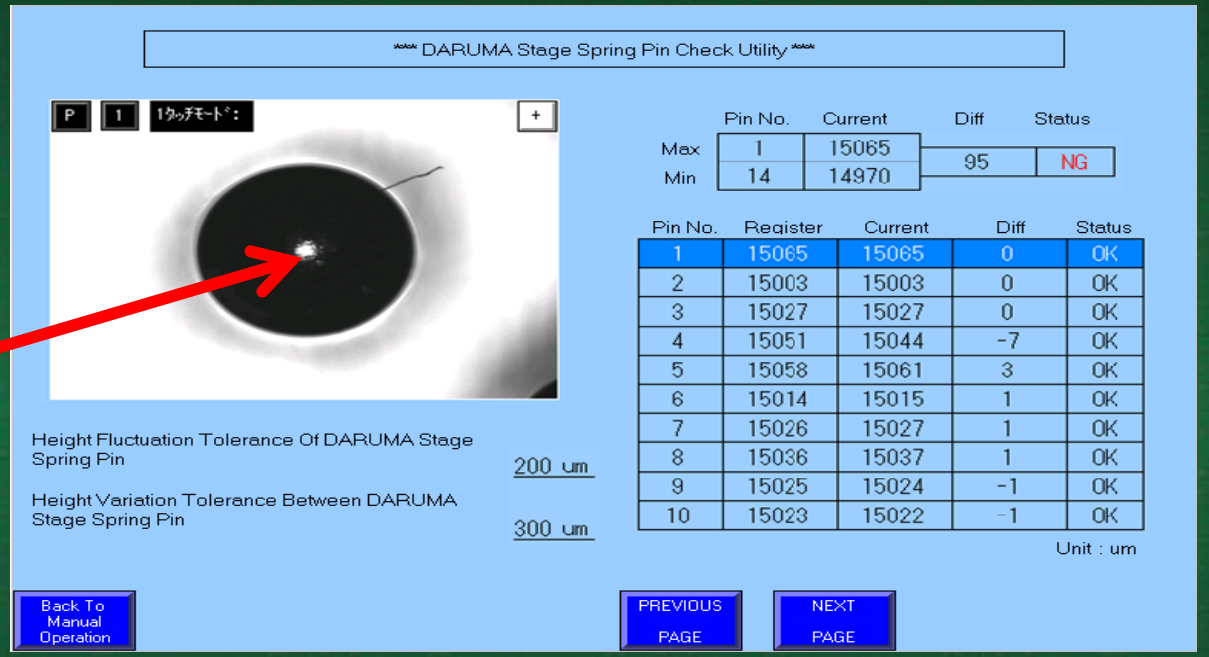


Maintain same distance

Alignment for Pogo Pins



Probe to pad alignment camera

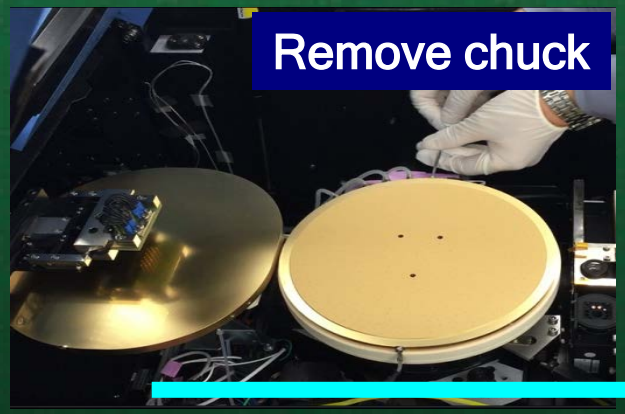


Search pogo pin height and check the difference using alignment camera. Then calculate the best over drive point for contacting to the DARUMA chuck.

Maintenance

- Turn ON voltage/Contact resistance <- Chuck surface condition
- Large current/Inductive load test -> Deteriorating chuck top

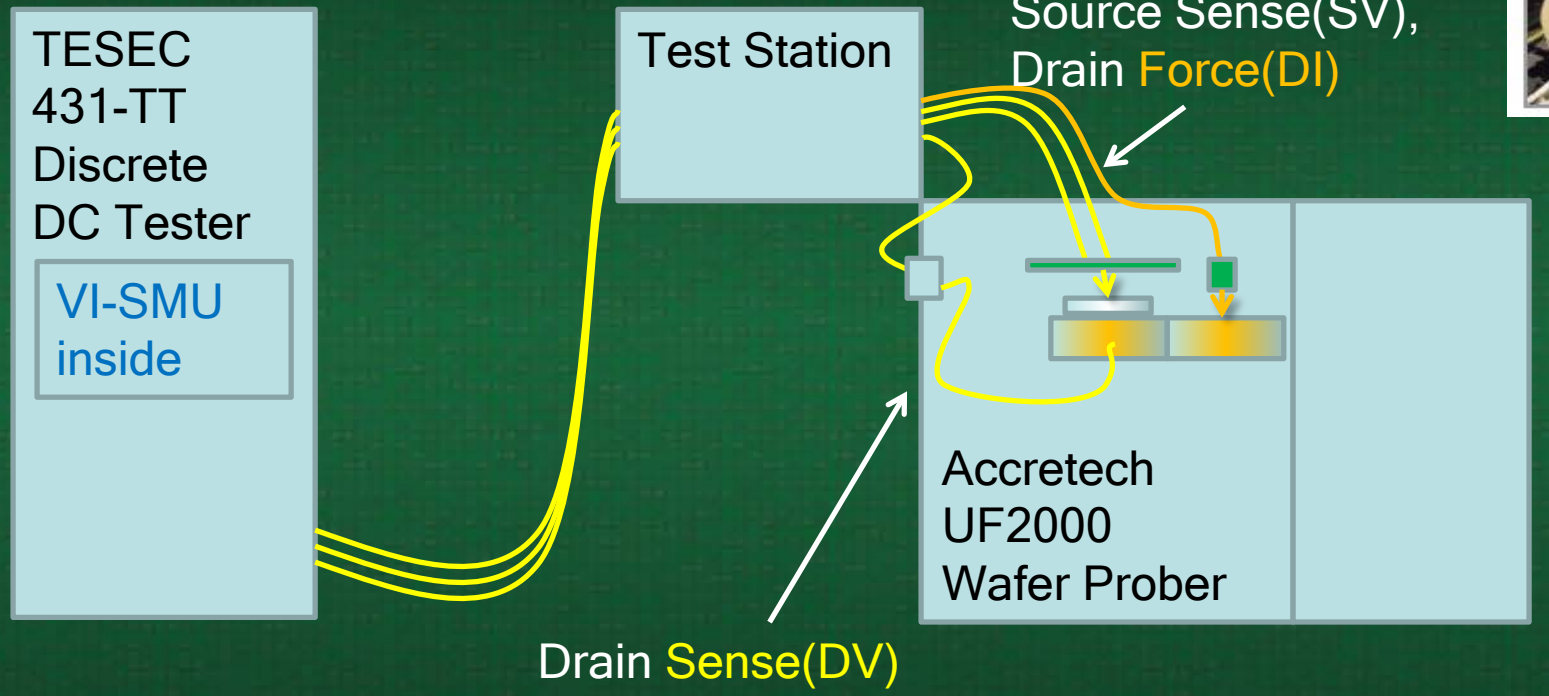
Required periodical chuck top maintenance

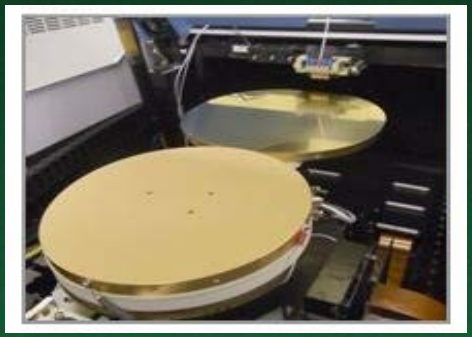


Overview of Evaluation Setup

Verification

- DARUMA System connection



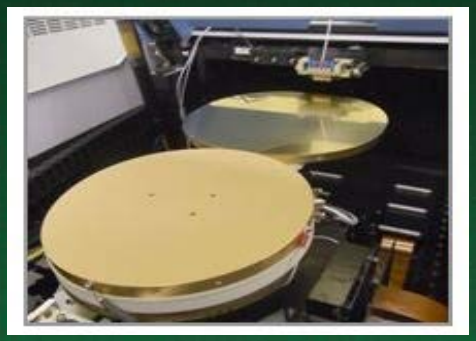


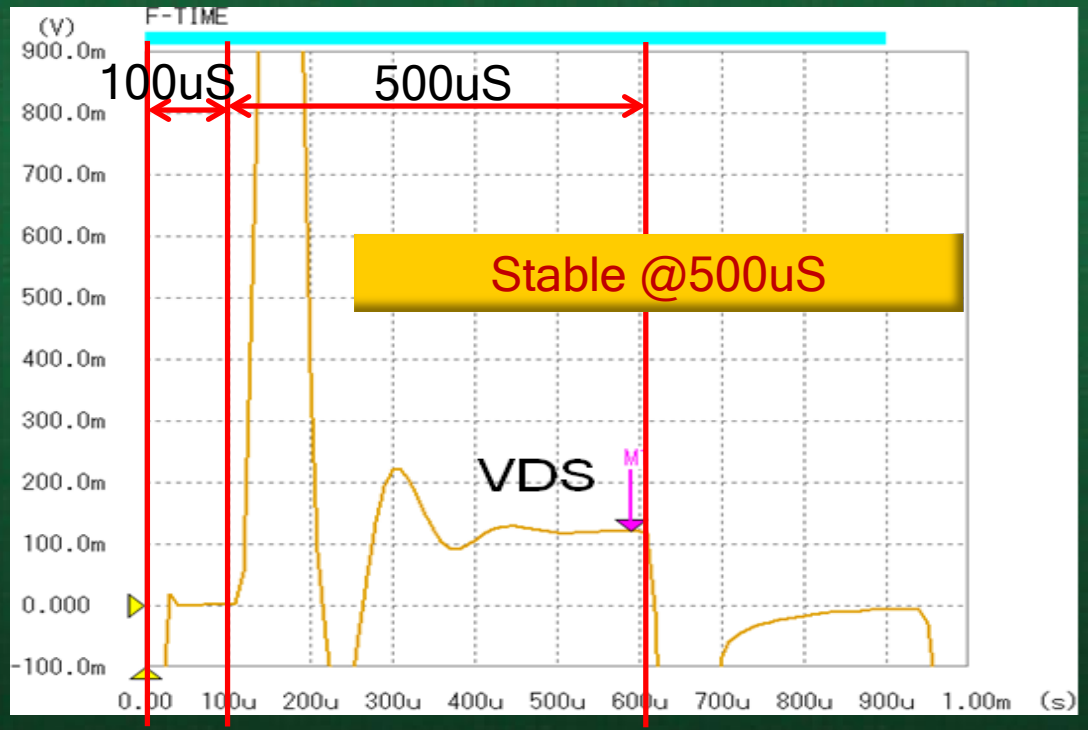
Verification

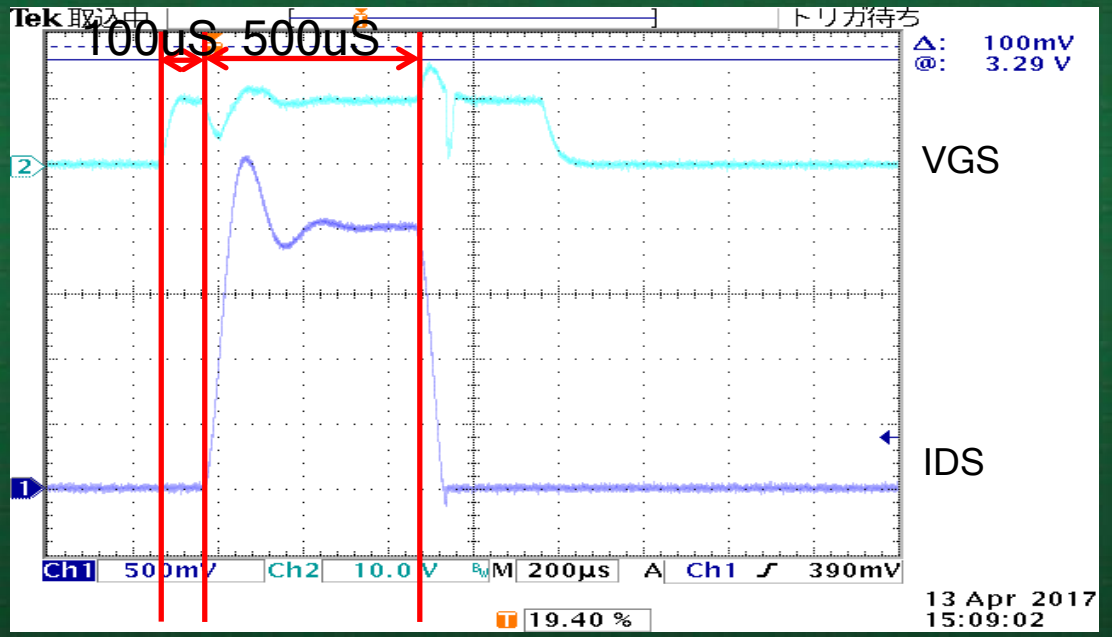
[Measurement result-1]

Test condition : $Rds_{(on)}$, IDS=200A, Test time=500uS

Stage type : DARUMA





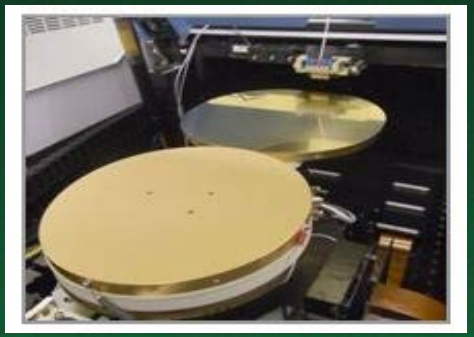


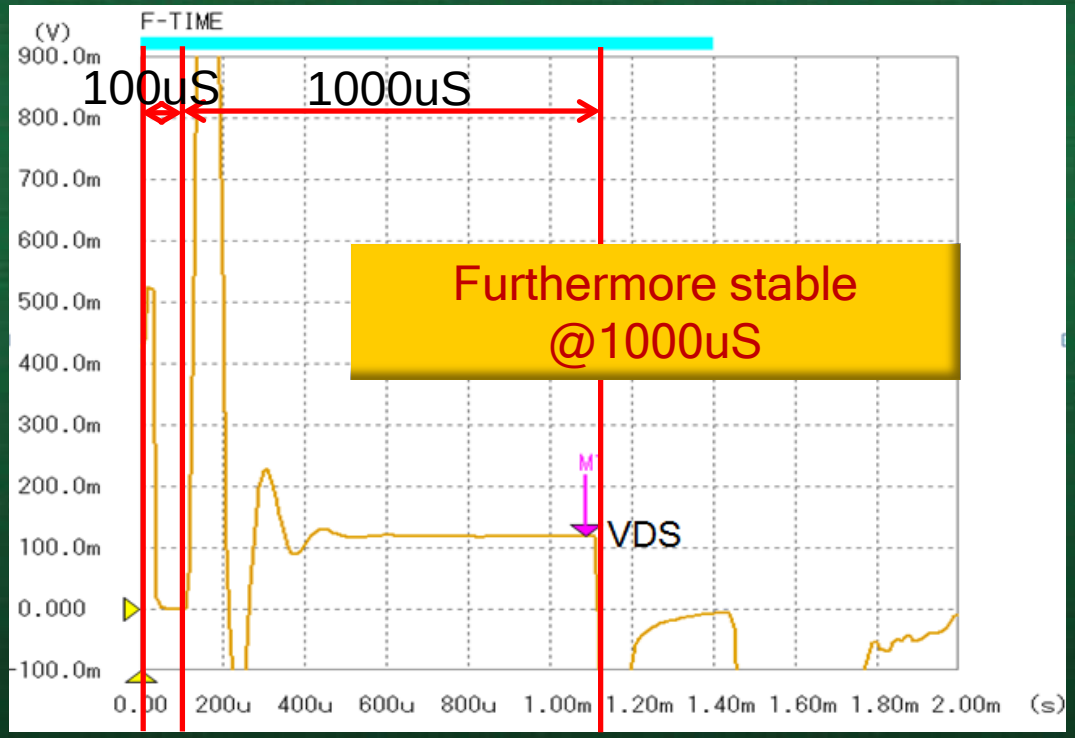
Verification

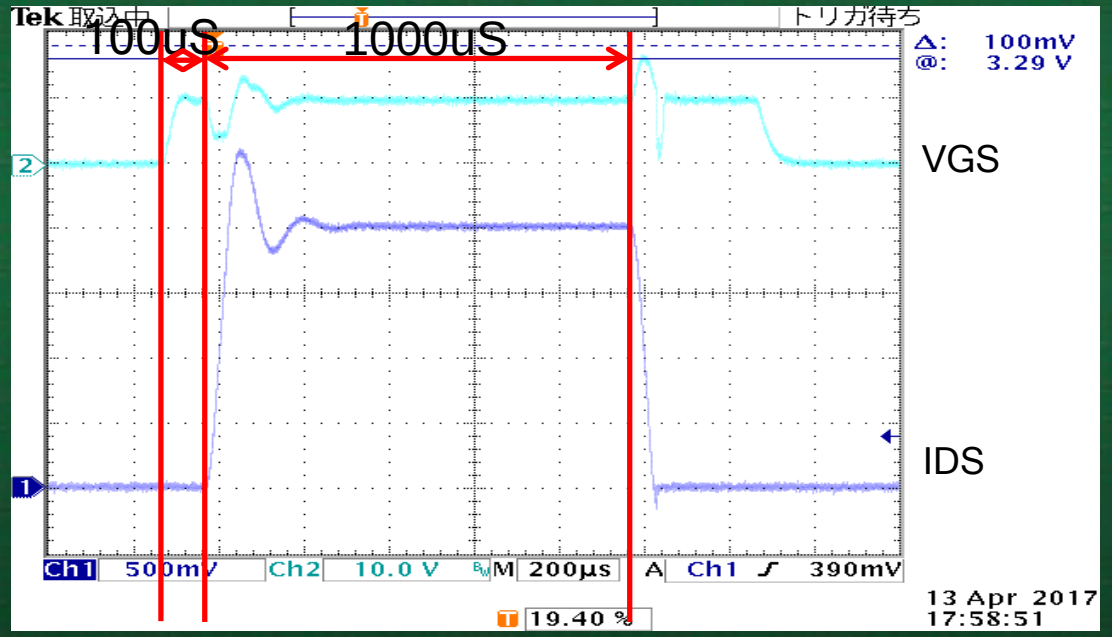
[Measurement result-2]

Test condition : **$Rds_{(on)}$**, IDS=200A, Test time=1000uS

Stage type : DARUMA



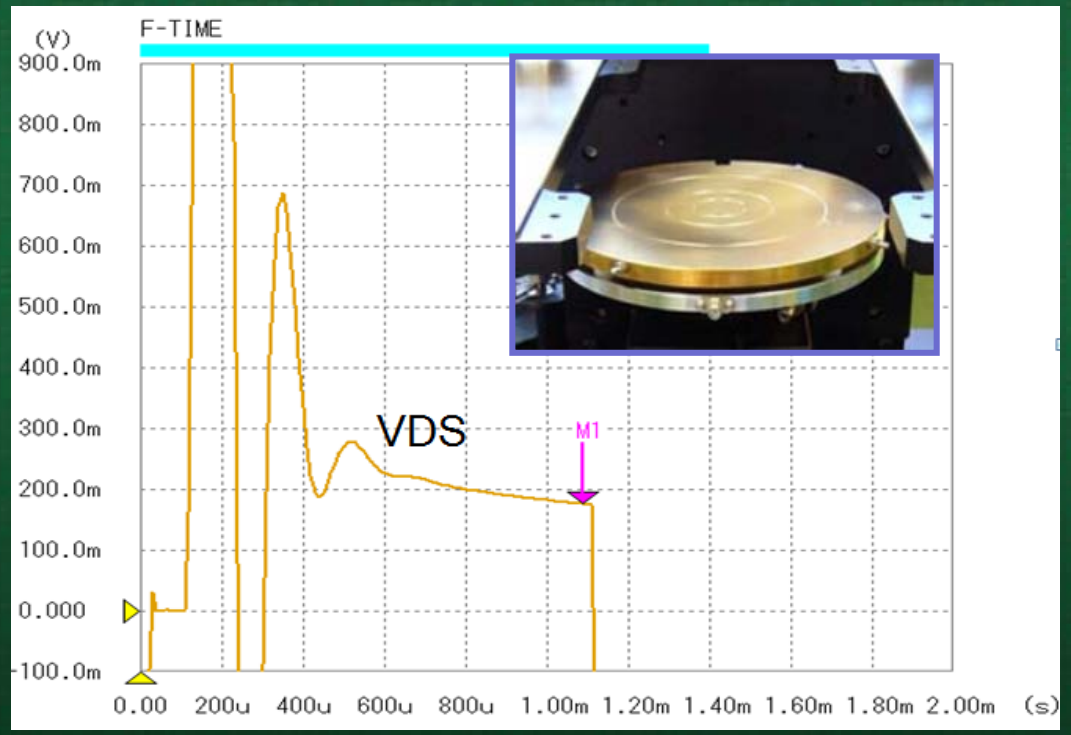




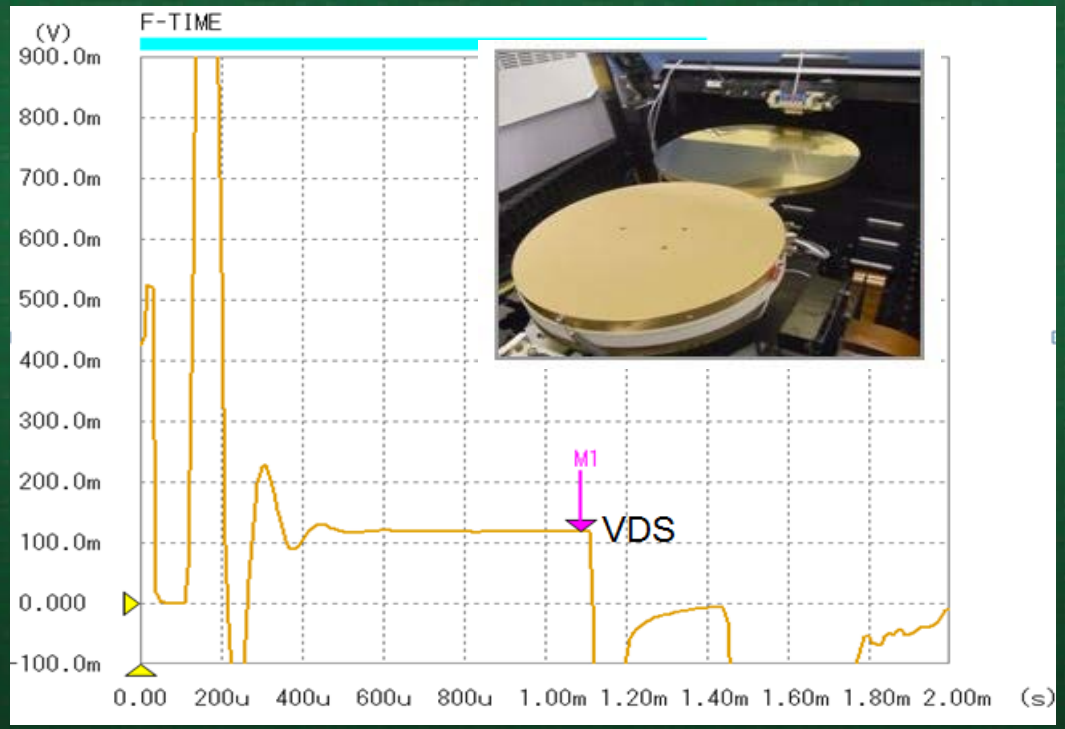
Comparison with standard stage

Test condition : **$Rds_{(on)}$**, IDS=200A, Test time=1000uS

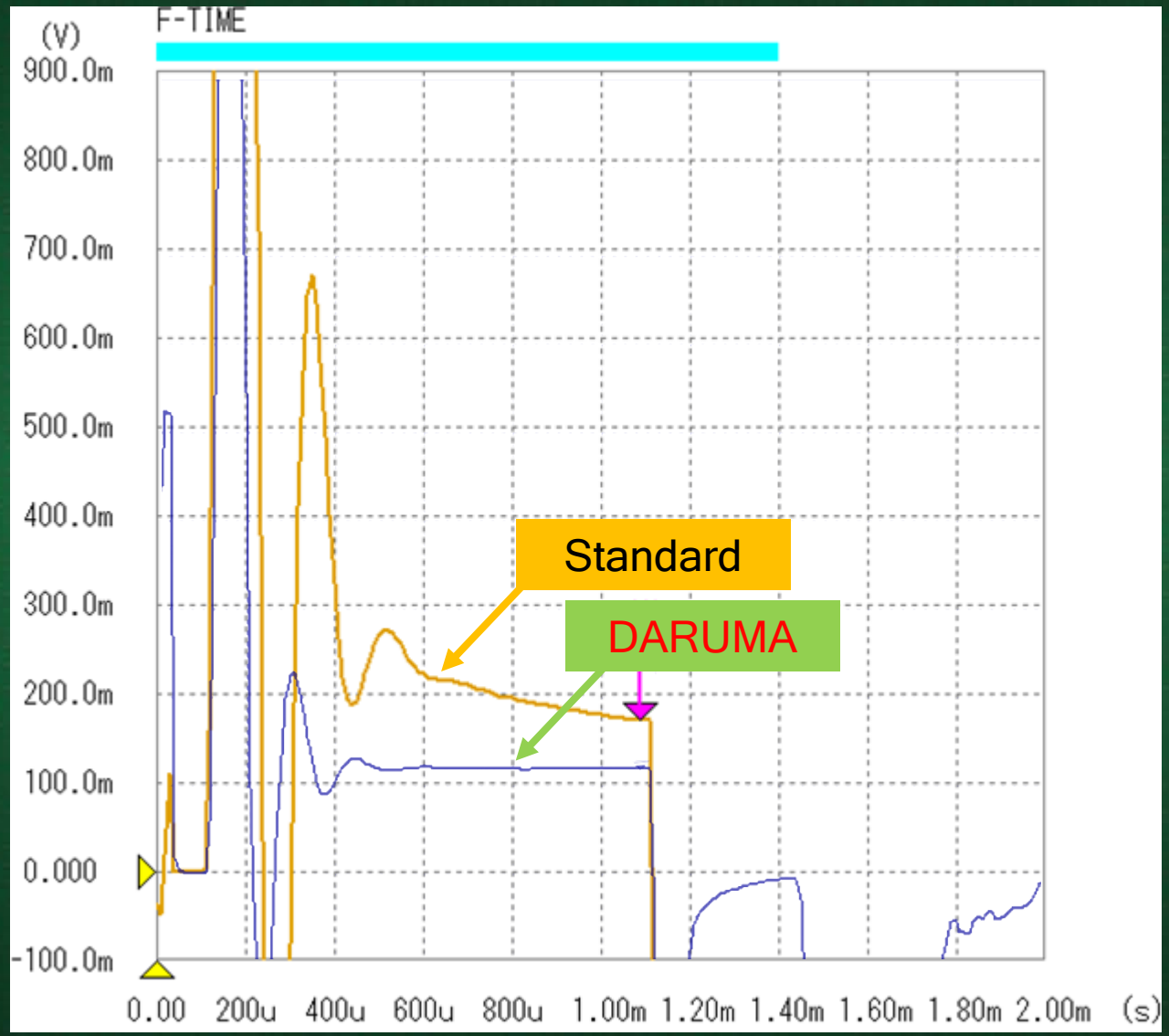
Standard connection



DARUMA connection

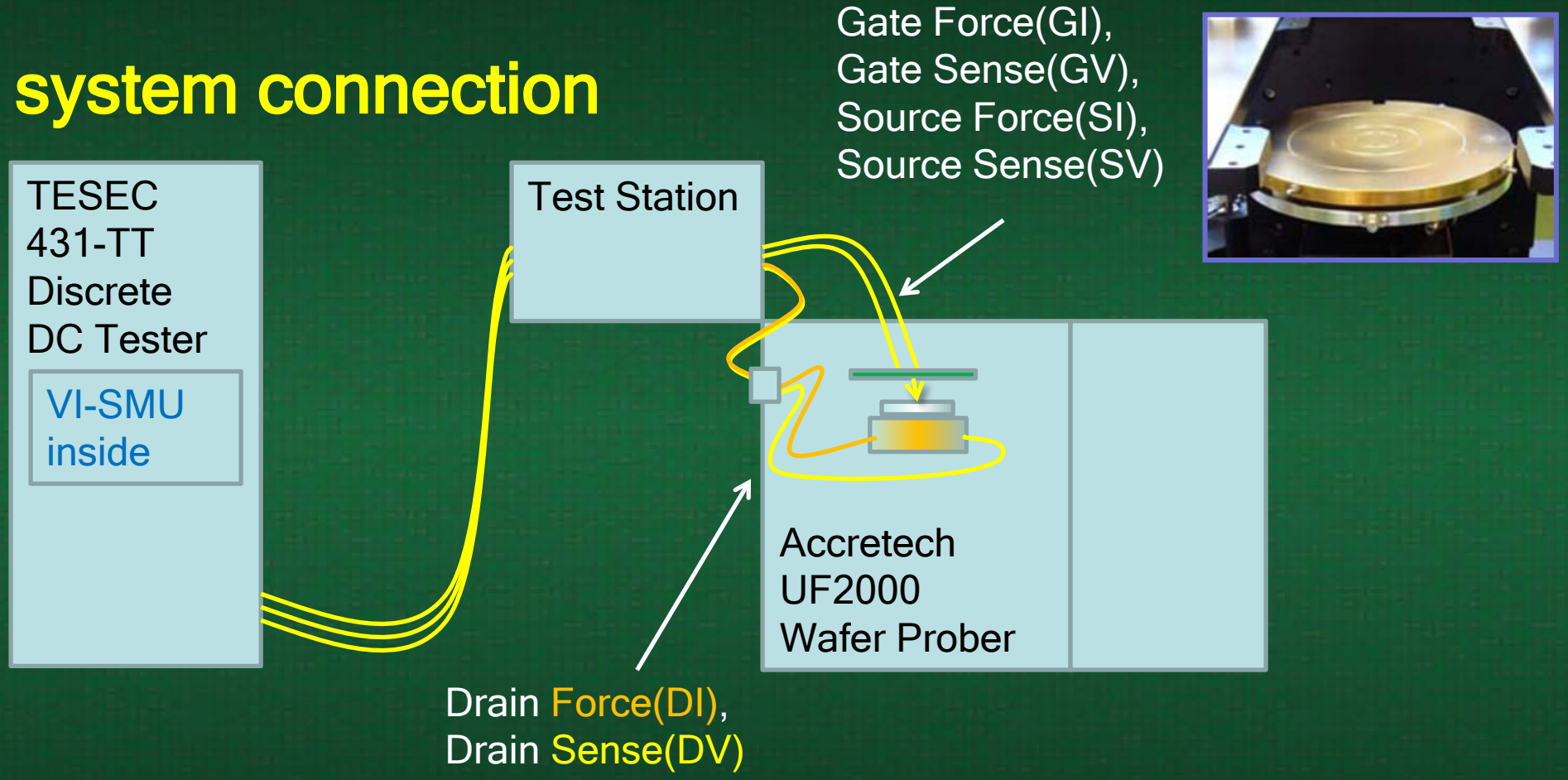


Comparison with standard stage



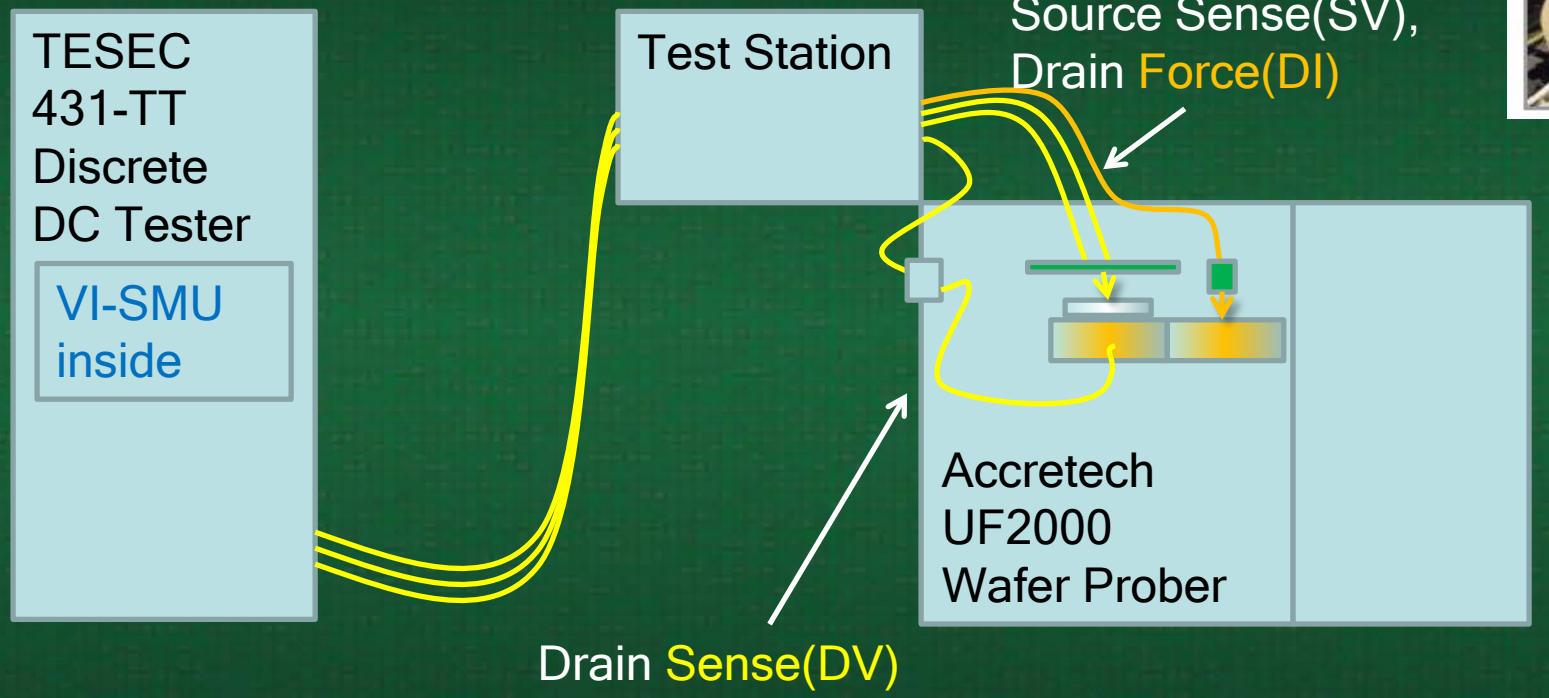
Comparison with standard stage

- **Standard system connection**



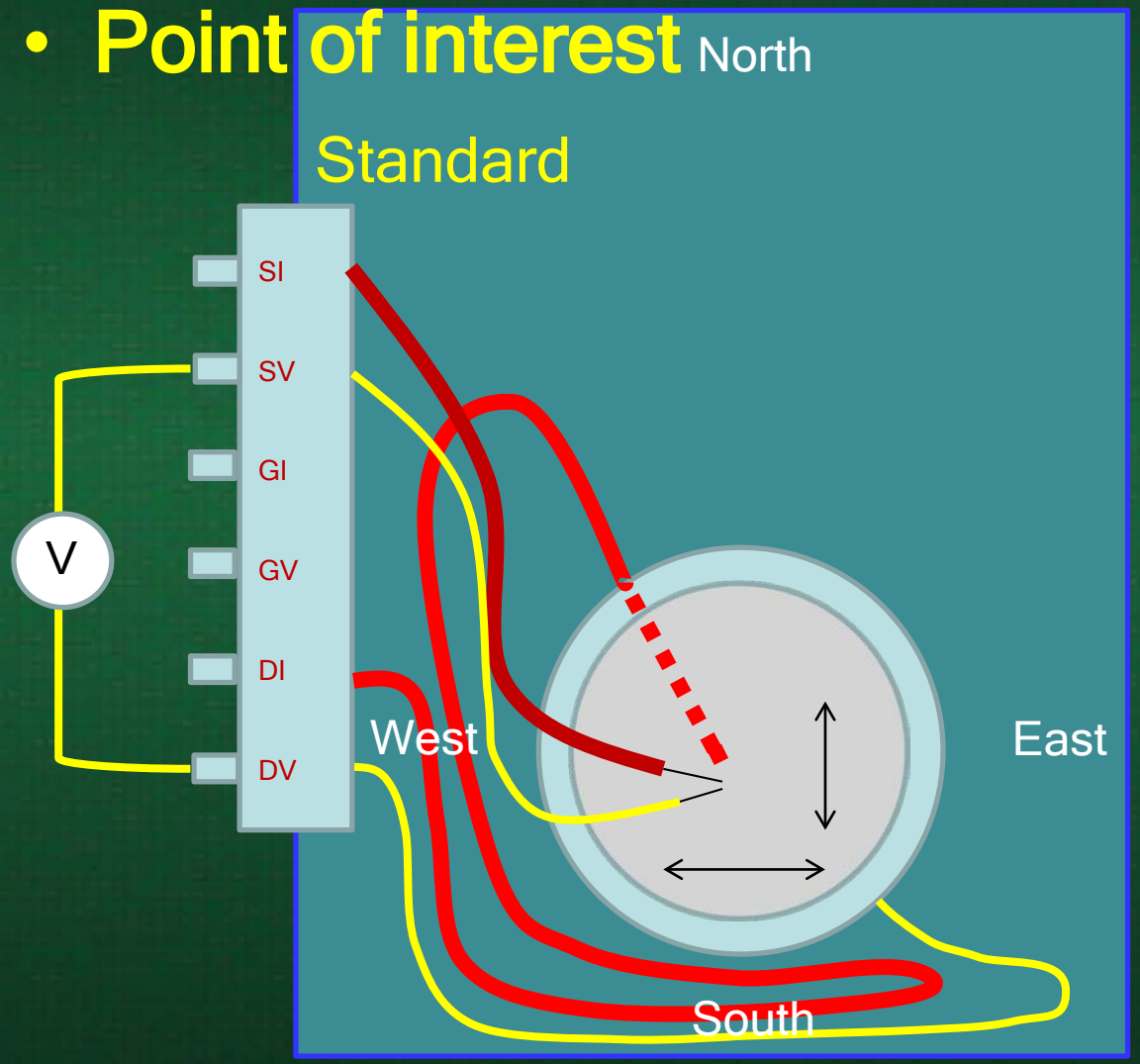
Comparison with standard stage

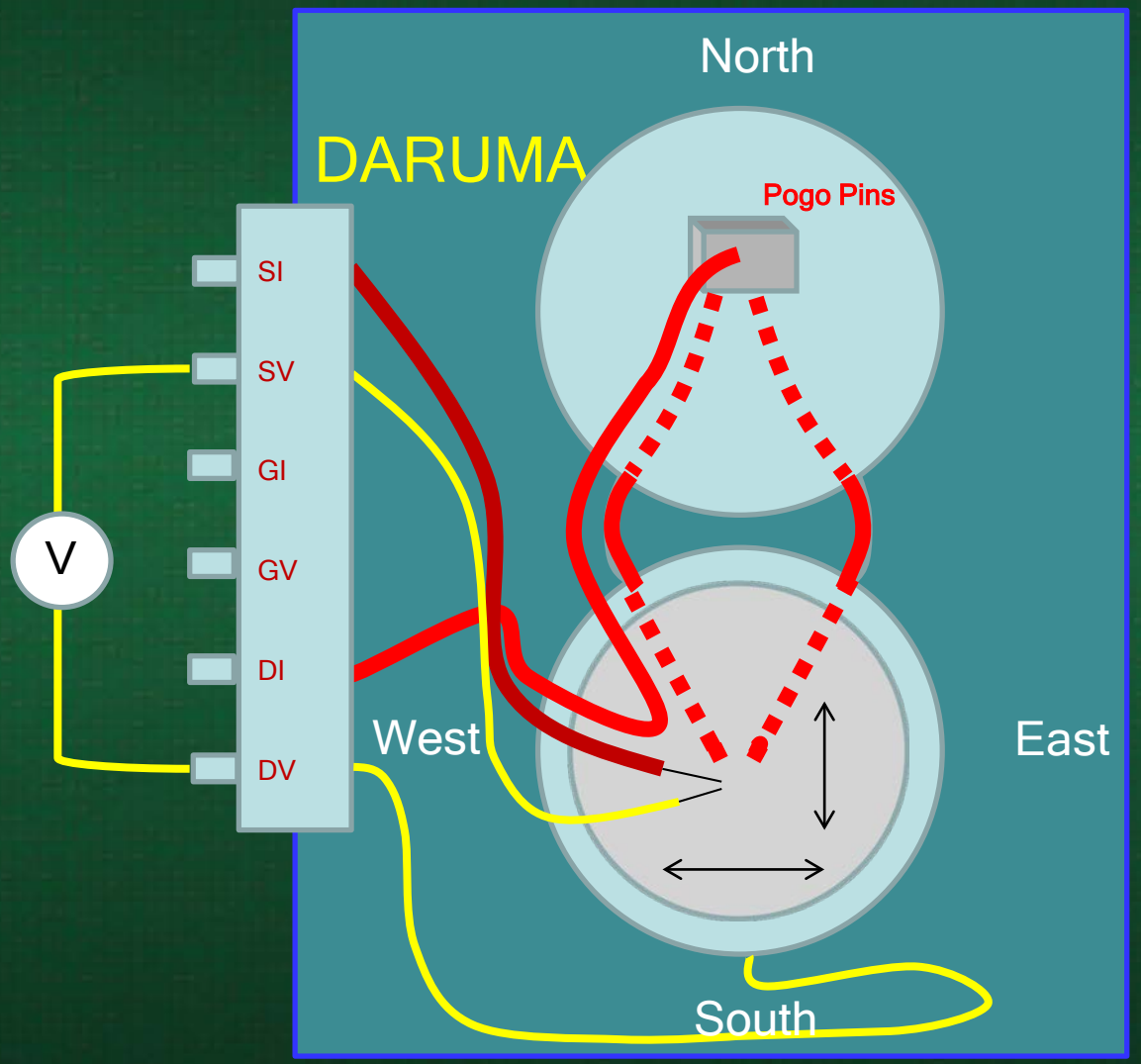
- DARUMA system connection



Comparison with standard stage

- **Point of interest**





Comparison with standard stage

- **Point of interest**

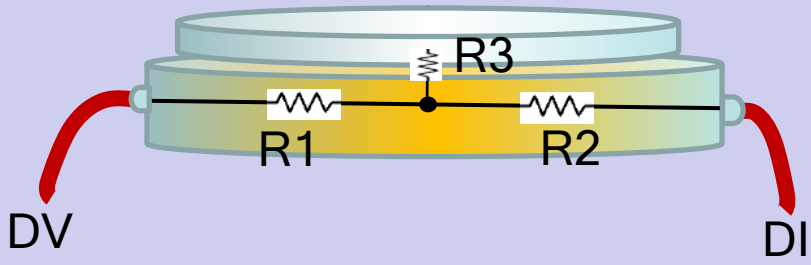
Device Connection Comparison Table
Standard vs DARUMA

	Standard	DARUMA
GV	Probe Card	←
GI	Probe Card	←
SV	Probe Card	←
SI	Probe Card	←
DV	South East of the Stage	South of the Stage
DI	North West of the Stage via 2m Wire	North of the Stage via DARUMA

Comparison with standard stage

- Point of interest

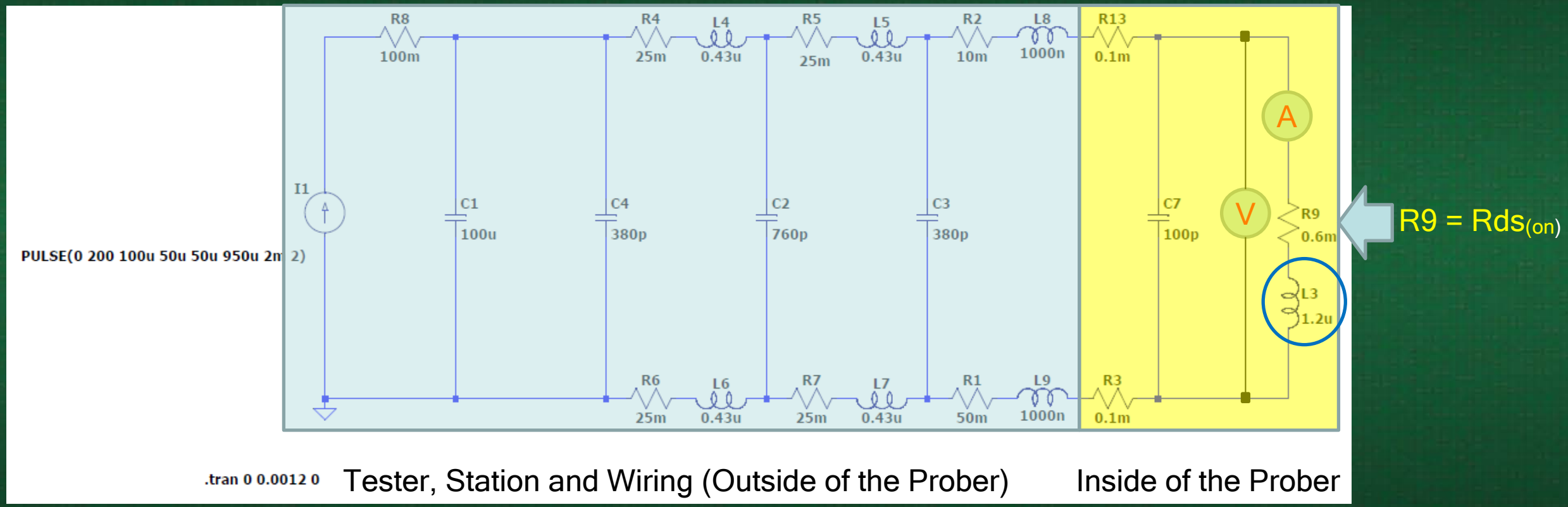
R3 is Contact resistance between Wafer and Stage.



R1 and R2 do not affect to VDSON value.
R3 is added to VDSON.
It is only R3 that increases VDSON.
Measurement values are almost independent of location.

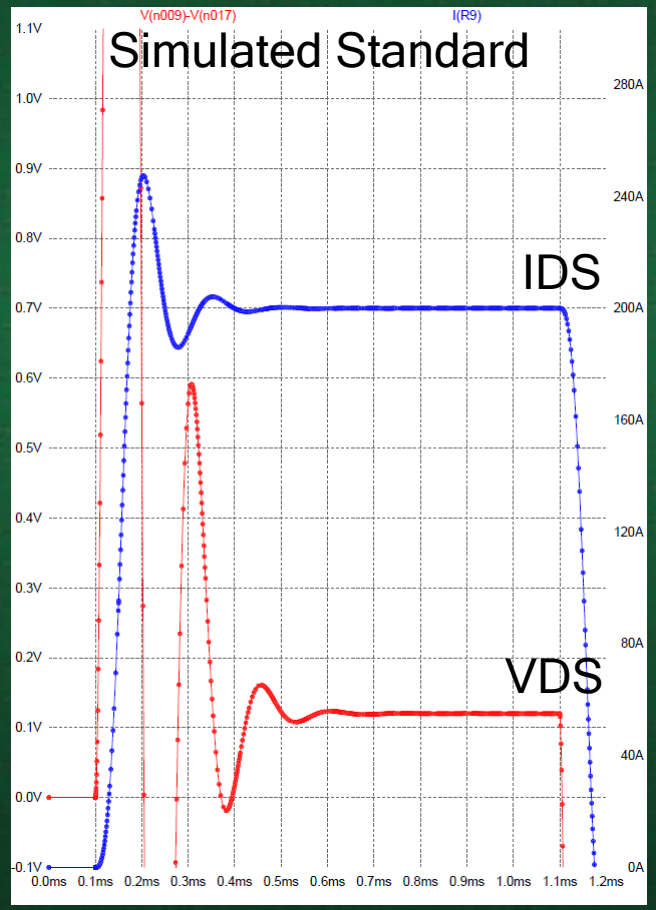
Simulation

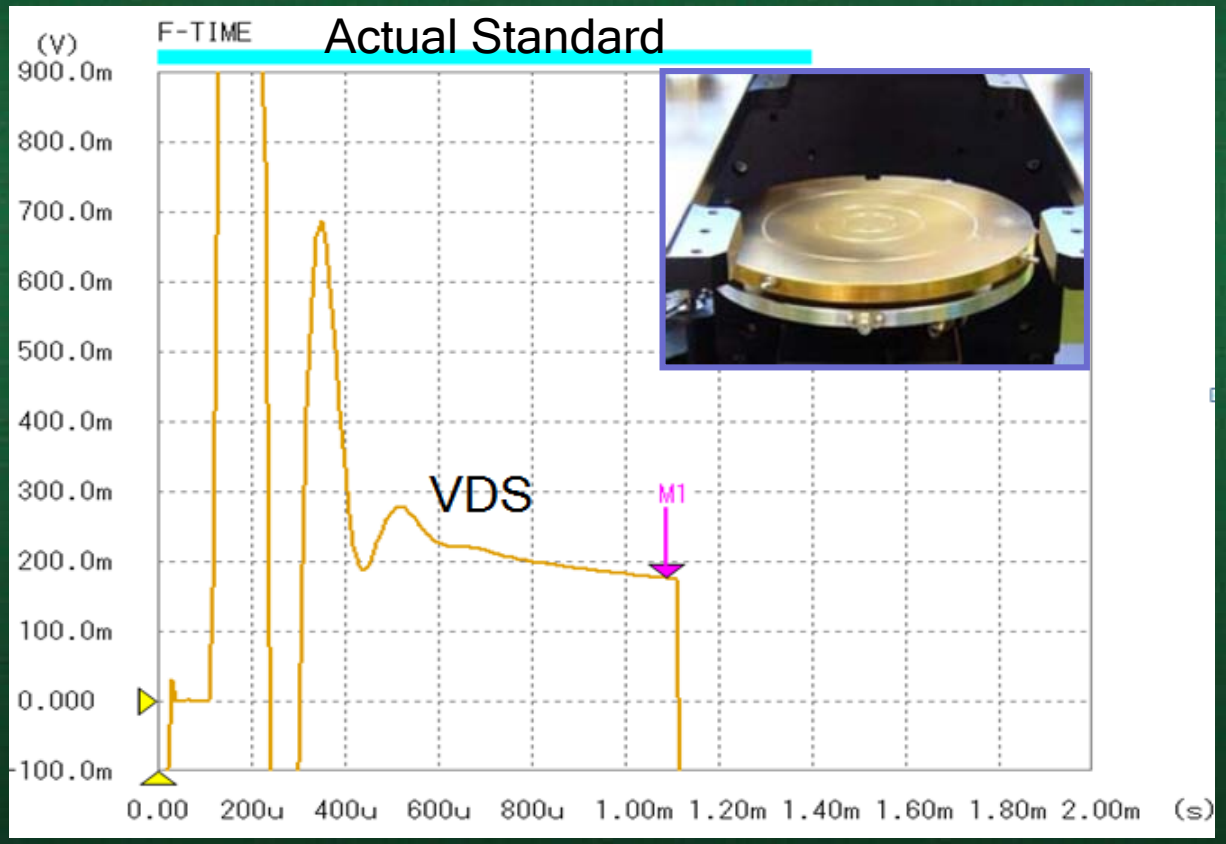
- Simulated model Schematics for Standard connection



Simulation

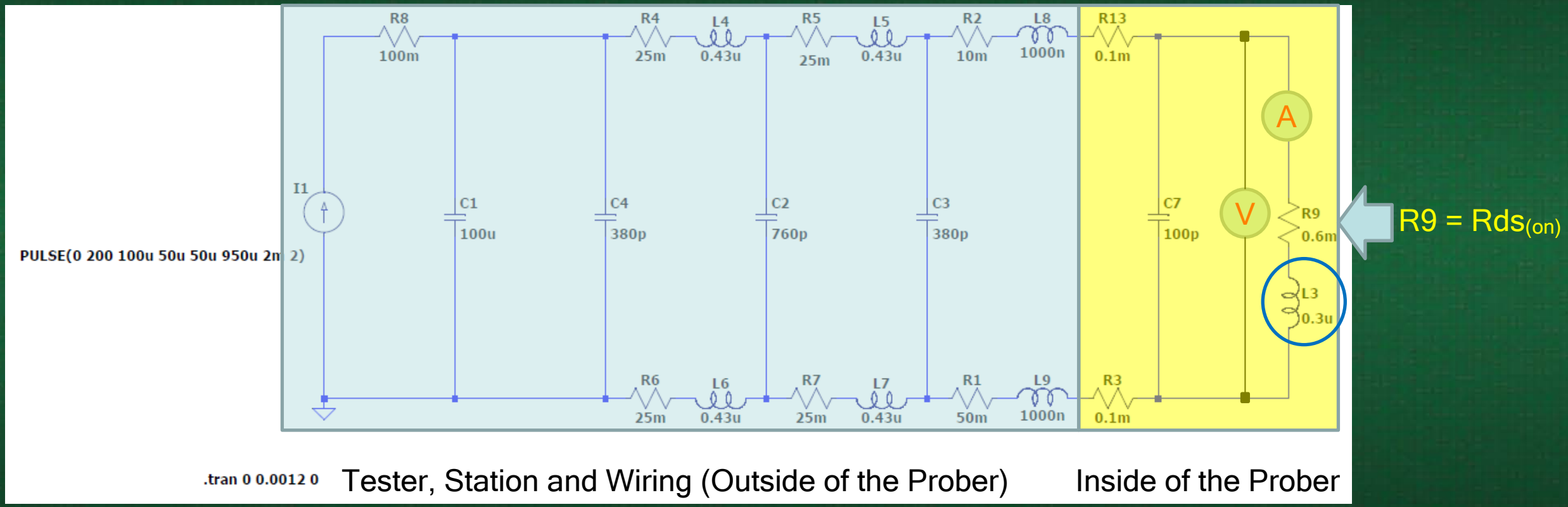
- Waveform Simulated vs Actual, @Standard





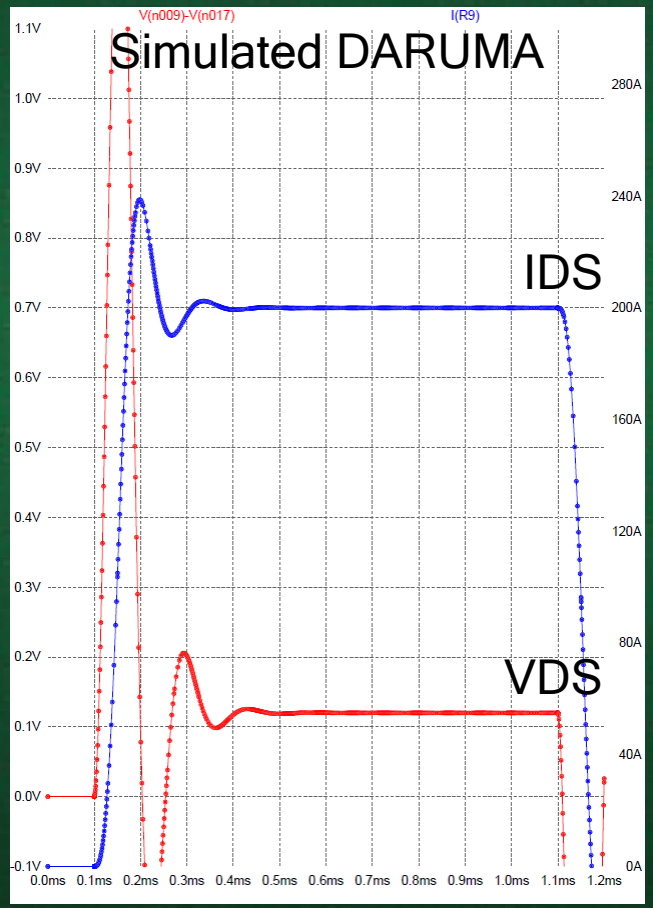
Simulation

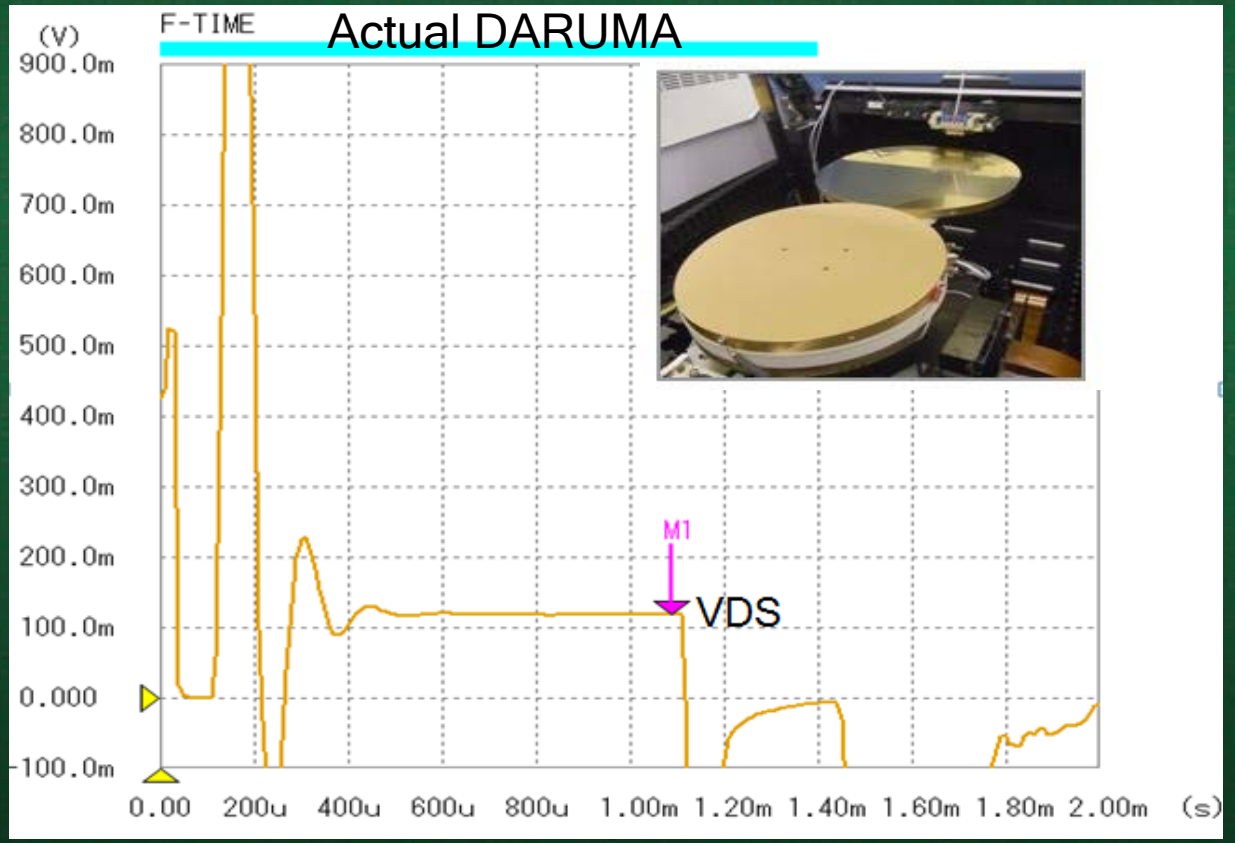
- Simulated model Schematics for DARUMA connection



Simulation

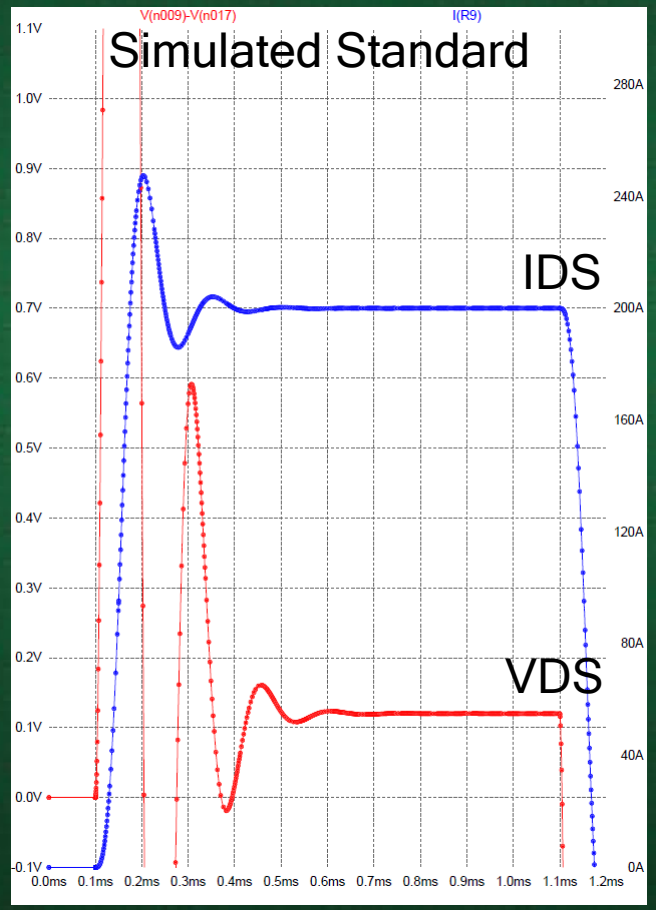
- Waveform Simulated vs Actual, @DARUMA

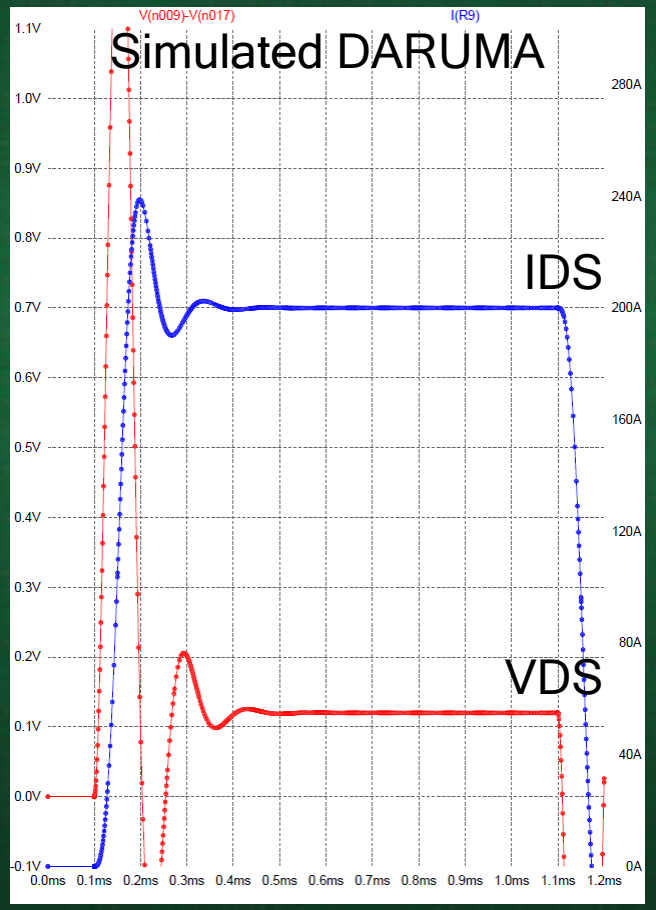




Simulation

- Simulated Waves comparison Standard vs DARUMA





Conclusion

- Demand for higher-efficiency of Mobile and Automotive devices, is driving the need for MOSFETs with even lower **$Rds_{(on)}$** .
- Improving measurement accuracy while at the same time reducing device stress will continue to be test challenges for the future.
- However, by employing a “DARUMA” stage, these test challenges can be met at wafer probe when testing ($Rds_{(on)}$) on MOSFETs. Ls will be minimized to enable reduced test time (especially at high current). By reducing test time, temperature rise will be reduced producing less stress on the DUT also resulting in more stable and accurate measurements.

Acknowledgements

We would like to thank the following colleagues for supporting this workshop.

ACCRETECH

Yuji SHIGESAWA
Tomoyuki MYOJO
Shoji TERADA

TESEC®

Yuichi KAKIZAKI
Kiyoaki KOYAMA
Muneo ISHINOHACHI
Masashi HOSHINO

- We hope these efforts bring further development of products that will contribute to societal advancements.

Thank you