SW Test Workshop
Semiconductor Wafer Test Workshop

A Proposal of Multi Para CIS Probe Card Concept for Improvement of PI/SI

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WILL TECHNOLOGY
Wafer Inspection Leading Lab

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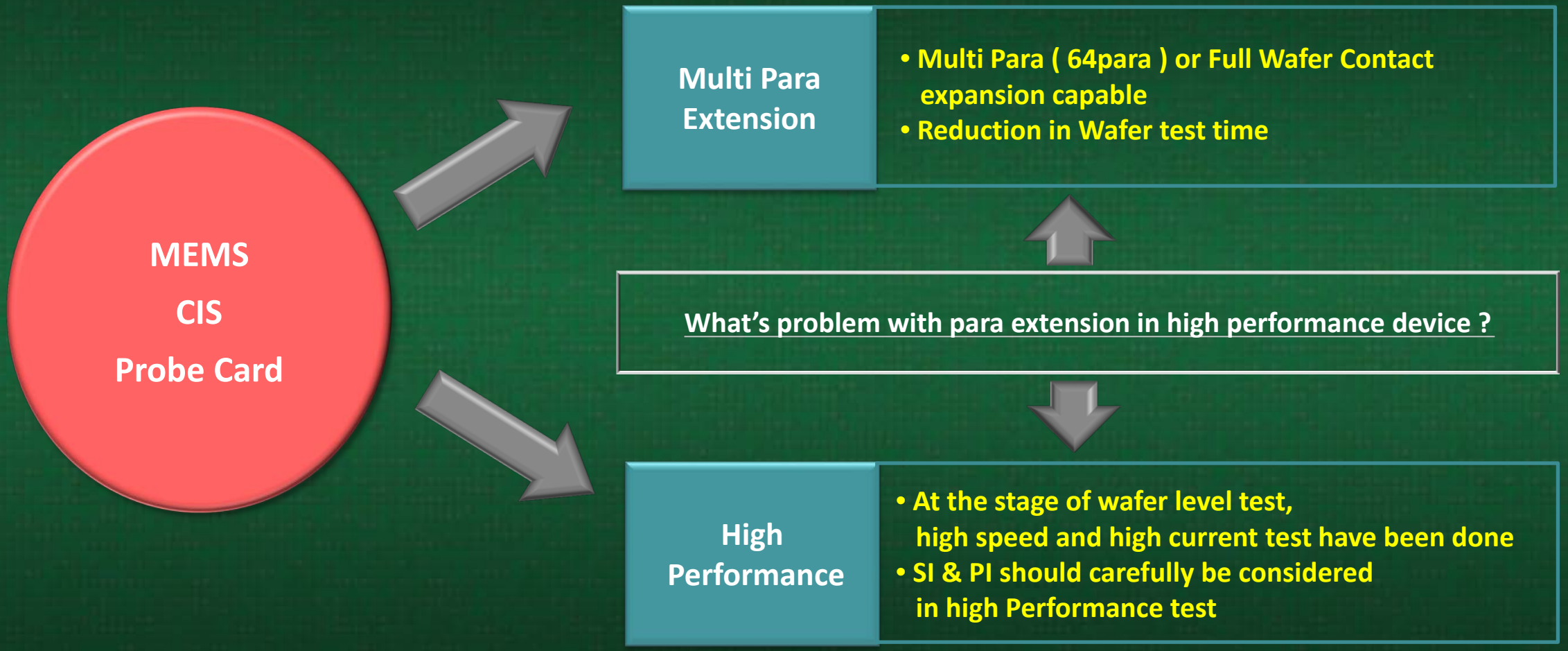
Overview

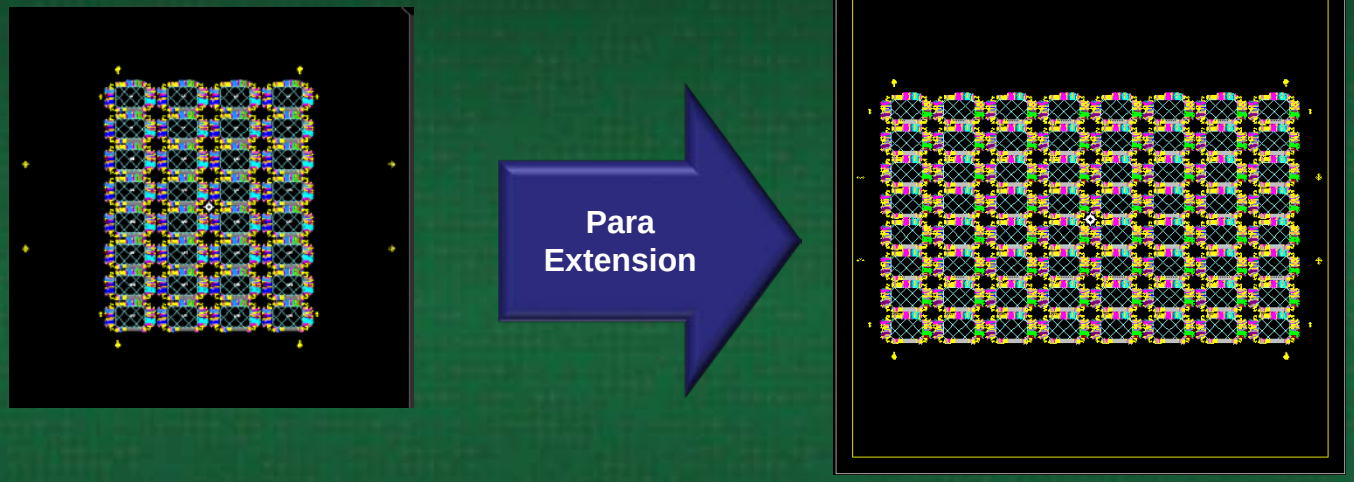
- **Introduction**
- **Problem due to Para Extension**
- **Design Concept**
- **Improve Power Integrity**
  - DC Resistance
  - AC Power Impedance
- **Improve Signal Integrity**
  - Insertion Loss
  - Eye Diagram
- **Conclusion & Future work**

Introduction



Problem due to Para Extension

- **CIS Probe Card Para Extension**

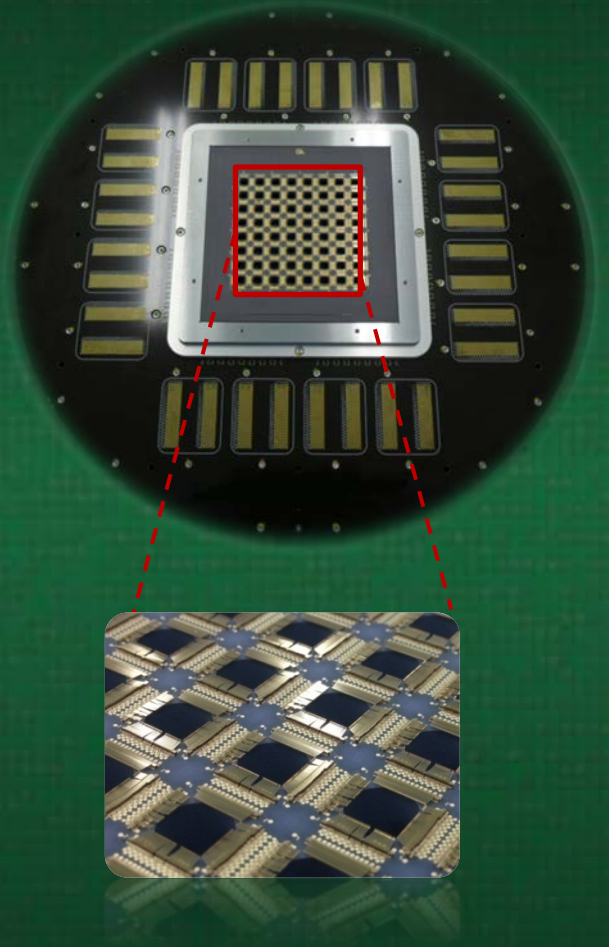


Benefit

- Reduction in Wafer test time

Problem

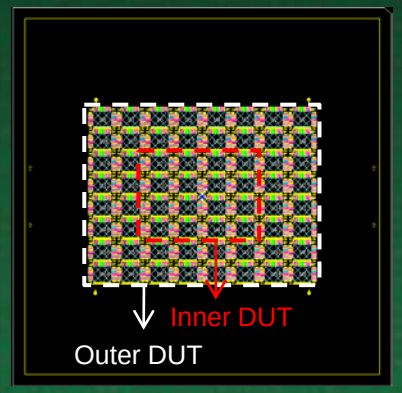
- Deviation between DUTs
- PI / SI degradation



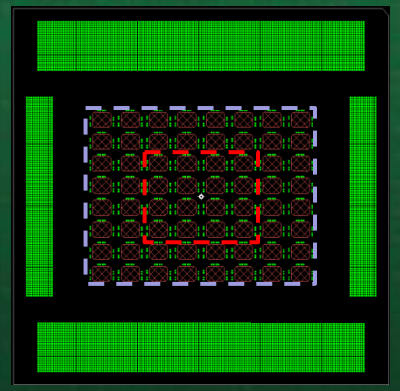
< 64Para MEMS CIS Probe Card >

Problem due to Para Extension

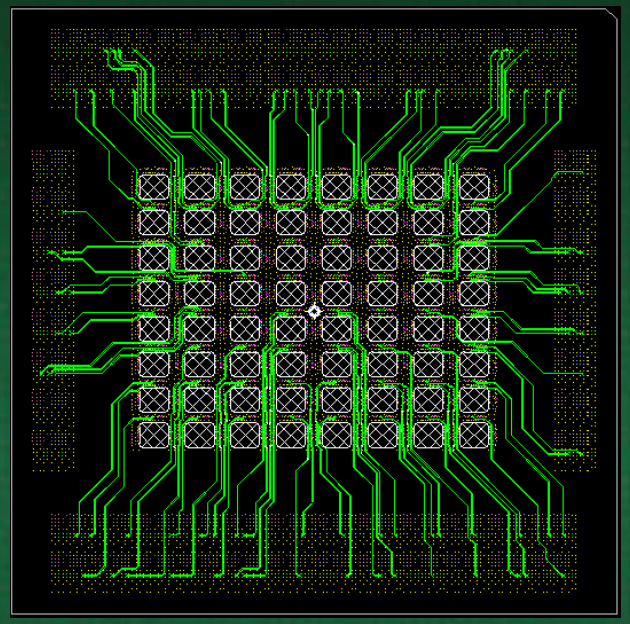
- **MLC Design**



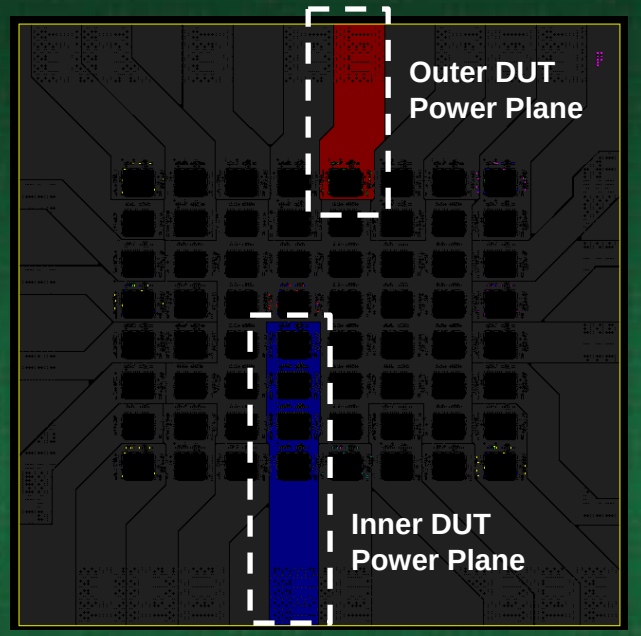
[MLC Top]



[MLC Bottom]



[Signal Layer]



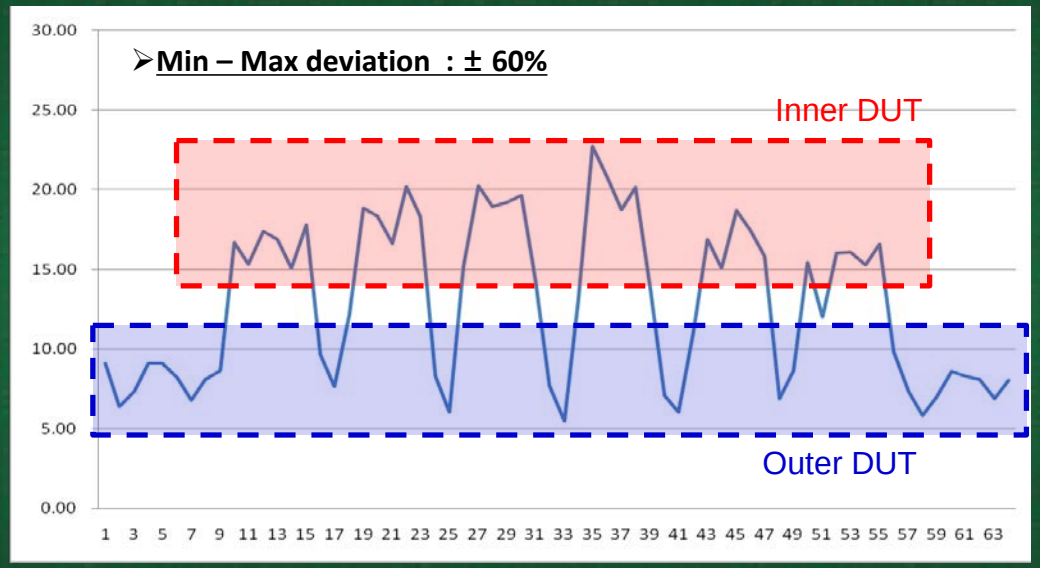
[Power Layer]

Weak Point	• As para extension, there is a physical distance difference between inner and outer DUT • It cause SI & PI deviation between DUTs • Higher Performance devices can cause more serious problems

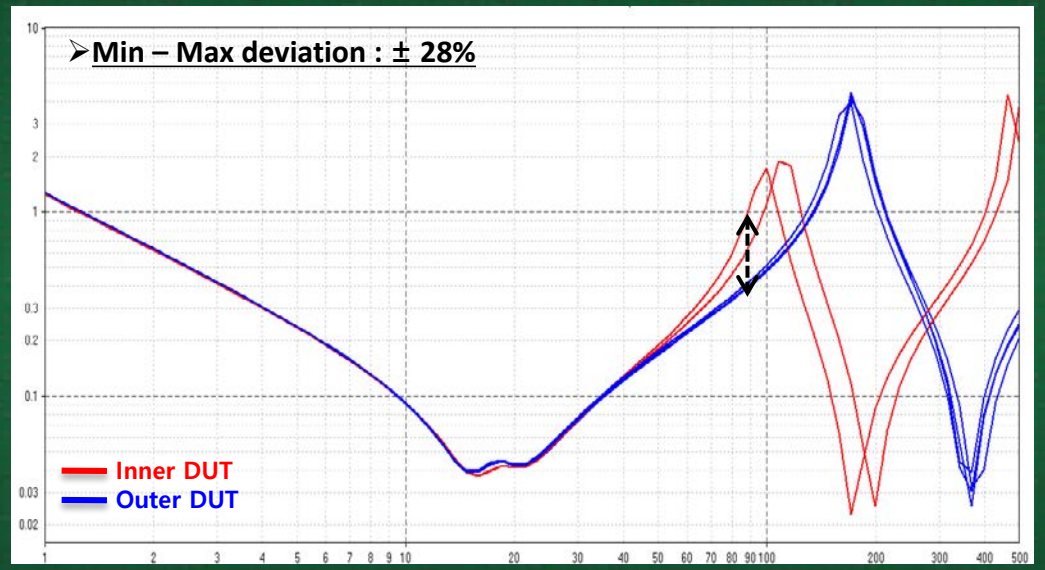
Problem due to Para Extension

- **PI Deviation between DUTs**

[Power DC Resistance]



[PDN Impedance]

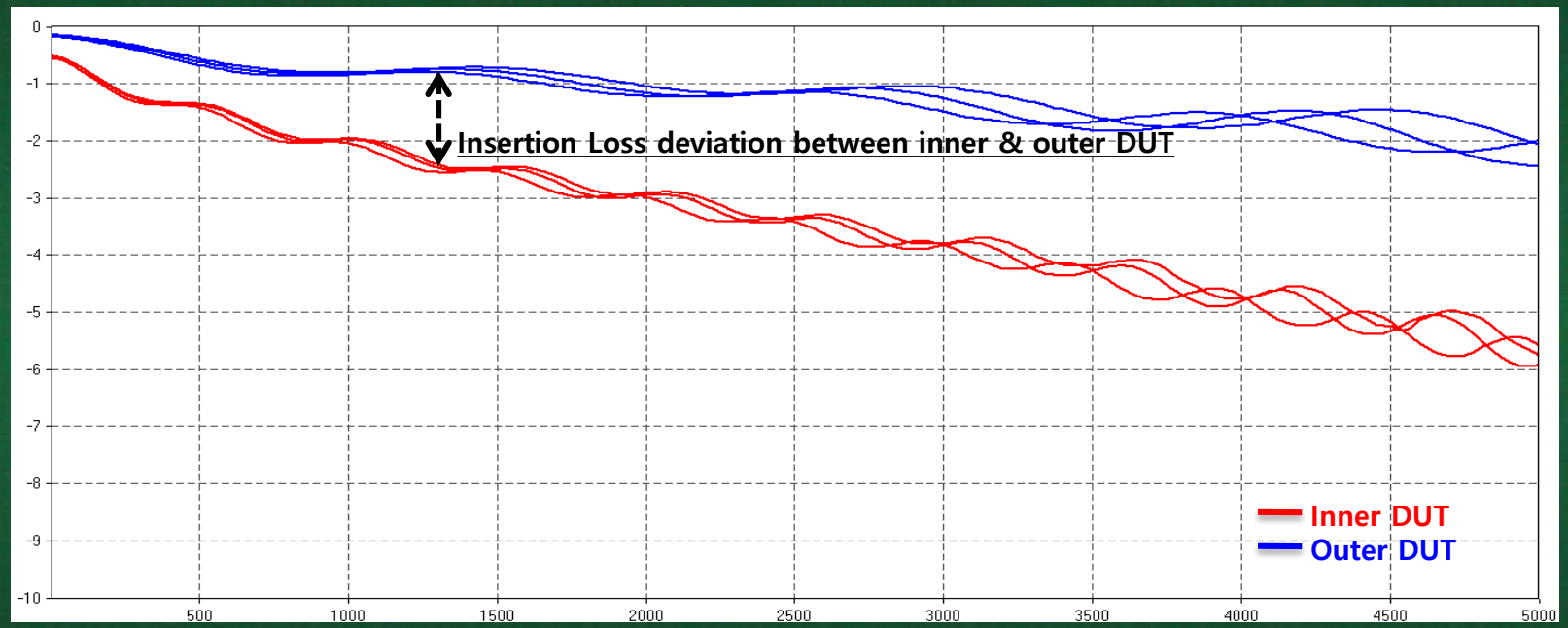


- Power DC Resistance Min - Max Deviation between DUTs is about ± 60%
- PDN impedance Min - Max Deviation between DUTs is about ± 28%
- These are two simulation results that shows deviation of PI by para extension

Problem due to Para Extension

- **SI Deviation between DUTs**

[MIPI Channel Insertion Loss]



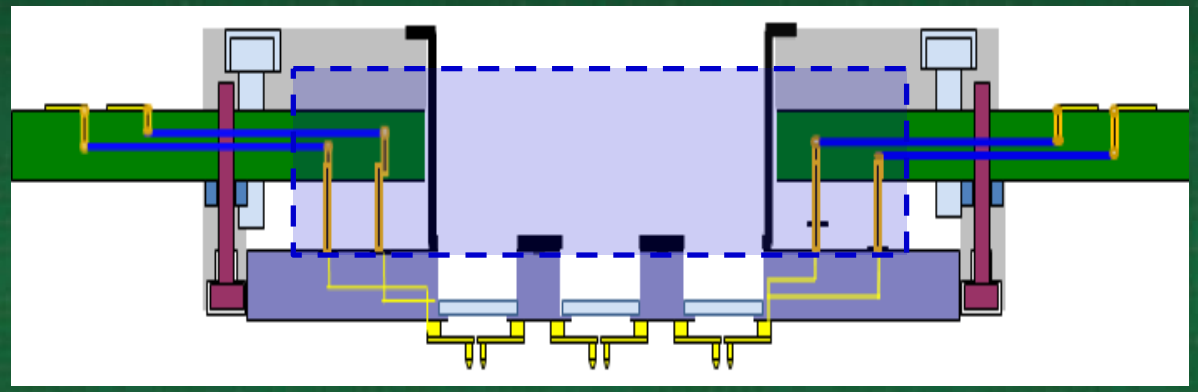
- **Inner DUT has relatively high insertion loss level compared to the outer DUT**

How to improve Deviation between Inner & Outer DUT ?

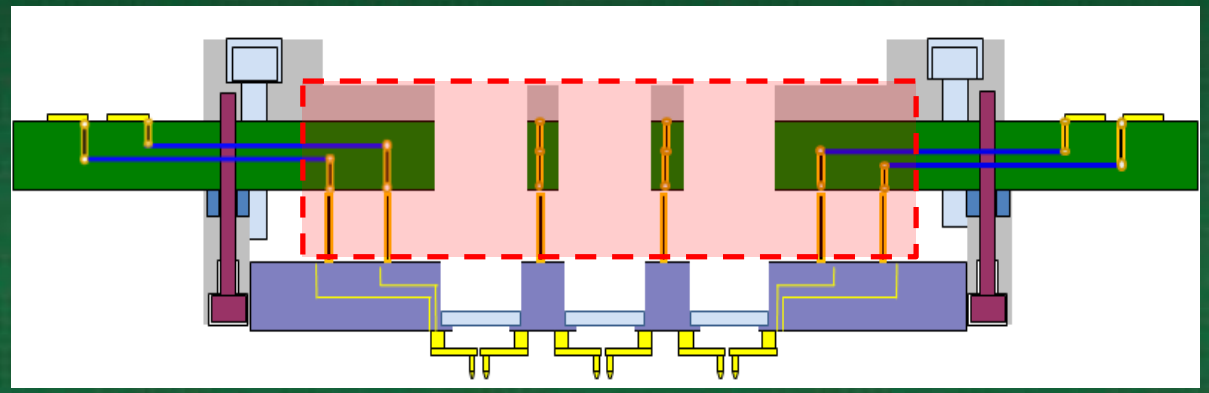
Design Concept

- **Probe Card Structure**

[Origin Concept]



[New Concept]

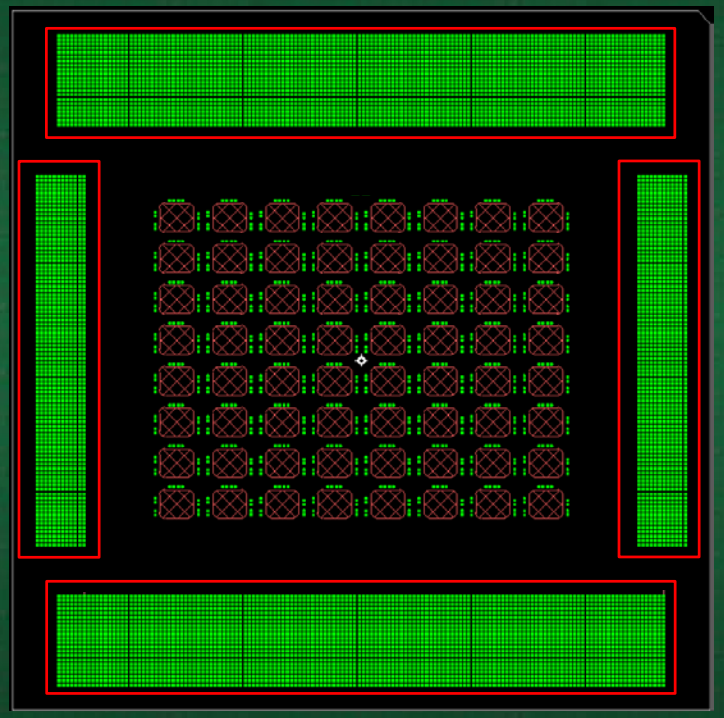


	Origin Concept	New Concept
STF	MLC	
LGA Location on STF	Outside DUT Area	Inside DUT Area & Outside DUT Area

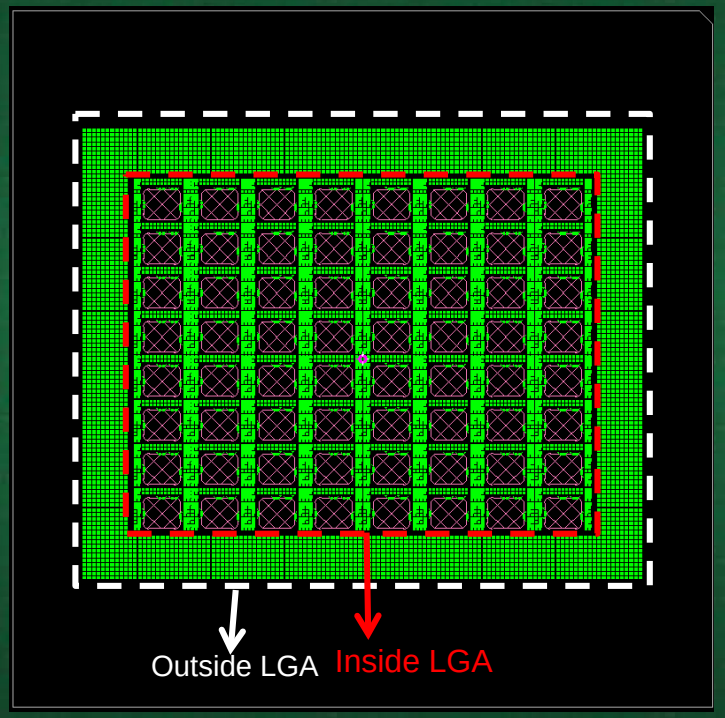
Design Concept

- **MLC Design**

[Origin Concept]



[New Concept]

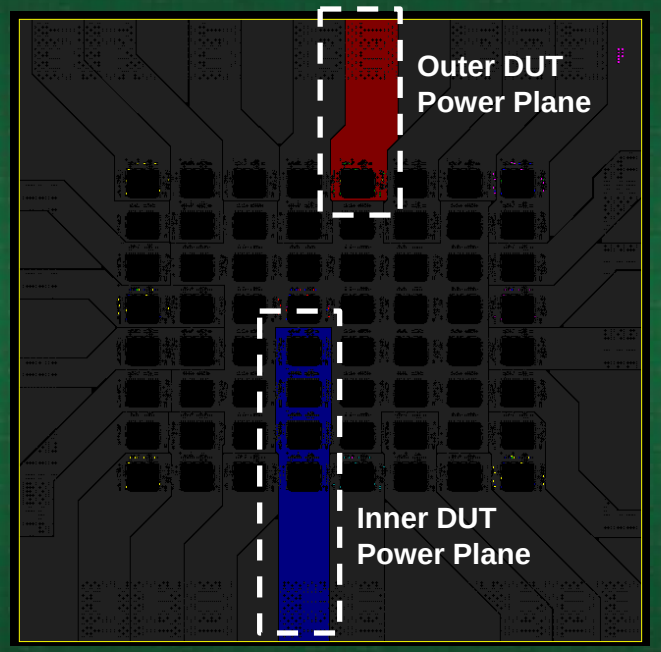


- Add LGA to DUT area
- Inside LGA Area - High Speed (ex. MIPI) & High Current Power placed

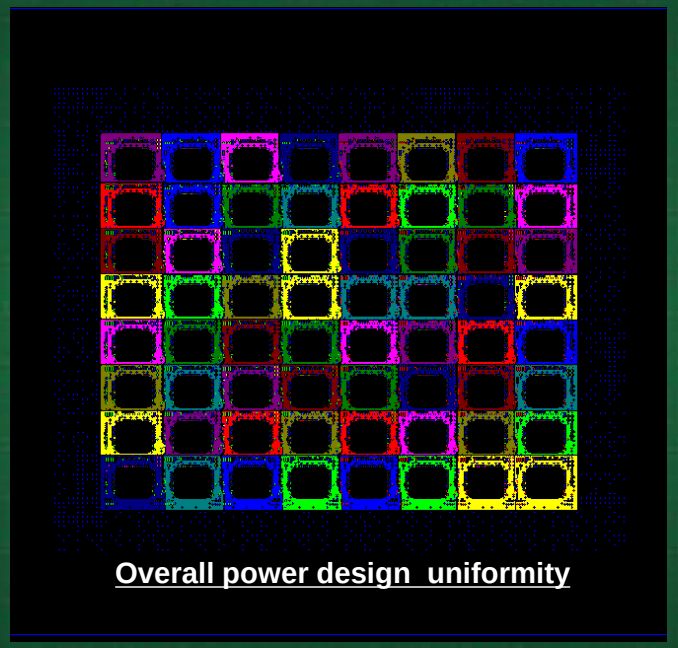
Design Concept

- **MLC Power Design**

[Origin Concept]



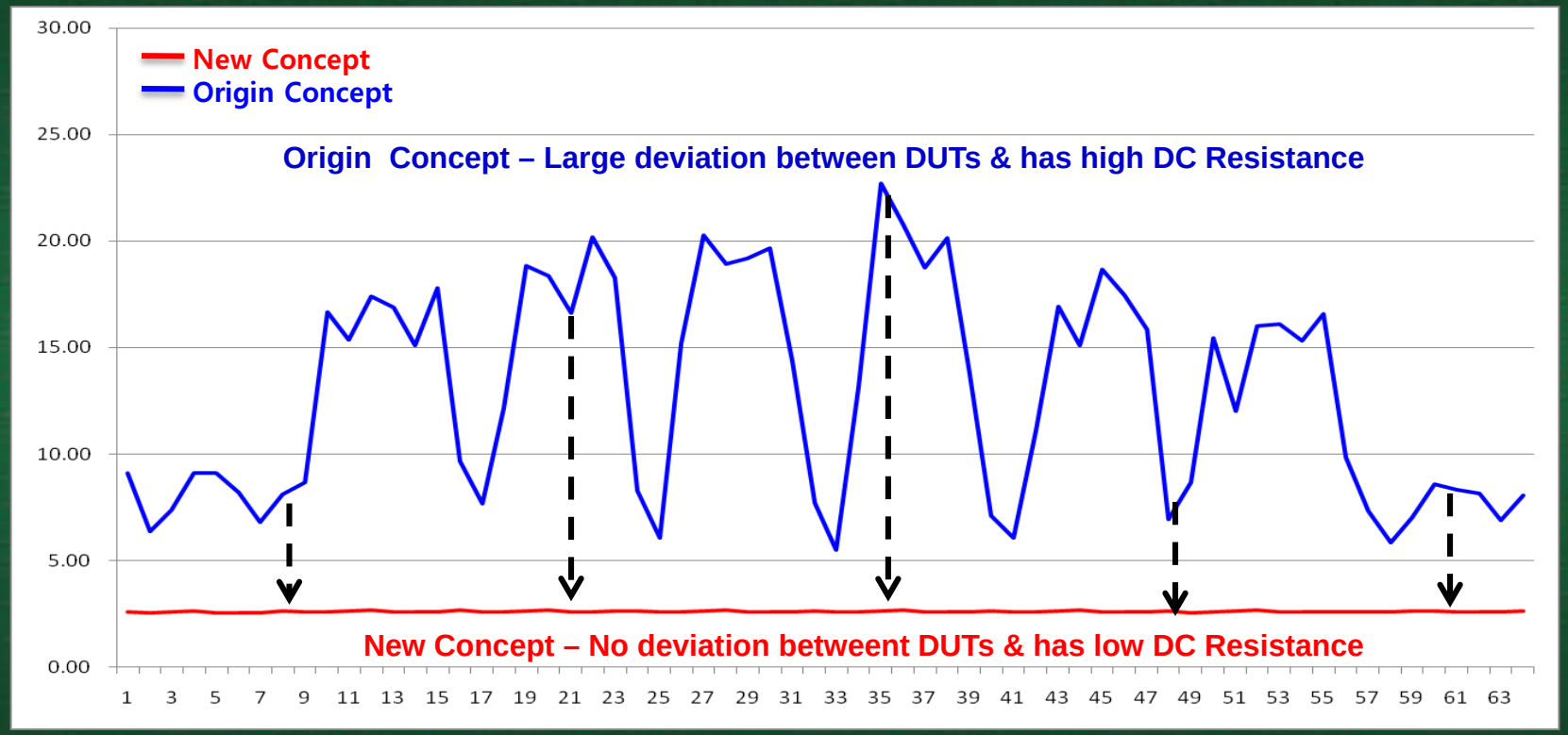
[New Concept]



MLC Power Design	• Long Path length between DUT - LGA • Different design for each DUT • Required No. of Layer : Over 4 Layer	→ • Short Path length between DUT - LGA • Same design for all DUT • Required No. of Layer : Under 2 Layer

Improve Power Integrity

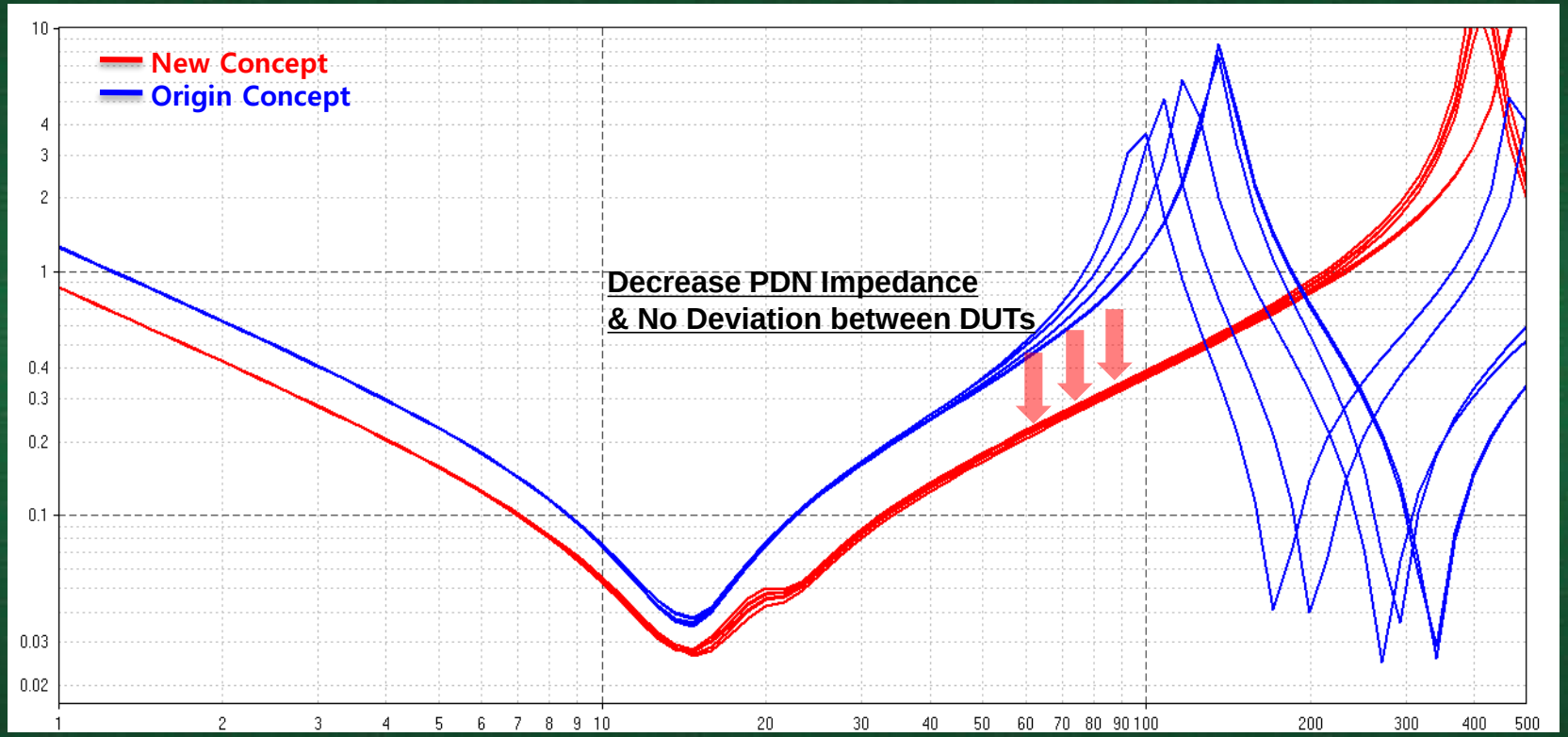
- **Power DC Resistance**



- Deviation between DUTs of less than ±2% in New Concept
- DUT - LGA Path is shortened, DC resistance reduced by more than 50%

Improve Power Integrity

- **PDN Impedance**

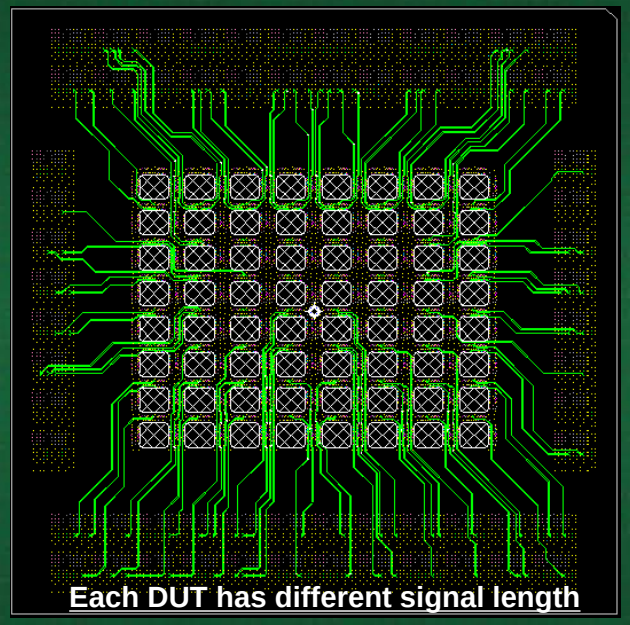


Improved PDN Impedance & Deviation between DUTs.

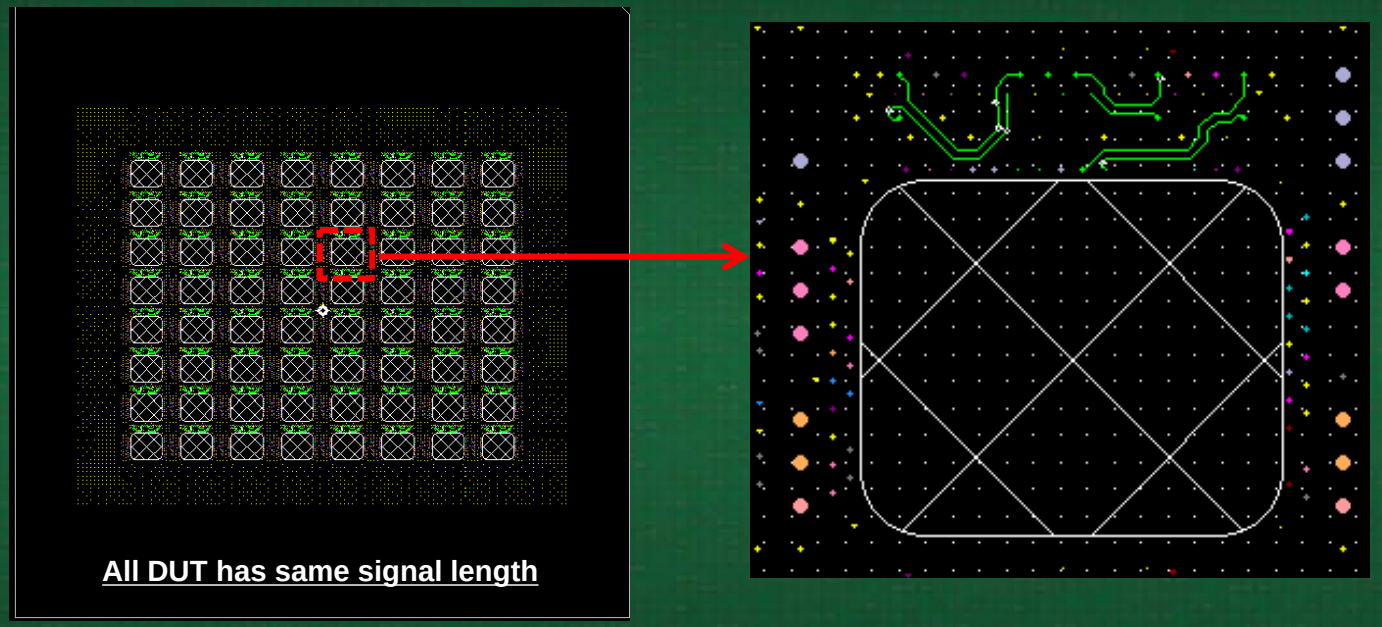
Improve Signal Integrity

- **MLC Signal Design**

[Origin Concept]



[New Concept]



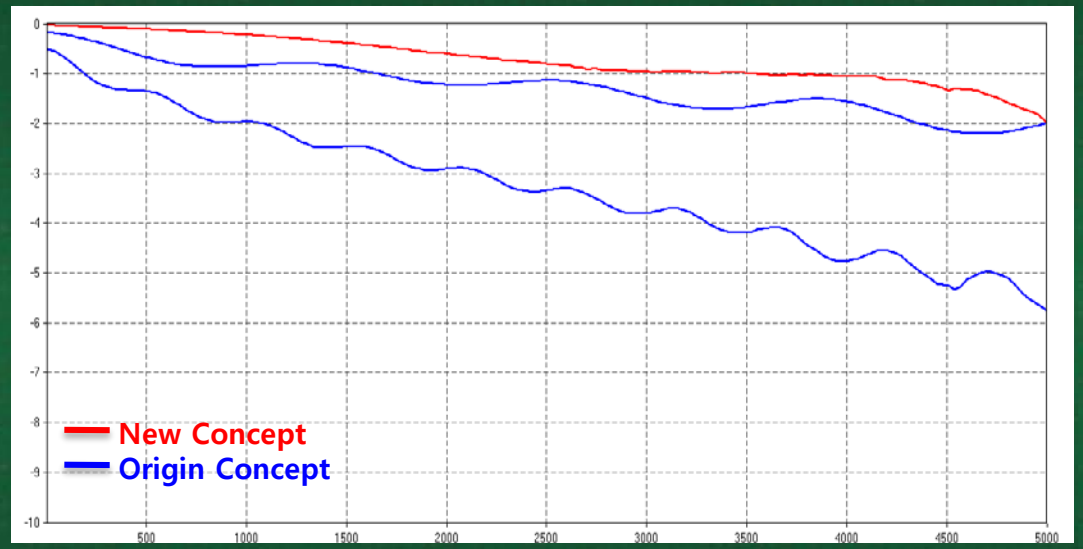
	Origin Design	New Design
Signal Length (mm)	25 mm ~ 65 mm	5mm Under

Improved SI performance due to shortened MLC trace length

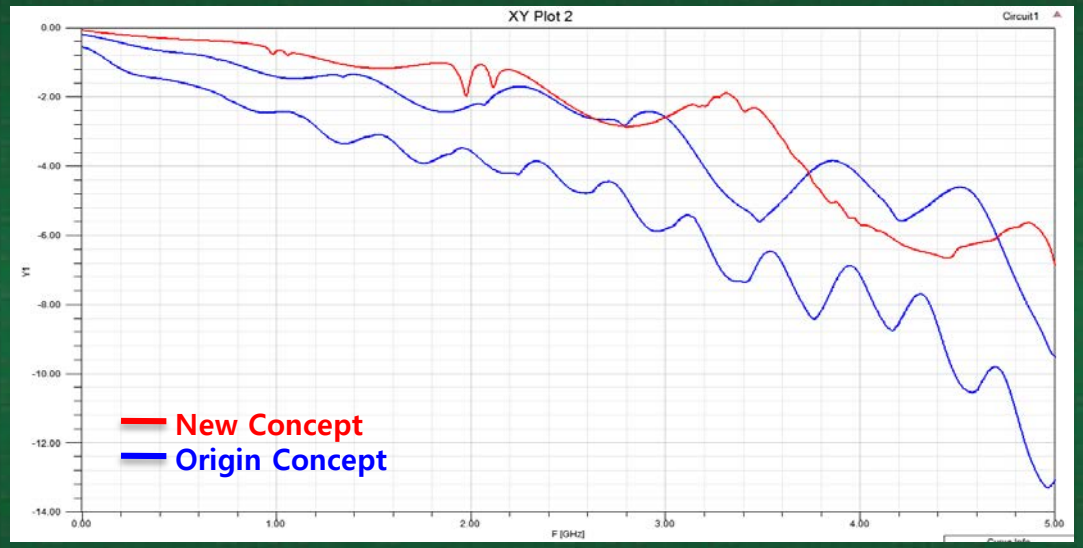
Improve Signal Integrity

- **Signal Integrity (Insertion Loss)**

[Insertion Loss _ MLC Only]



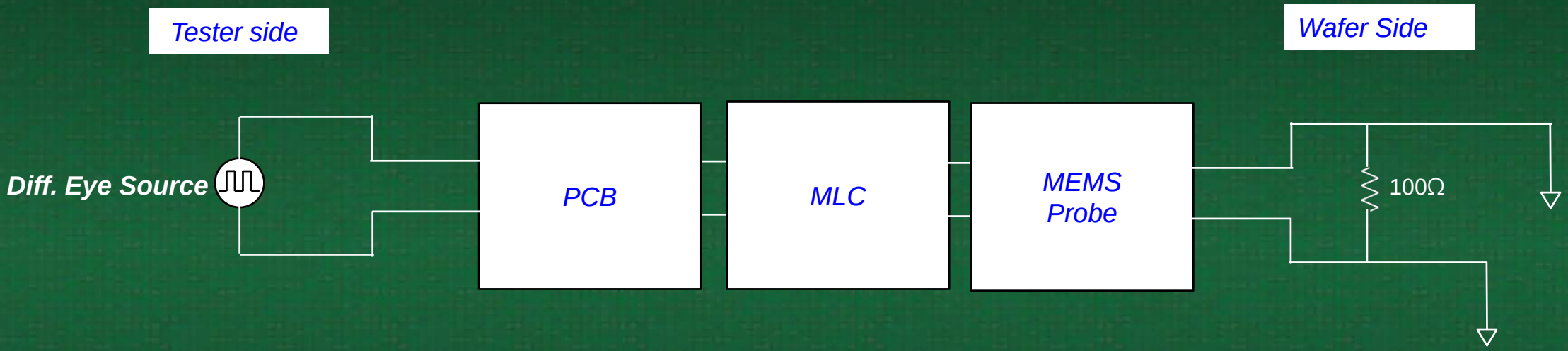
[Insertion Loss _ Full Path]



검토 항목	Insertion Loss (S21) @ 1.2GHz	
	Origin Design	New Design
MLC Only	-0.8 dB ~ -2.4 dB	-0.3 dB
Full Path	-1.9 ~ -3.1 dB	-1.0 dB

Improve Signal Integrity

- **Differential Eye Simulation Condition**

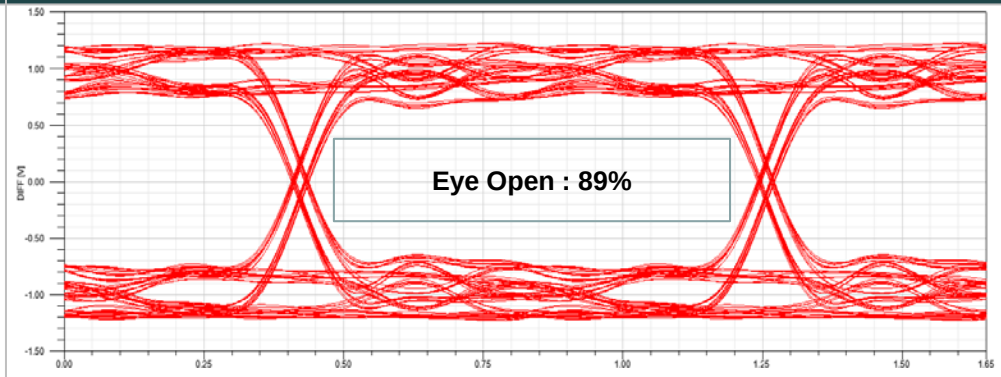
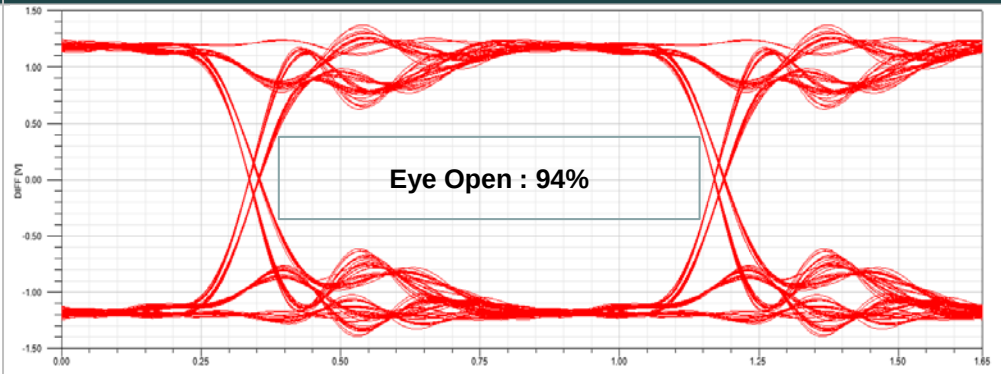
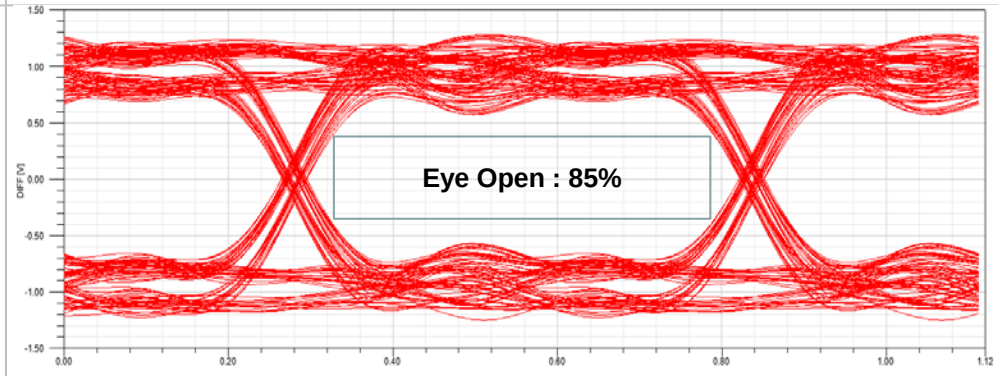
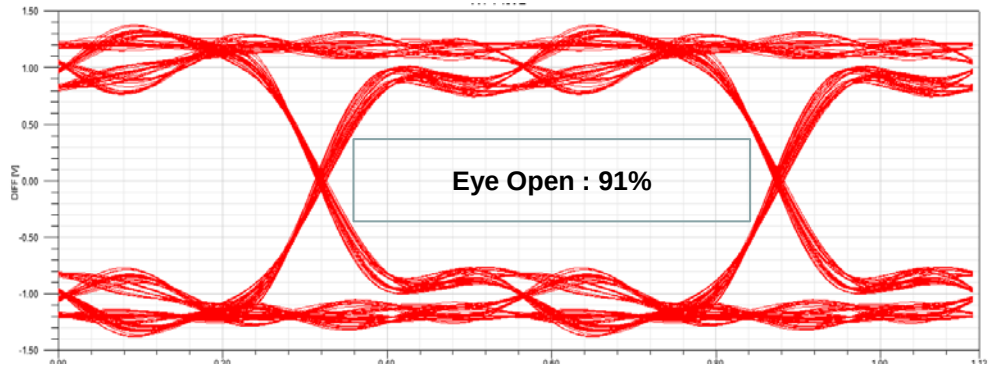


- Simulation Setup

- Input Voltage : 1.2 V
- Data rate : 1.2 / 1.8 / 2.4 / 3.2 Gbps
- Rise / Fall Time : UI/4
- Differential Impedance : 100 ohm
- Data pattern : PRBS 2^5

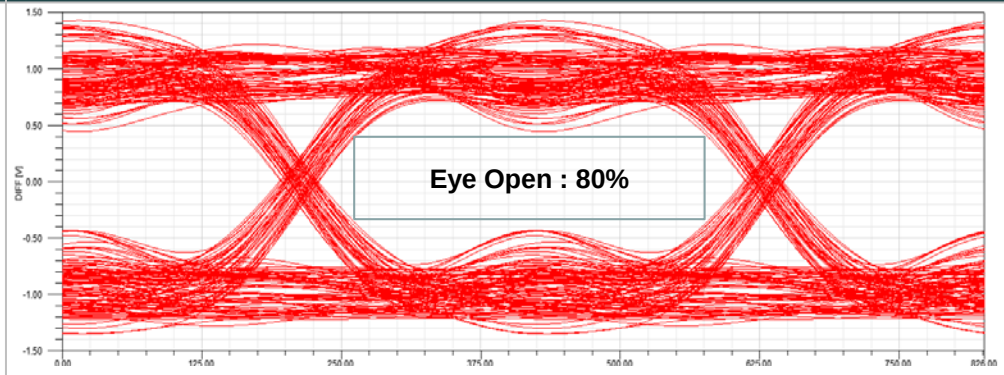
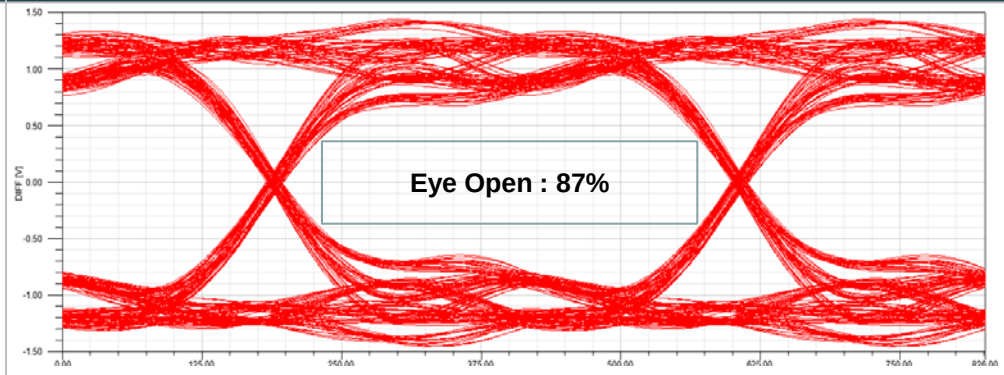
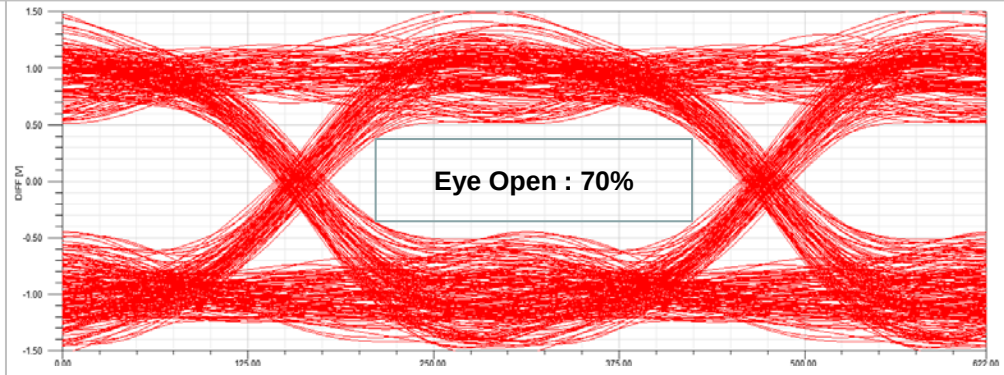
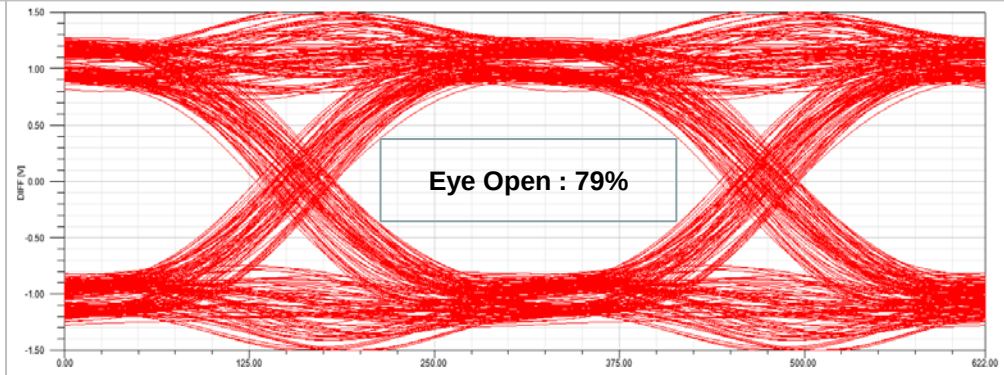
Improve Signal Integrity

- **Eye Diagram @ 1.2Gbps & 1.8Gbps**

Data rate	Eye Diagram	
	Origin Design	New Design
@1.2Gbps		
@1.8Gbps		

Improve Signal Integrity

- **Eye Diagram @ 2.4Gbps & 3.2Gbps**

Data rate	Eye Diagram	
	Origin Design	New Design
@2.4Gbps		
@3.2Gbps		

Conclusion

- Currently, there is a need for high performance and para expansion in the CIS probe card test .
- Para extension causes PI / SI degradation and deviation between DUTs
- We proposed a solution to solve this problem by placing LGA in the DUT Area
- Overall DUTs high current Power and high speed Signal designed uniformly
- Improvement of PI / SI
  - Improvement of PI and SI has been achieved through the new structure that has short DUT – LGA path length
- Reduce Deviation between inner and outer DUT
  - Overall design uniformity → Reduced the deviation between inner and outer DUT
- Further research required to solve mechanical problem
- Thanks.

Acknowledgements

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