SW Test Workshop
Semiconductor Wafer Test Workshop

Improvement of High Speed Testing through Signal Path Enhancement

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GLOBALFOUNDRIES

FEINMETALL
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Overview

- Introduction
- Problem statement
- Critical Probe Card Design Parameters for High Speed Testing
- Probe Cards Characterization and Comparison
- Conclusion

Introduction

- As IC technology advances, more components are integrated into a single chip to increase functionality and reduce cost of manufacturing
- Thus, effective and efficient wafer-level test systems are in demand to screen off failed chips before packaging to significantly decreases cost of manufacturing
- To test wafer precisely, at-speed test which conducts test at the actual operation speed (which is usually high)
- Thus, high performance probe cards are in demand, particularly at high speed

Problem Statement

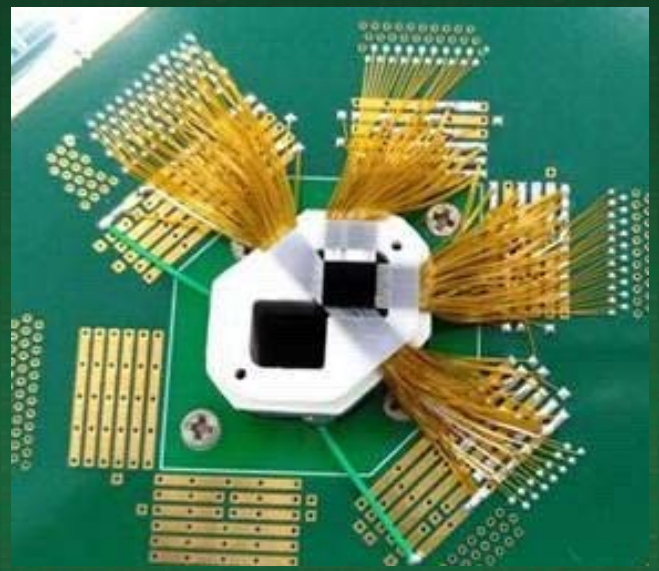
- We found that ordinary probe card consistently overkill particularly in some high speed test (eg. Mbist high speed, Core high speed test etc)
- We required high performance probe card for high performance ICs testing which required
  - ✓High pin count
  - ✓High operating frequency
  - ✓Good power distribution network
  - ✓Low crosstalk noise between needles

Knowing Probe Card Critical Design Parameters

Design A

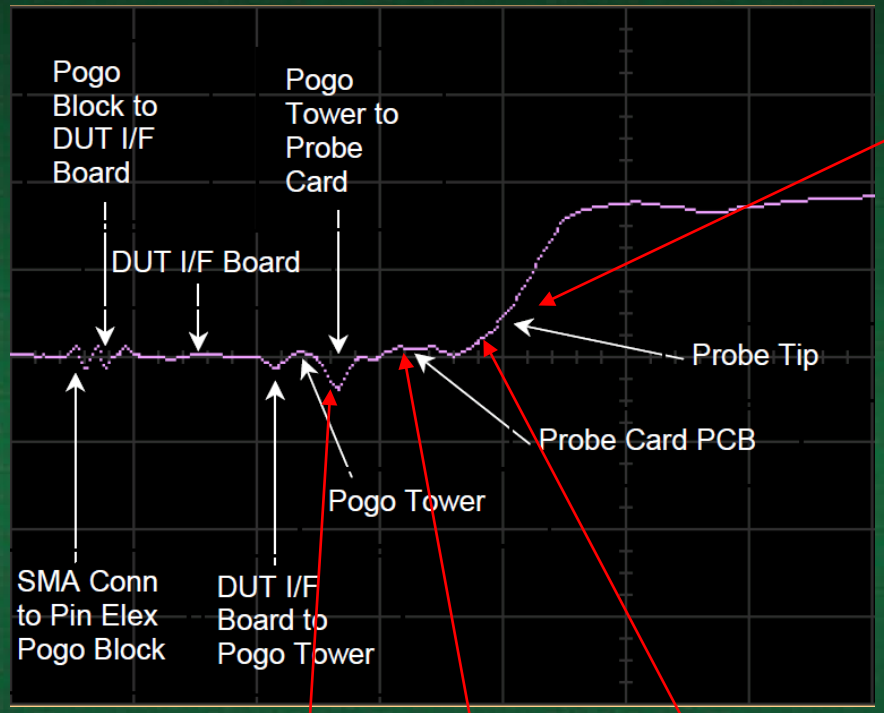
- ✓ Probe fan-out on 4 sides to better improve probe clearance.
- ✓ Identify critical signals and shielding it for cleaner electrical results.
- ✓ High grade epoxy with improve insulation properties.

Design B



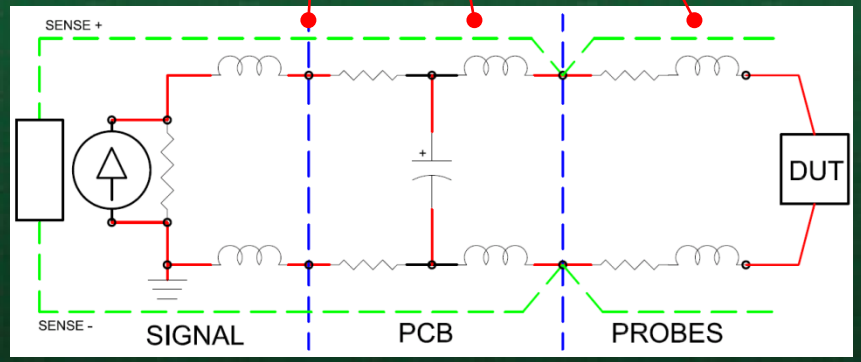
- ✓ Probe clearance reduce on 2 sides (diagonal side).
- ✓ Critical signals not shielded
- ✓ Low grade epoxy

Knowing Probe Card Critical Design Parameters



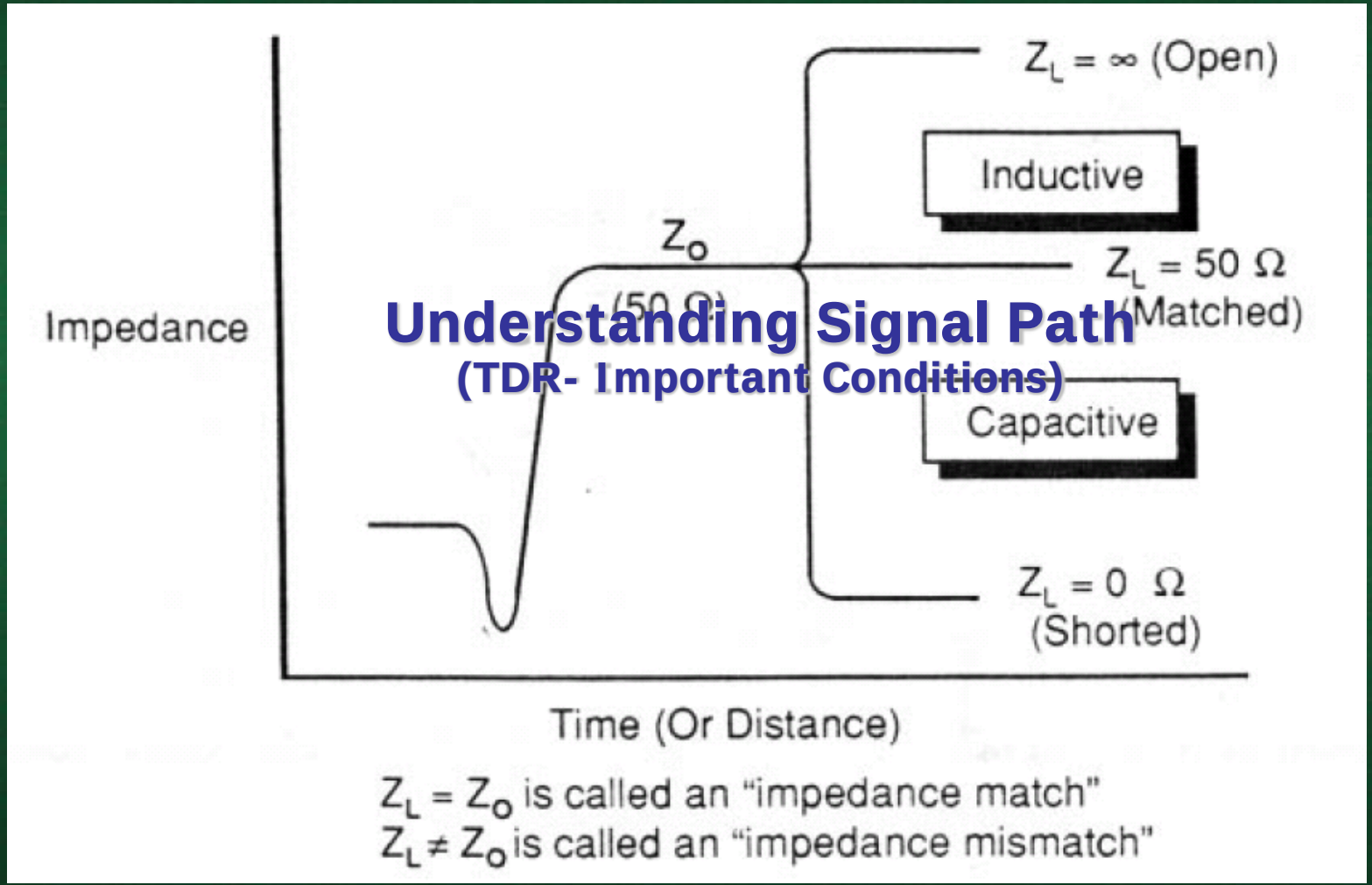
What is happening at signal critical phase.

Extending GND shield on critical signals



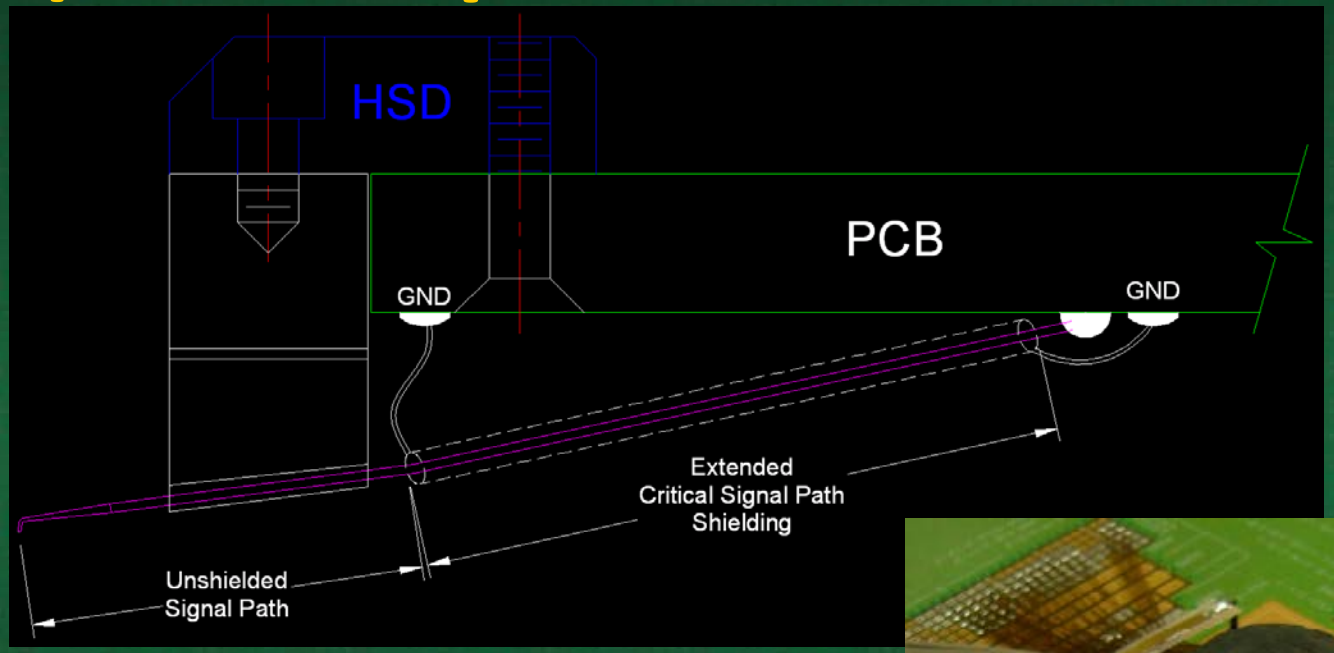
Schematic

Understanding Signal Path (TDR- Important Conditions)

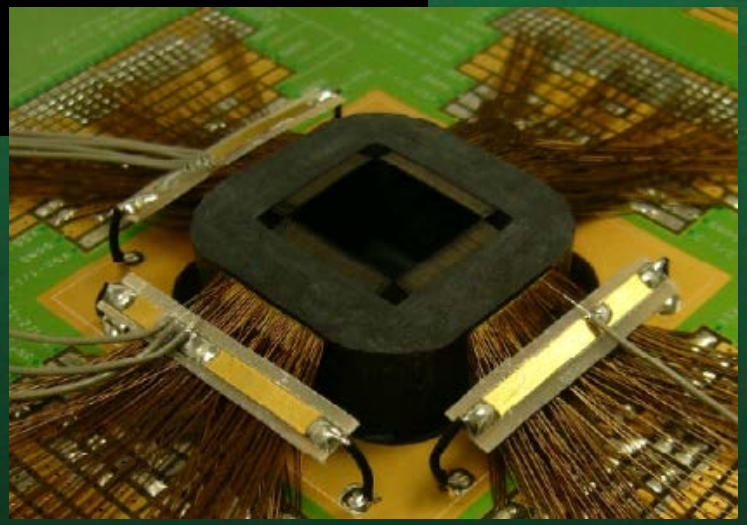


Understanding Signal Path (TDR- Important Conditions)

Design



Extending GND shield on Aggressor or Victim signal path lines.



Actual

Yield Summary Comparison

Probe card from Design A specially designed for high speed testing shows better performance:

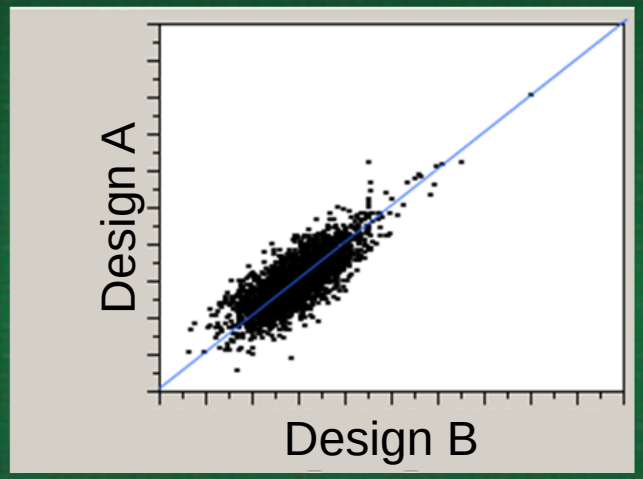
- ✓ Better Mbist High Speed test by 5-8%
- ✓ Better Core Speed test by 8-20%

WF	Split			F Yield Loss		Pass	
	P/C vendor	Cleaning frequency	Cleaning OD	MBIST_Low_Speed	MBIST_High_Speed	Bin1_1.5Ghz	Bin1_1.4Ghz
V	Design B	5 times	40um	3.0	5.6	74.1	8.8
V	Design A	5 times	40um	3.0	0.5	86.5	1.0
W	Design B	5 times	40um	5.7	3.3	73.6	6.9
W	Design A	5 times	40um	5.6	0.3	82.0	1.5
X	Design B	5 times	40um	5.0	7.4	69.5	10.5
X	Design A	5 times	40um	5.0	0.4	85.2	1.2
Y	Design B	5 times	40um	3.1	4.2	78.3	5.5
Y	Design A	5 times	40um	3.1	0.4	84.7	2.2
Z	Design B	5 times	40um	7.9	9.5	45.2	24.9
Z	Design A	5 times	40um	8.0	0.7	72.9	4.3

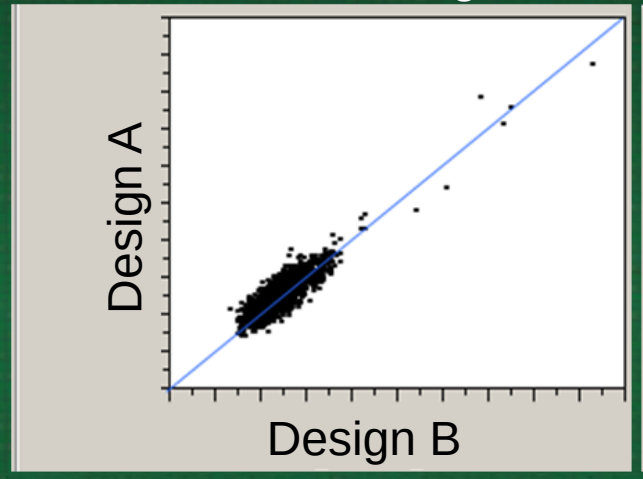
Probe Cards Characterization and Comparison

- ✓ All IDDs are well correlated for both probe cards

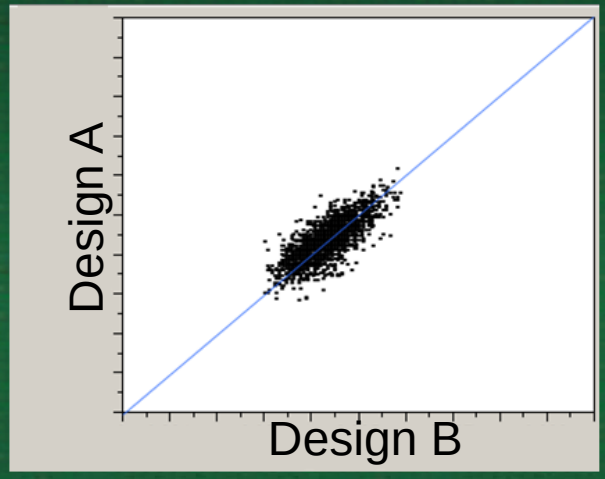
IDD_VDD_CPU



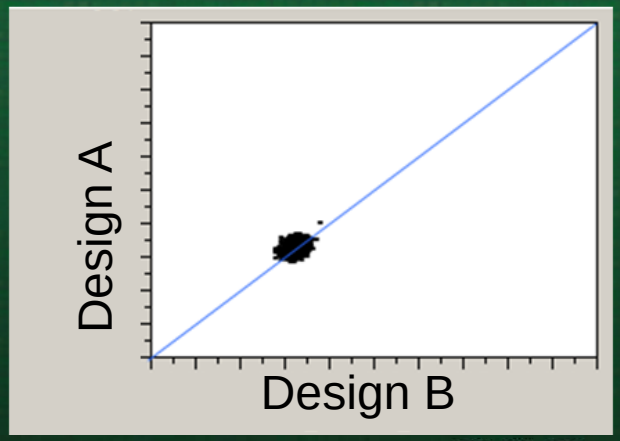
IDD_VDD_Logic



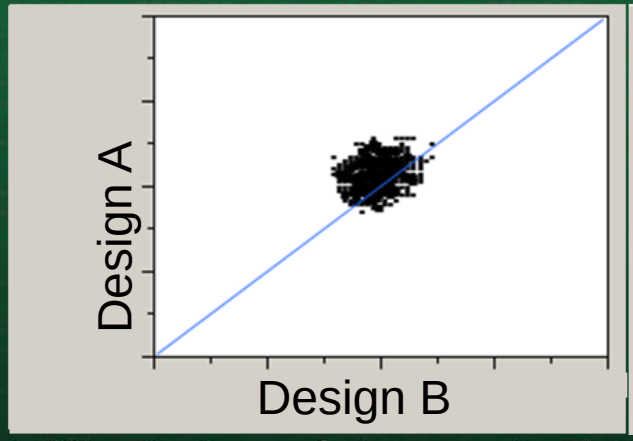
IDD_VDD_1V



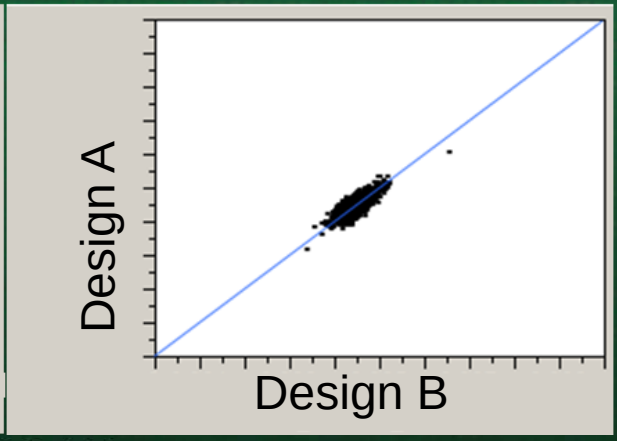
IDD_VCC_3.3V



IDD_VCC_1.8V



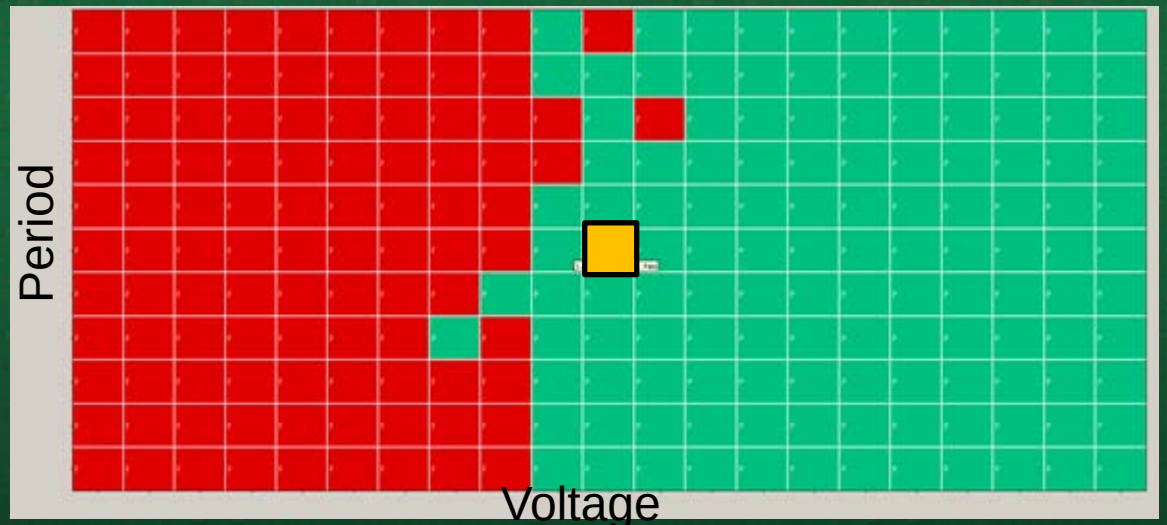
IDD_VCC_DDR



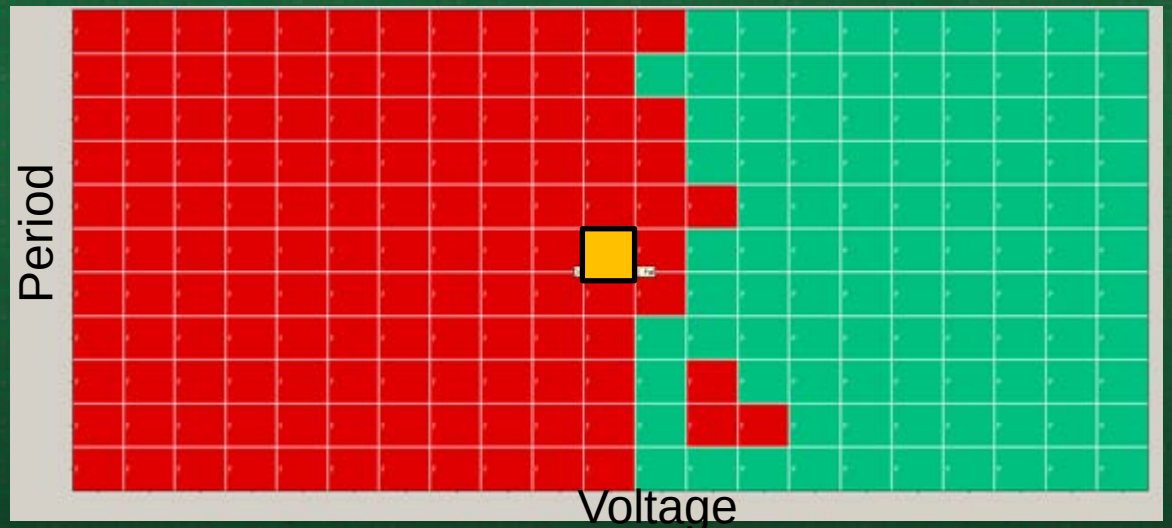
Probe Cards Characterization and Comparison

- Specially designed Probe card from Feinmetall having lower Vmin by 10mV in Core Speed Test

Design A



Design B



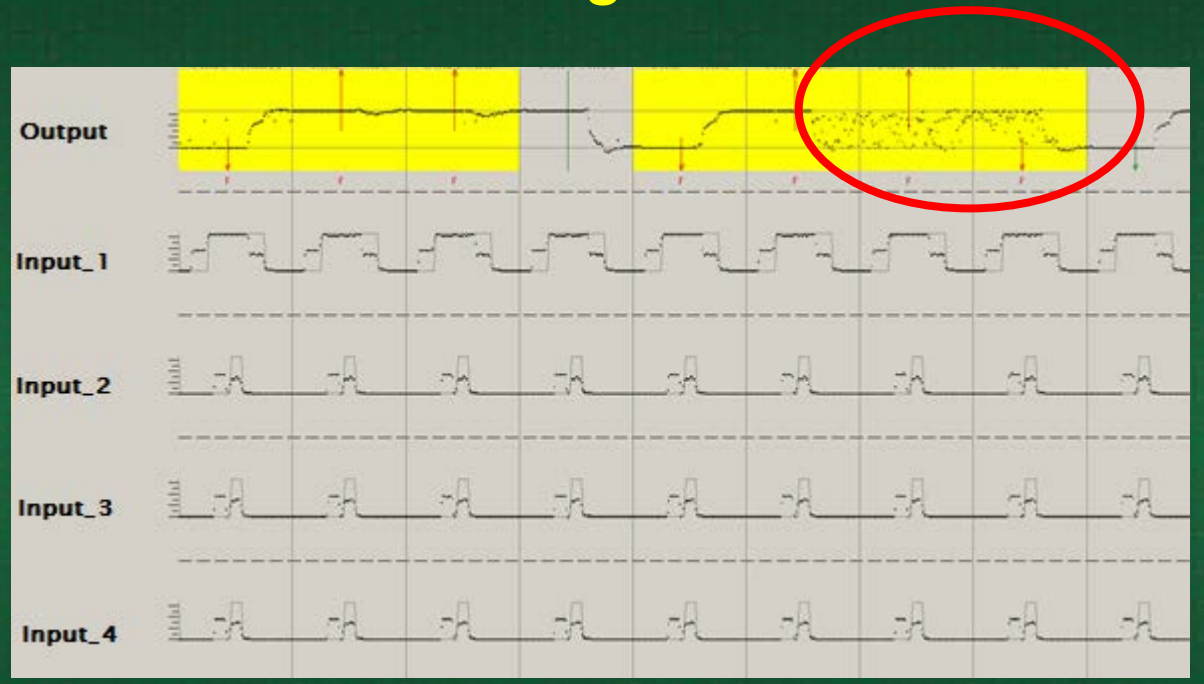
Test point

Probe Cards Characterization and Comparison

Design A

- ✓ Smooth and clean output

Design B



- Crosstalk noises
- Causes unstable output

Conclusion

- This presentation summarized our works to achieve high performance probe card for high speed testing
- Special designed probe card with better fan-out and shielding of critical pins out perform ordinary probe card in high speed testing
- Lower Vmin and better noise isolation achieved

Thank You