SW Test Workshop
Semiconductor Wafer Test Workshop

2017

Advanced Vertical Technologies for Low Damage Probing of Bumps, Pillars, and Pads

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June 4-7, 2017

Agenda

- Background
- MJC MEMS Spring Probe (MSP) for Solder Bumps, Cu Pillars, and Pads
- Qualification of MJC MSP Probe on Cu Pillar Devices at End User
  - End User Objectives
  - Qualification Test Plan
  - Results Summary
- High Volume Manufacturing Validation
- Summary / Conclusions

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Texas Test Corporation (TTC)

WHO WE ARE

Team of former Texas Instruments Engineers.

WHAT WE OFFER

The full range of product and test engineering services.

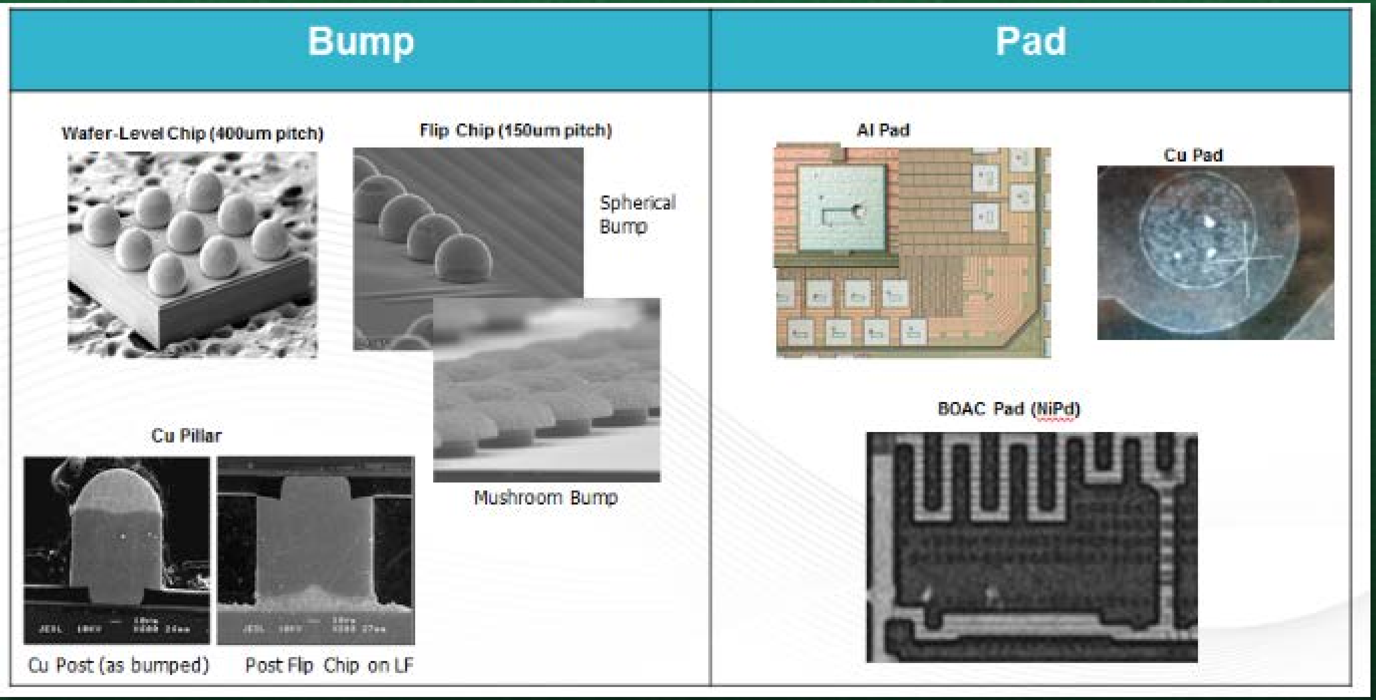
LOCATION

Headquarters: Dallas, Texas, U.S.A.
Product and Test Engineering: Sophia Antipolis, France
Manufacturing Operations: Hsinchu, Taiwan and Shanghai, China

TTC
Texas Test Corporation

Next Gen Requirements Create Probe Challenges

- **Bumped devices are moving from 150um pitches to 80um (and smaller) with high numbers of smaller bumps**
  - Bump pitch range from 130 to 100um today ⇨ moving into 80um (or less)
  - Bump diameters shrinking from 70um ⇨ sub-30um for certain structures
  - Reducing Cost of SoC Test is driven by large arrays for x256 multi-sites and pin-counts as high as 40,000 probes
- **Pitch reductions and minimum allowable damage for assembly and die stacks**
  - Mobile Devices ⇨ 80um
  - Automotive Devices ⇨ 65um
  - HBM Memory Devices ⇨ 50um
  - Wide I/O and Wide I/O 2 Devices ⇨ 40um
- **Electrical performance**
  - Low and stable CRES for functional test
  - Increased CCC for steady state and pulsed current
  - High speed performance testing
- **Tri-temperature characterization**
  - Demanding automotive standards
  - Multiprobe ⇨ -55C to 25C to 200C
  - Same test cell and probecard



Source: B. Mair SW-Test Archives

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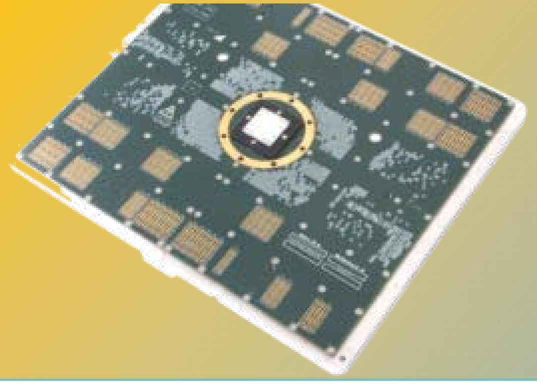
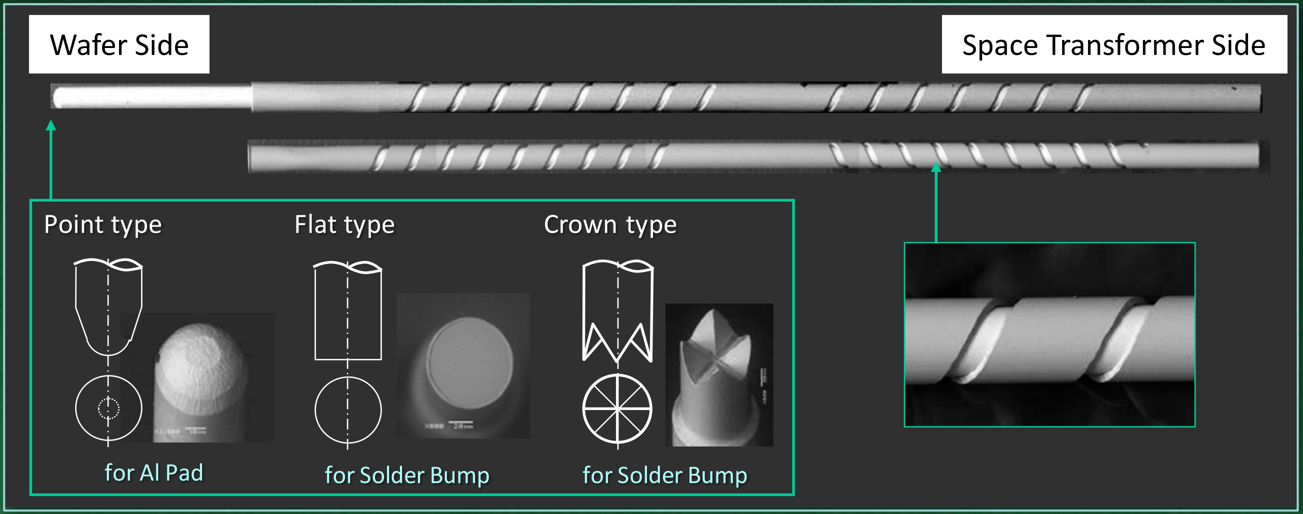
MJC MEMS Spring Probe for Solder Bumps, Cu Pillars, and Pads

MJC MEMS-SP (MSP)



Flip Chip Type Device
Multi-die test of devices with
Area Array (Bump / Cu Pillar)



MJC MEMS Spring Probe (MSP) Technology

- MEMS fabricated, non-oxidizing barrel & spring
- Proprietary fabrication process for probe architecture
- Spring force is controlled and defined by barrel geometries
- Preload at space transformer for stable contact
- On-site needle replacement capability

MJC MEMS Spring Probe for Solder Bumps, Cu Pillars, and Pads

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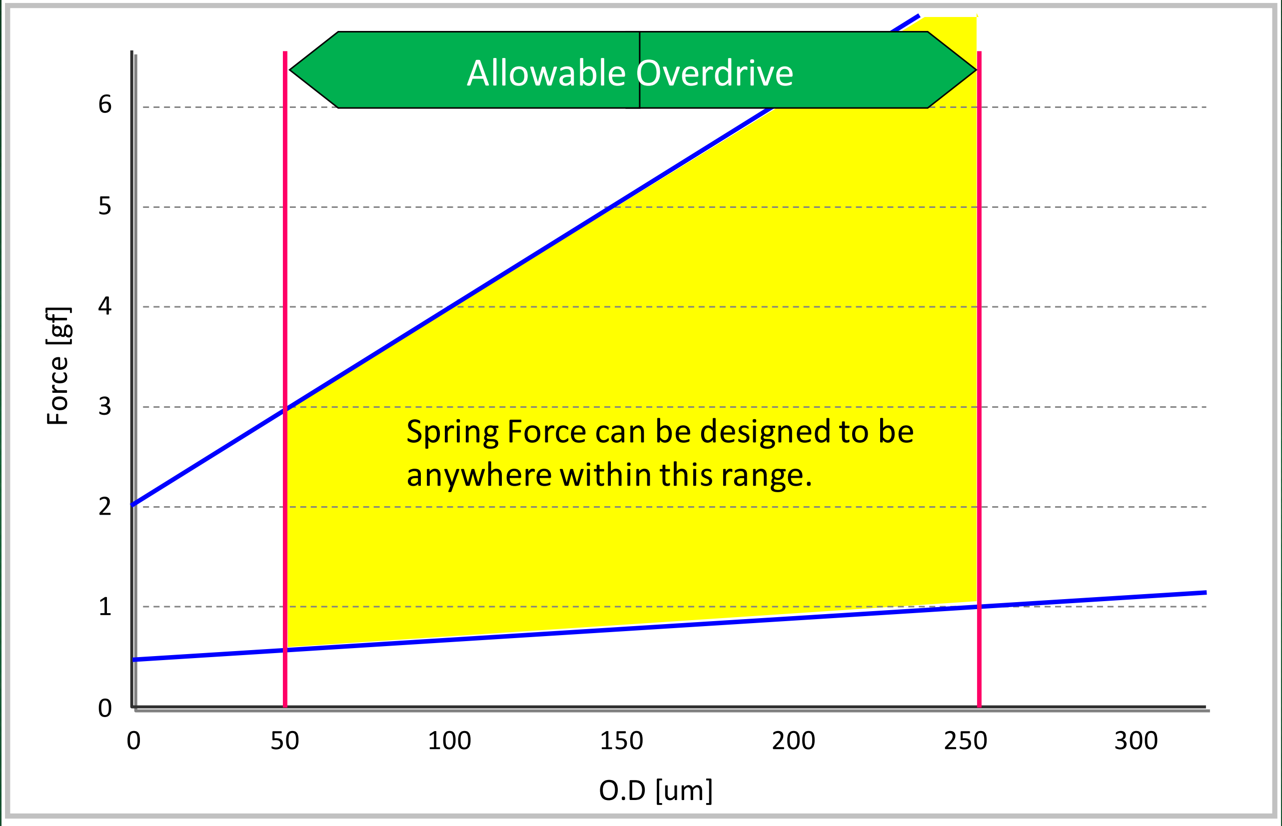

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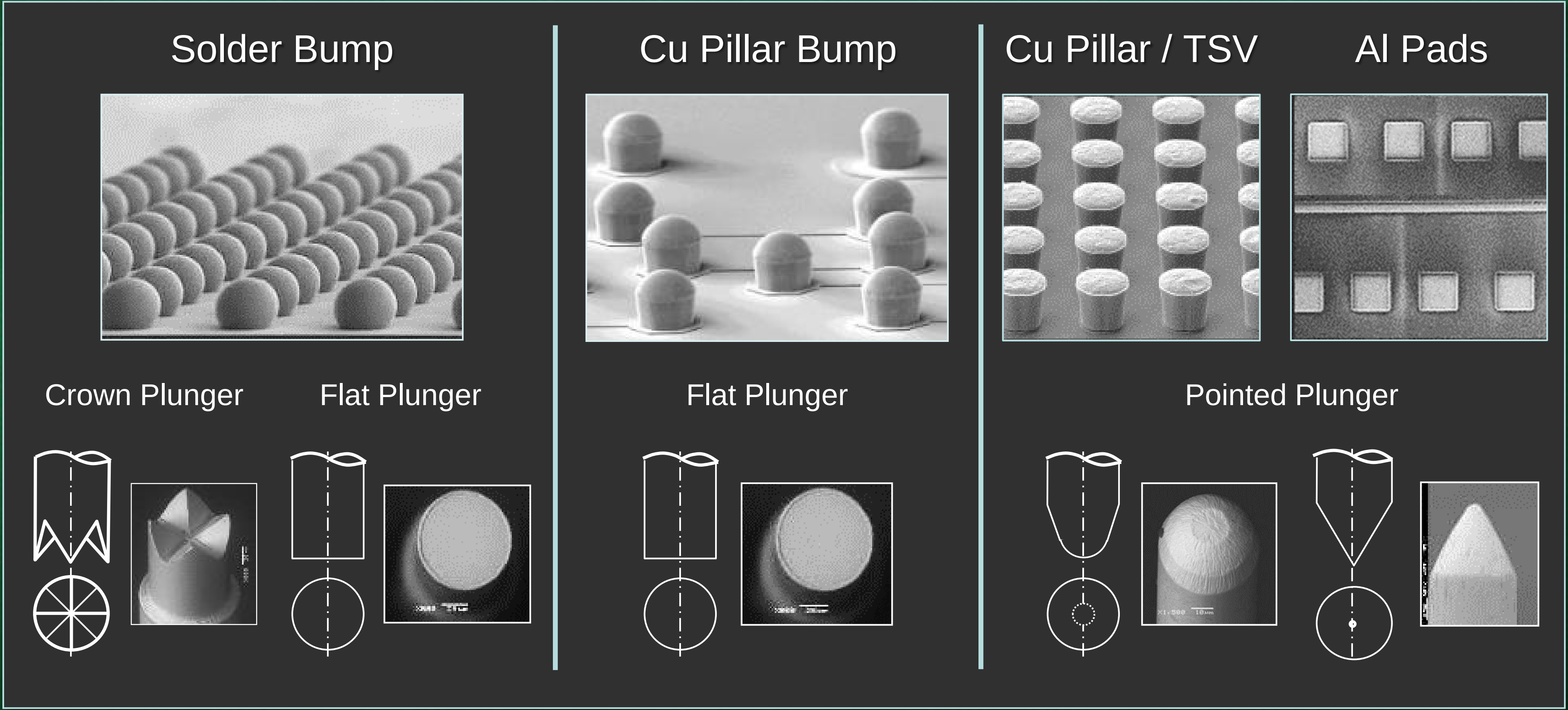
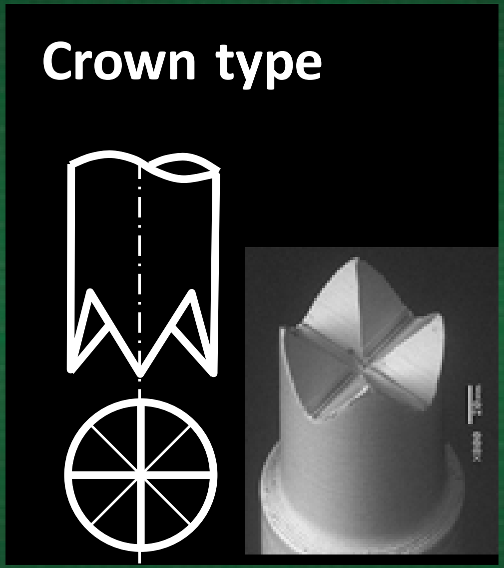
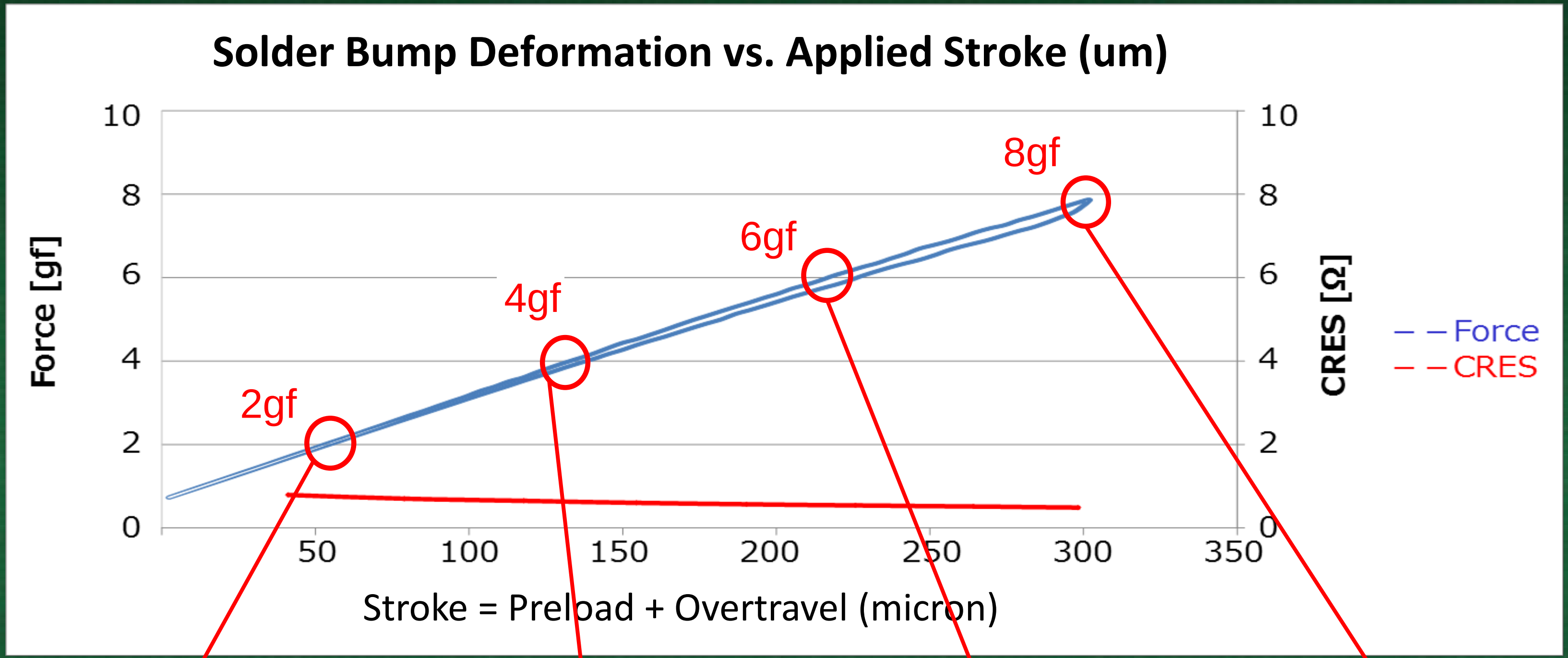
MJC MEMS Spring Probe Tip Plunger Geometry

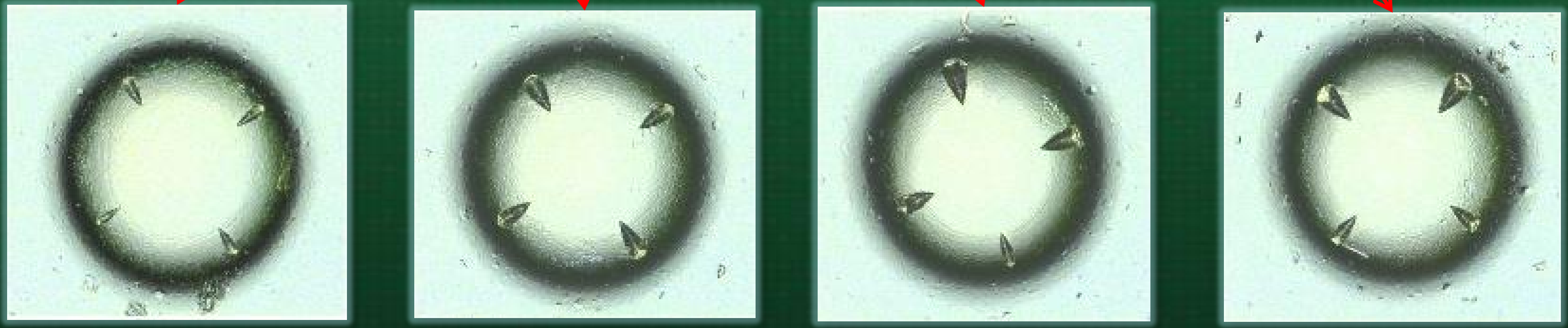
- **Plunger material and tip shape can be selected depending on the application.**



Solder Bump Probe with MJC MSP Crown Tip Plunger

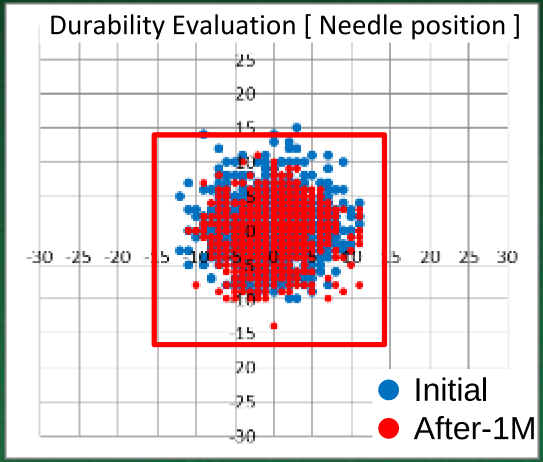


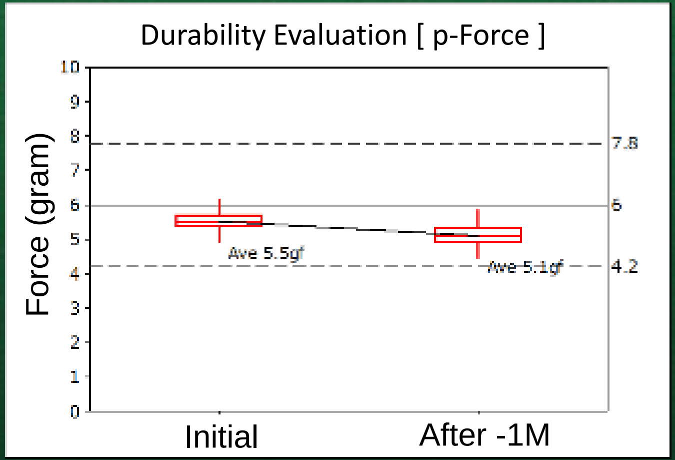


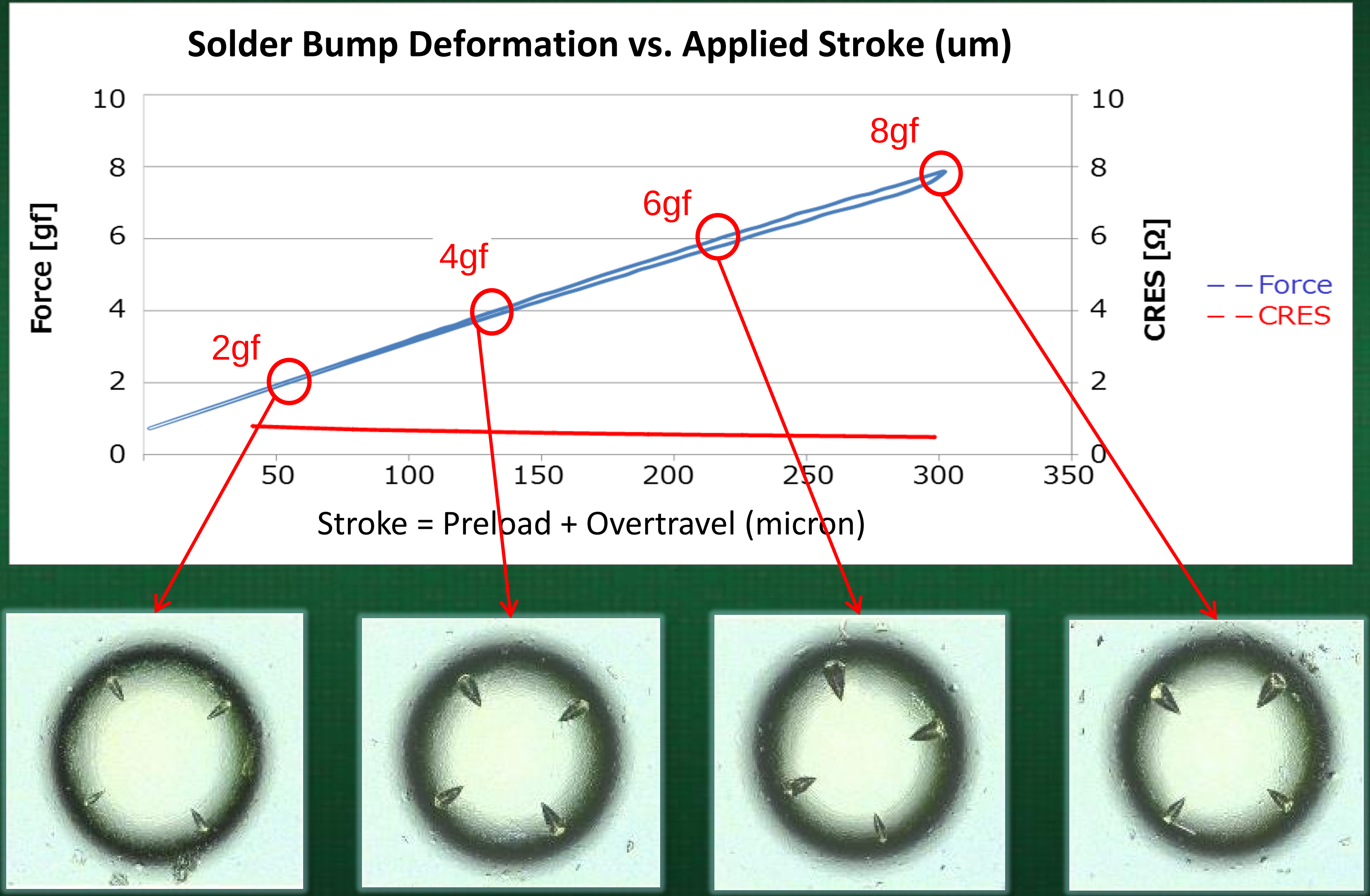


Solder Bump Probe with MJC MSP Crown Tip Plunger

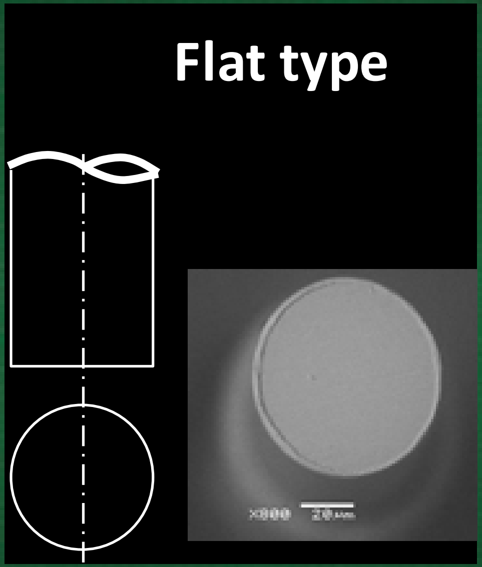
Solder Bump（6gf Probe）

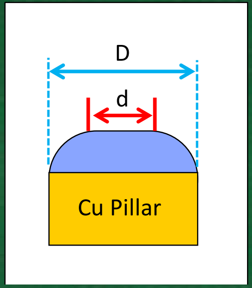


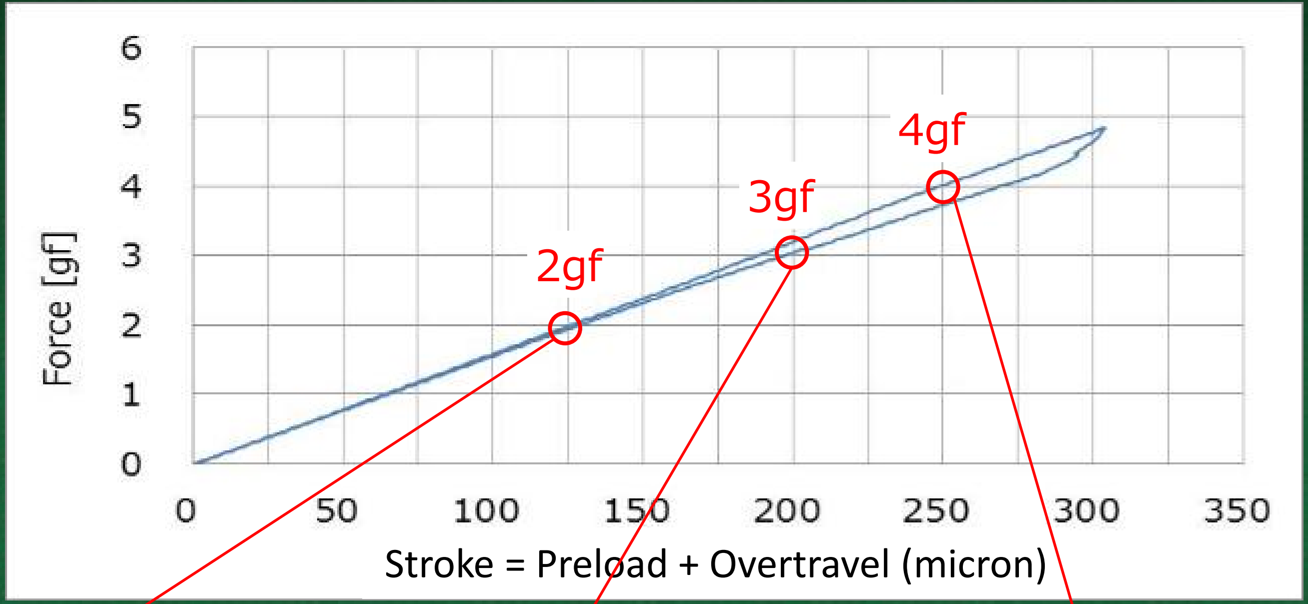


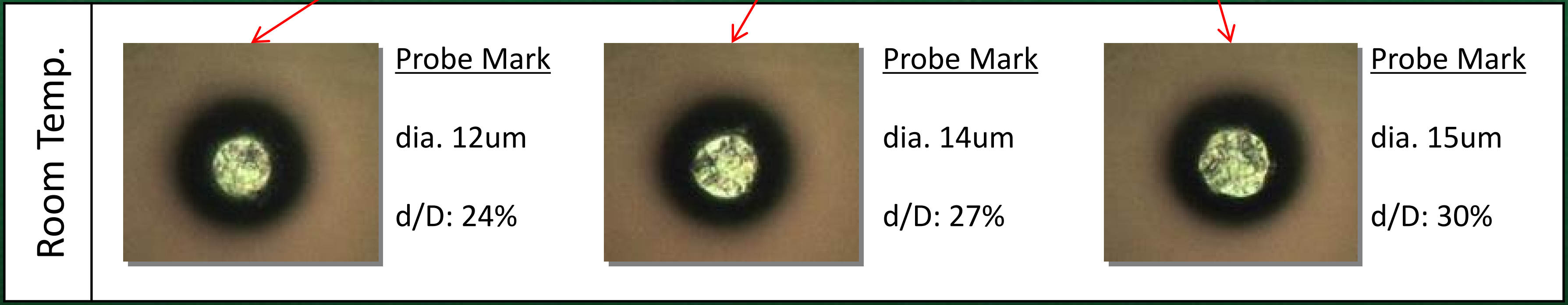


Cu-Pillar Bump Probe (RT) with MJC MSP Flat Tip Plunger





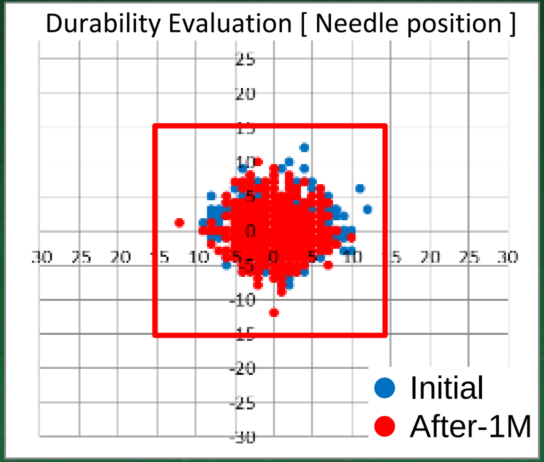


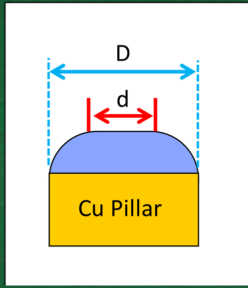


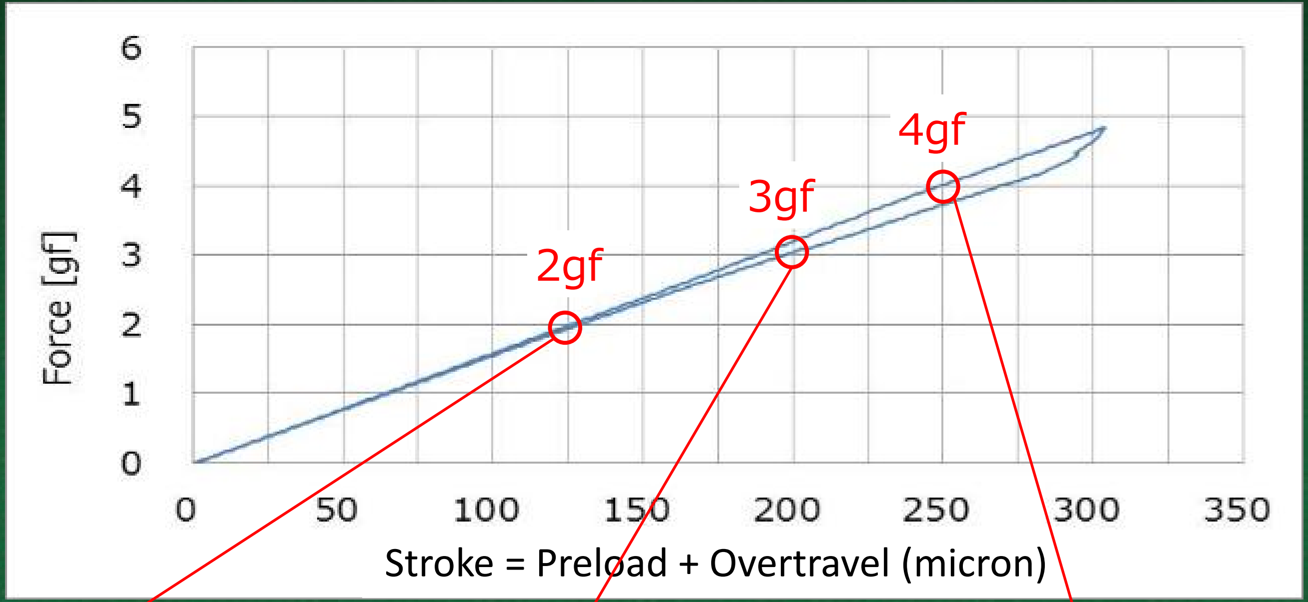
Dia_initial = 50um diameter Cu Pillar Bumps with Sn/Ag lead-free solder cap

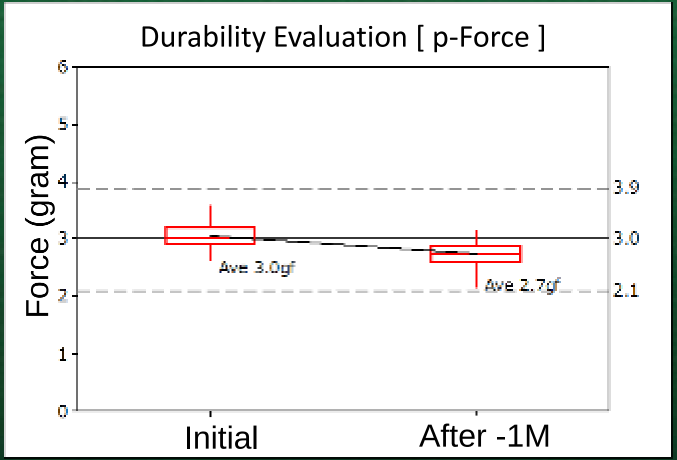
Cu-Pillar Bump Probe (RT) with MJC MSP Flat Tip Plunger

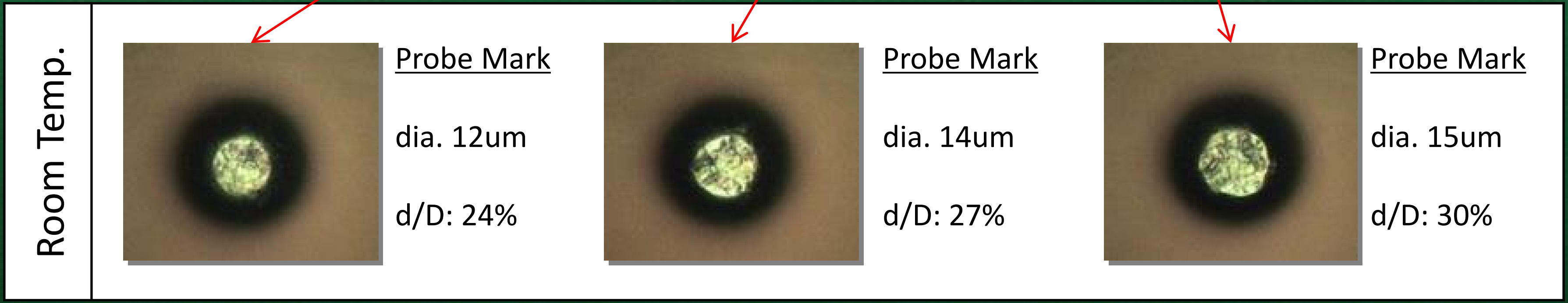
Cu Pillar Bump（3gf Probe）





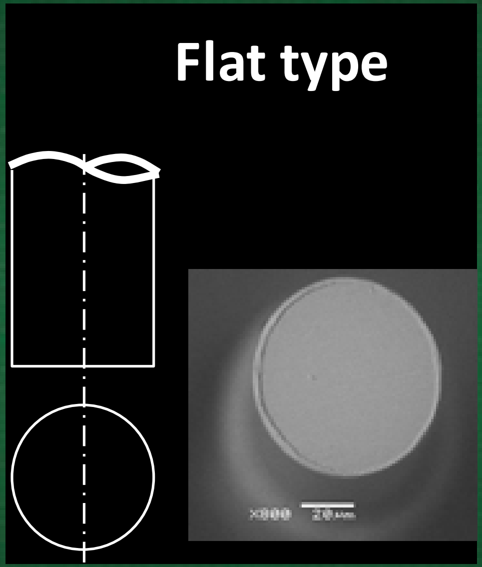


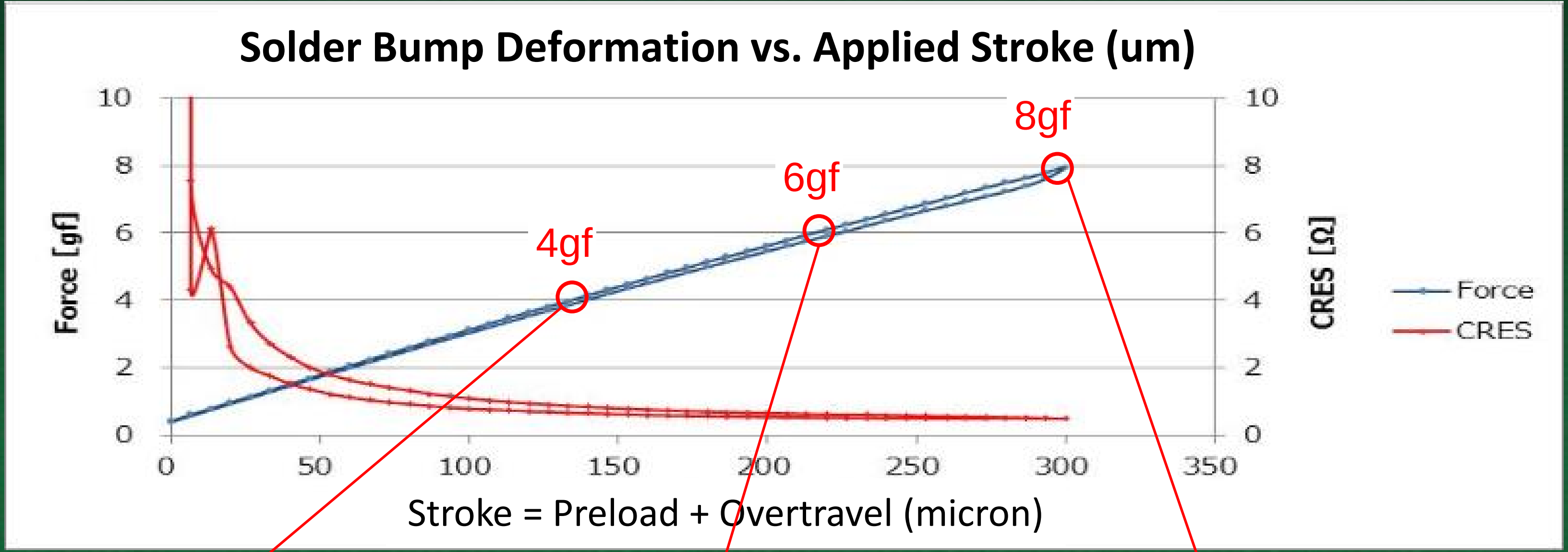


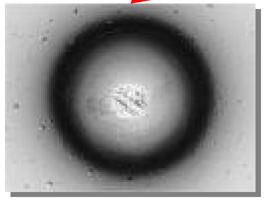
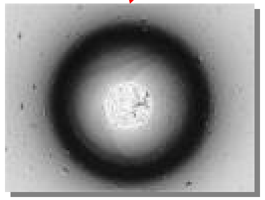
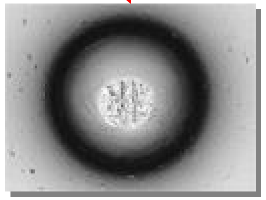
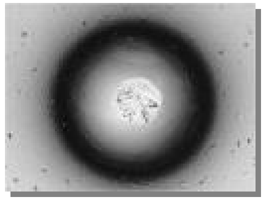
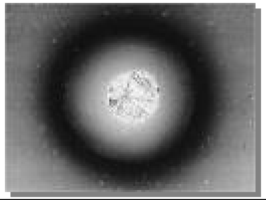
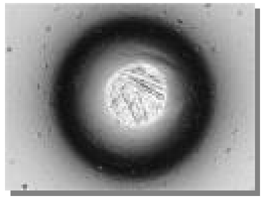


Dia_initial = 50um diameter Cu Pillar Bumps with Sn/Ag lead-free solder cap

Cu-Pillar Bump Probe (HT) with MJC MSP Flat Tip Plunger



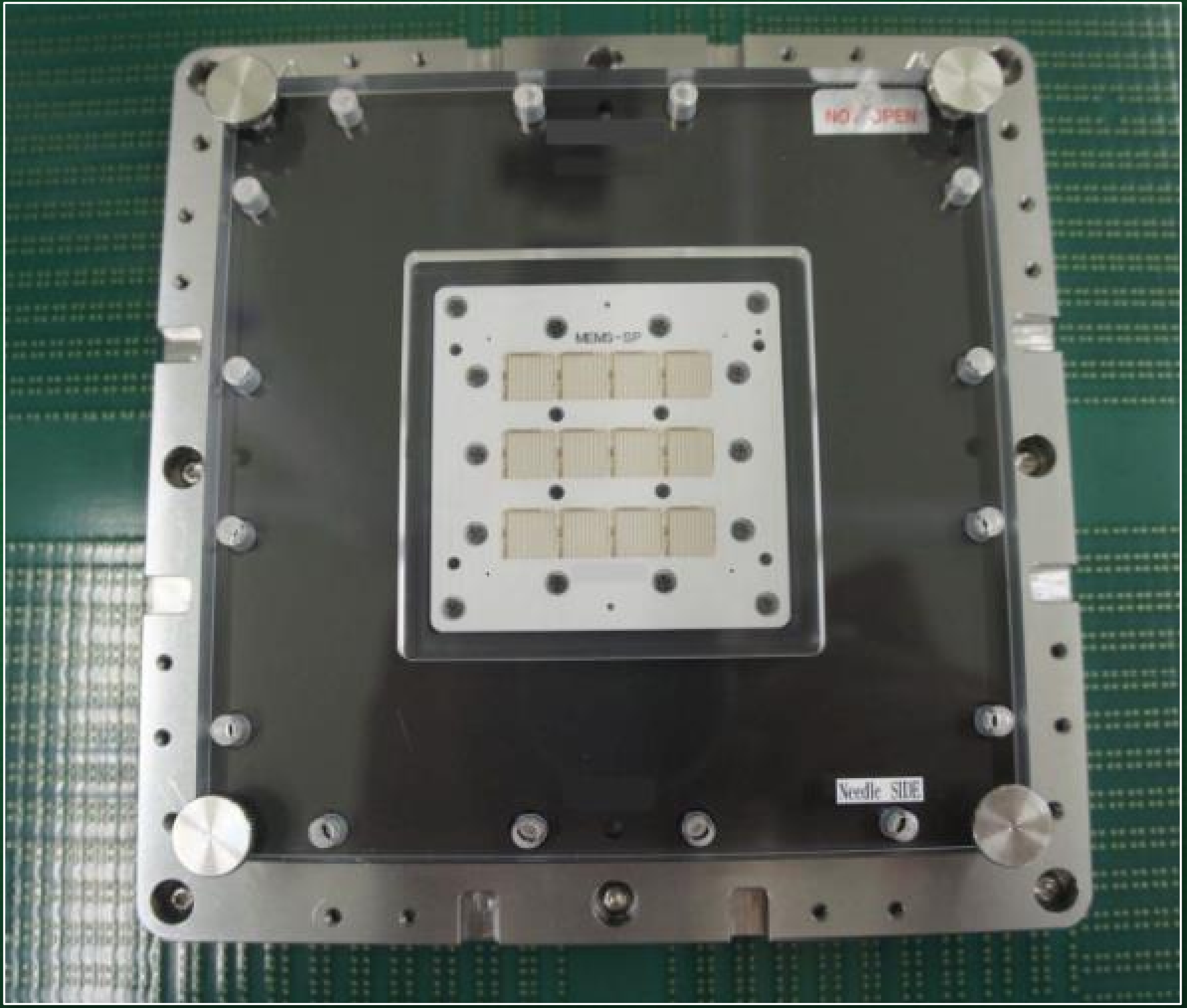


RT		Probe Mark Dia.18um d/D:20% a/A: 4%		Probe Mark Dia.23um d/D:26% a/A: 7%		Probe Mark Dia.25um d/D:28% a/A: 8%
HT90C		Probe Mark Dia.19um d/D:22% a/A: 5%		Probe Mark Dia.27um d/D:30% a/A: 9%		Probe Mark Dia.31um d/D:35% a/A:12%

Dia_initial = 90um diameter bumps (lead-free solder alloy, Sn/Ag3/Cu0.5) *SMIC_M705

MJC MEMS SP-Probe … In the Field !

- Multisite cards with > 28K pin counts have been successfully installed.



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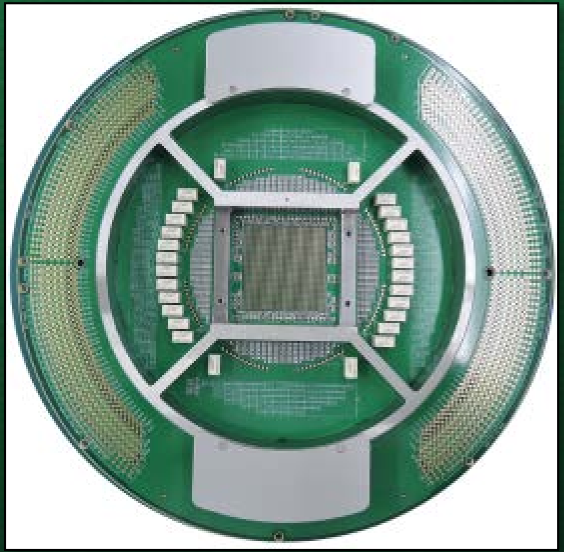
End User Objectives

- **Improve Sort Performance over Cobra Style Vertical Card**
  - Probe force consistency and "tune-ability" for uniform probe marks
  - Low damage on small bumps
  - Probe-to-bump alignment (PTBA)
  - Stable electrical performance
  - High 1st Pass Yields w/ reduced recovery test
- **Reduced Cost of Ownership over Cobra Style Vertical Card**
  - Reduced maintain and increased lifetime performance (MTBR and End of Life)
  - Minimize test cell down due to contact related
  - Easy repair and simple single pin replacement capabilities

Test Cell Overview

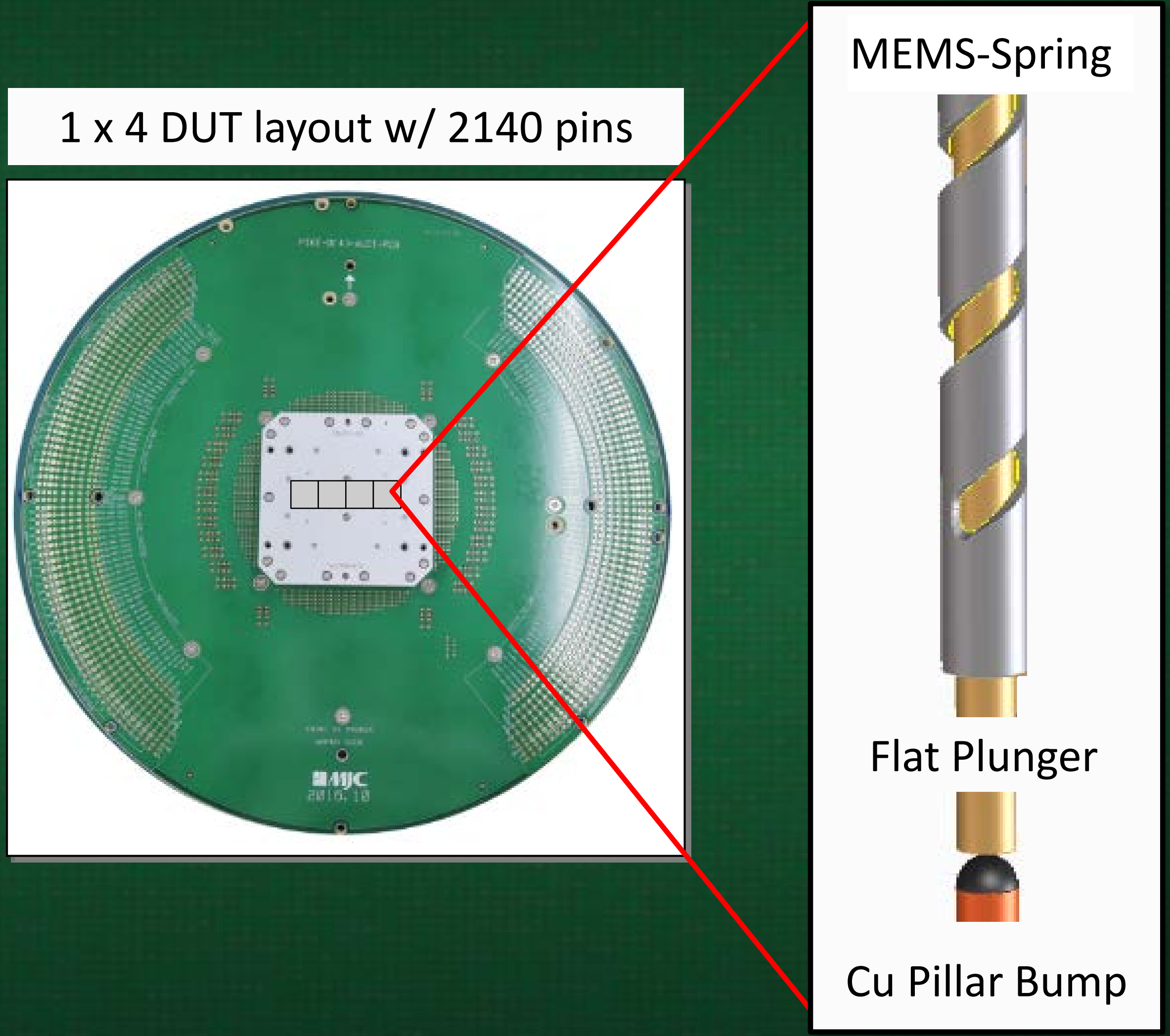
- **Equipment**
  - Tester = VLCT Platform
  - Prober = Accretech 300mm Prober
  - Probe Type = MEMS SP w/ flat tip plunger
  - Probe Card Test Vehicle = 1 x 4 DUT w/ 2140 pins
- **Test Conditions**
  - Test temp = 30C
  - OD = Variable as defined during testing
- **Cleaning conditions for all testing**
  - Octagonal movement
  - Cleaning Overtravel = 100um
  - Cleaning Frequency = 1 clean per 200 wafer TD

Wegleitner, SWTW 2005



Probe Card Test Vehicle and MSP Probe

Property	Specification
Target Material	Cu Pillar Bump
Minimum pitch	95um pitch with full array
Tip shape	Flat Plunger
Contact force	3gf / OD150um
C.C.C. (ISMI 20% force drop)	800 mA
Alignment	±15um
Planarity	Less than 50um
Temperature	-40C to 90C

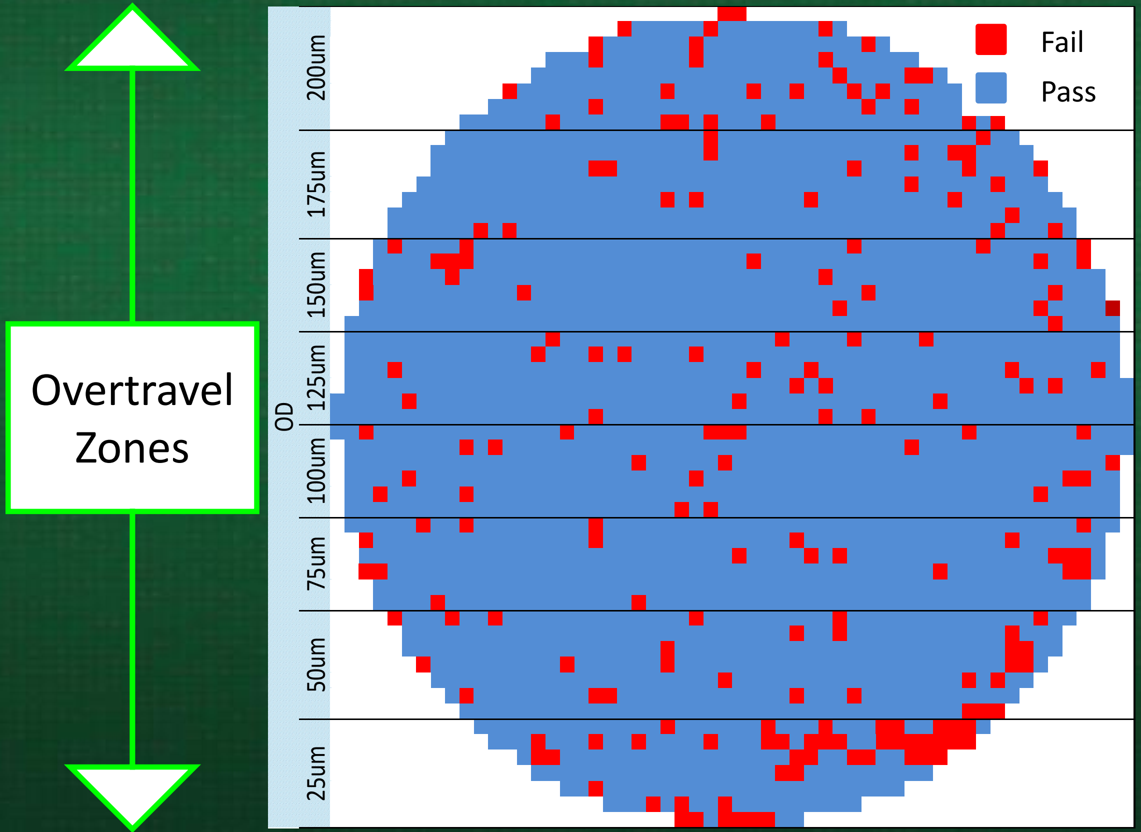


Qualification Test Plan

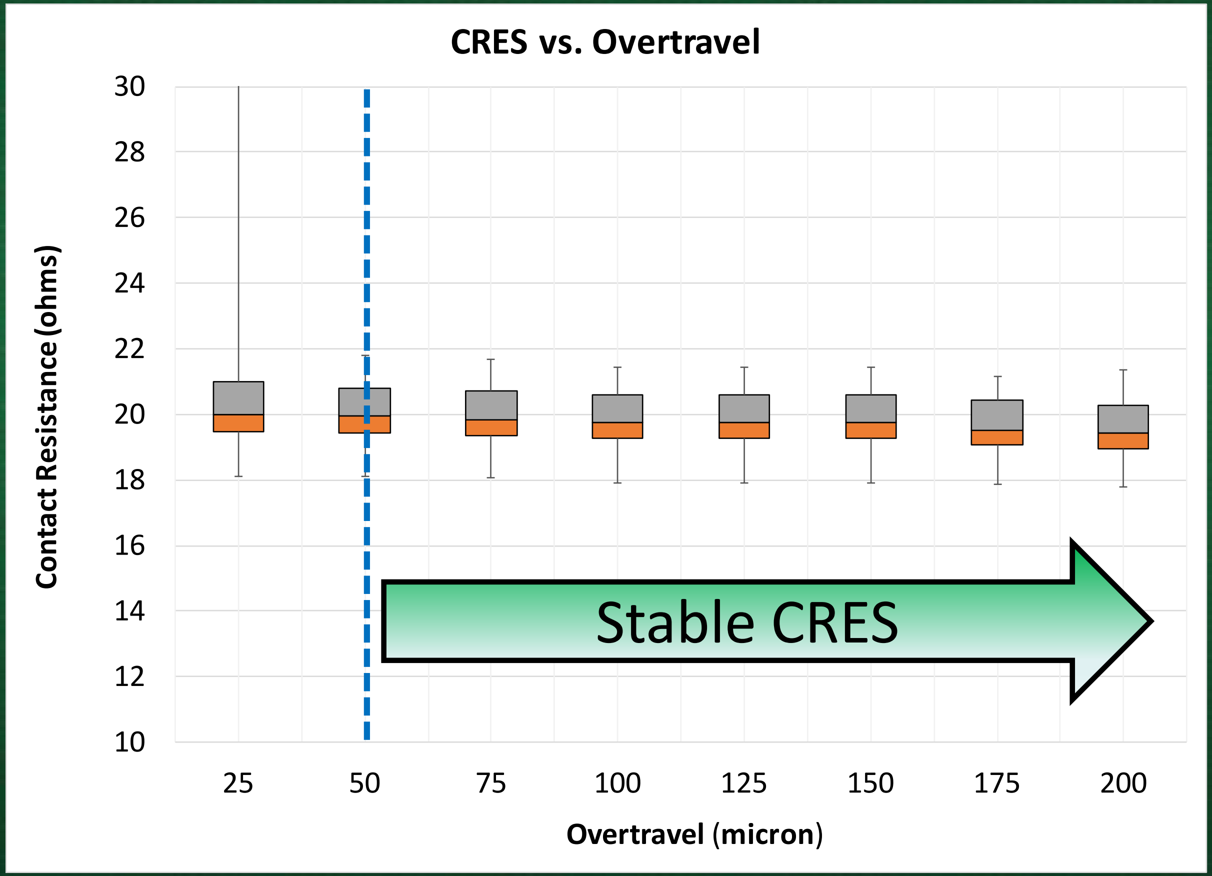
- **Contact Resistance (CRES) Assessment**
  - Determine OD to attain stable CRES
  - CRES vs. Repeated Touchdowns
- **Damage Assessment**
  - Bump Damage vs. Overdrive
  - Bump Damage vs. Repeated Touchdowns
- **Bin-to-bin Reproducibility**
- **Stable Correlation Wafer Yield Results**
- **CRES Determination and Trending**
  - MJC MSP Probe vs. Cobra Style Vertical

Overtravel to Attain Stable CRES

- **Overtravel Applied to Wafer**
  - Overtravel Range = 25 to 200um
  - Overtravel Increment = 25um
  - Single Touchdown

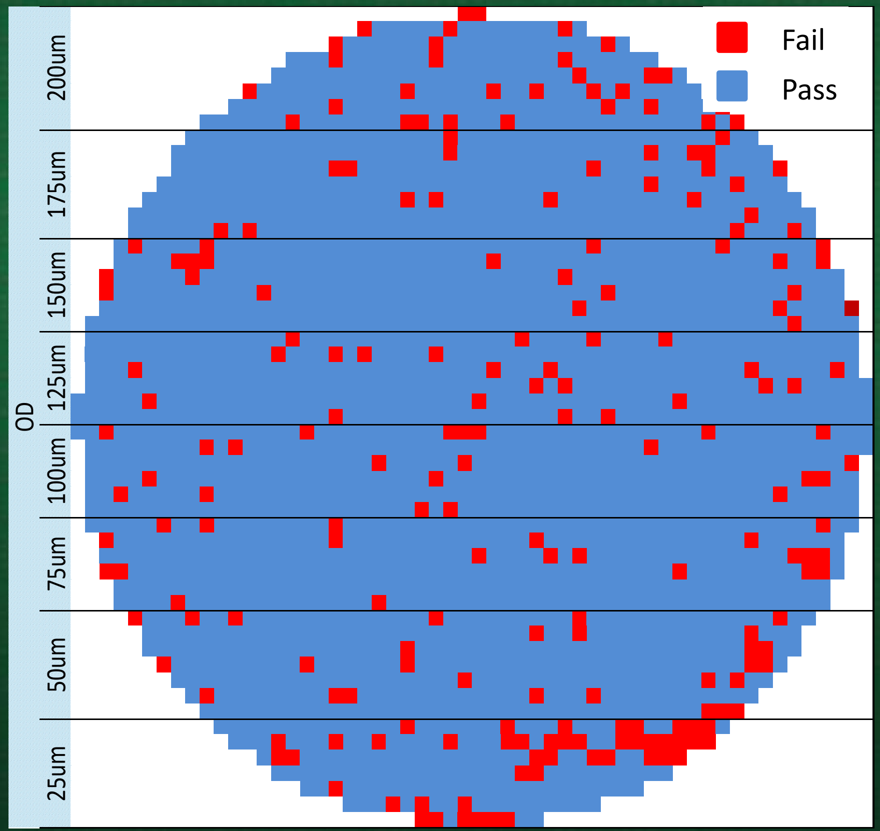


Stable resistance attained @ Overtravel > 50um

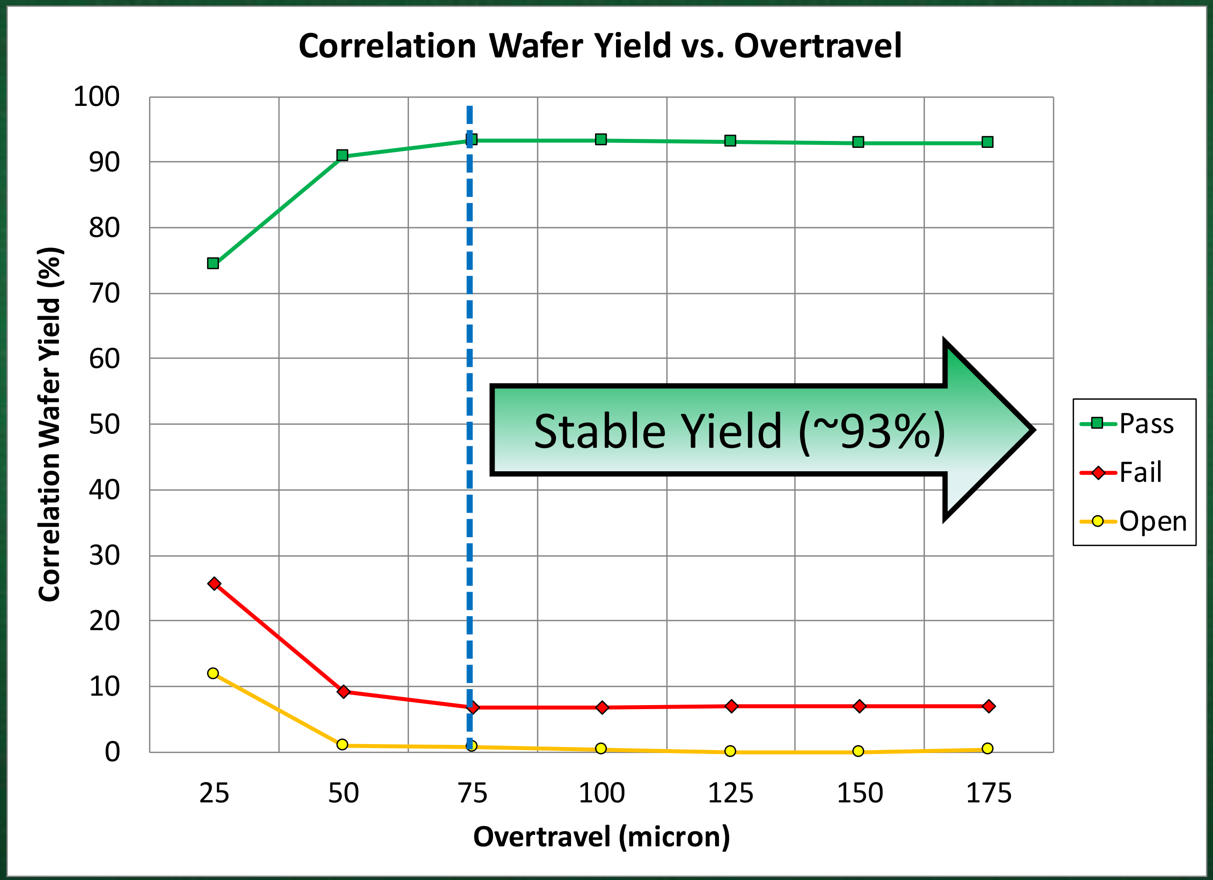


Overtravel to Attain Stable Correlation Yield

- **Overtravel Applied to Wafer**
  - Overtravel Range = 25 to 200um
  - Overtravel Increment = 25um
  - Single Touchdown

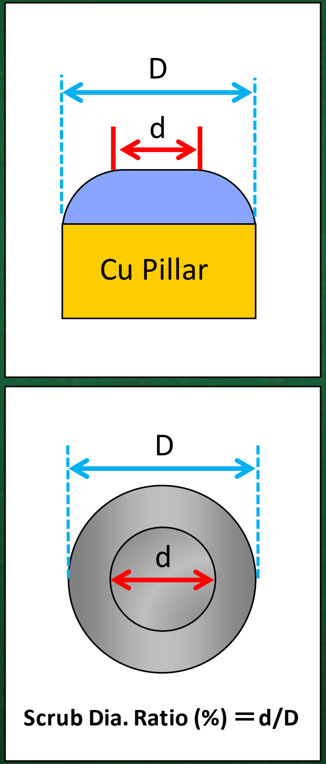


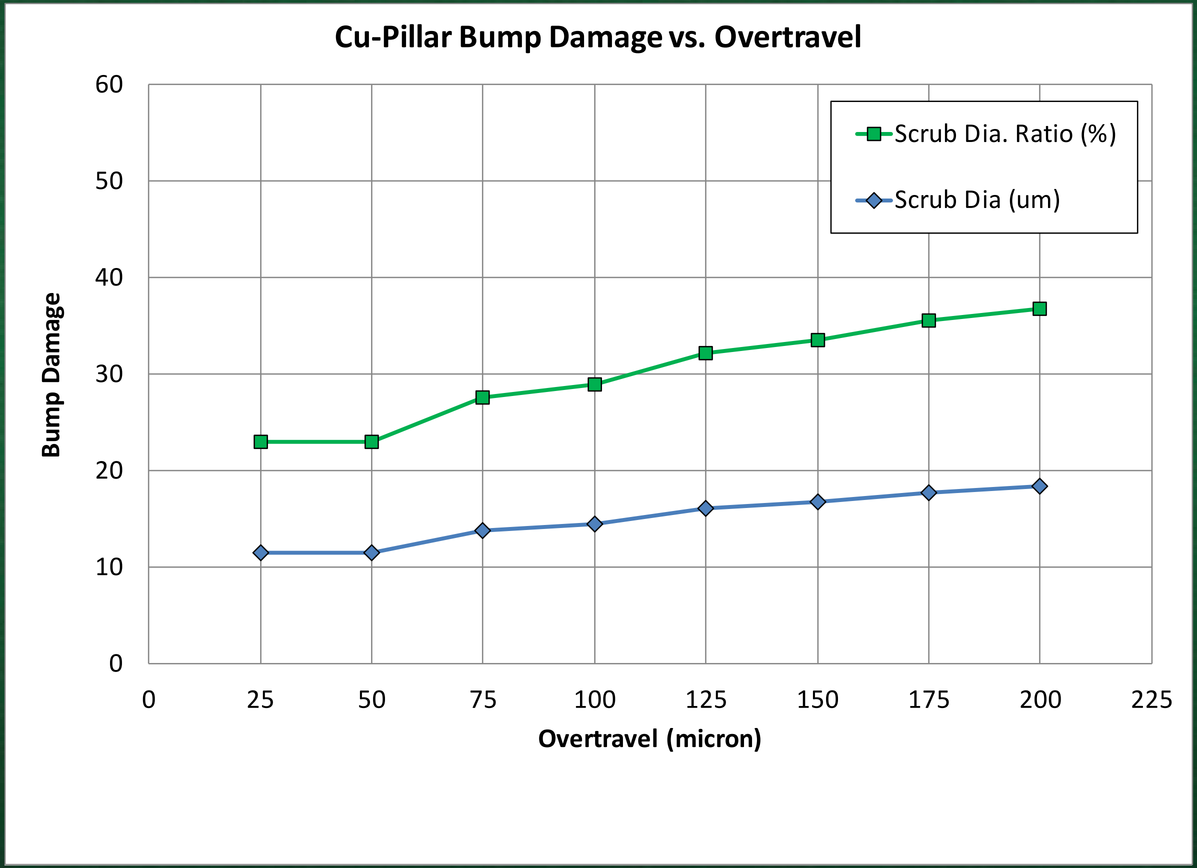
Stable Correlation Wafer Yield @ Overtravel > 75um

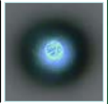
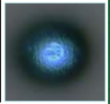
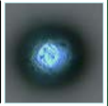
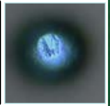
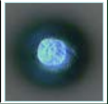


Overtravel vs. Bump Deformation and Damage

- At higher overtravel, the bump are more deformed and tend to higher %-damage.
- At OD = 200um, the %-Damage is significantly less than the specification limit (% Damage < 50%).





OD (micron)	Scrub Diam. (micron)	Scrub Ratio (%)	Scrub Mark
25um	11.5	23.0	
50um	11.5	23.0	
75um	13.8	27.6	
100um	14.5	28.9	
125um	16.1	32.2	
150um	16.8	33.6	
175um	17.8	35.5	
200um	18.4	36.8	

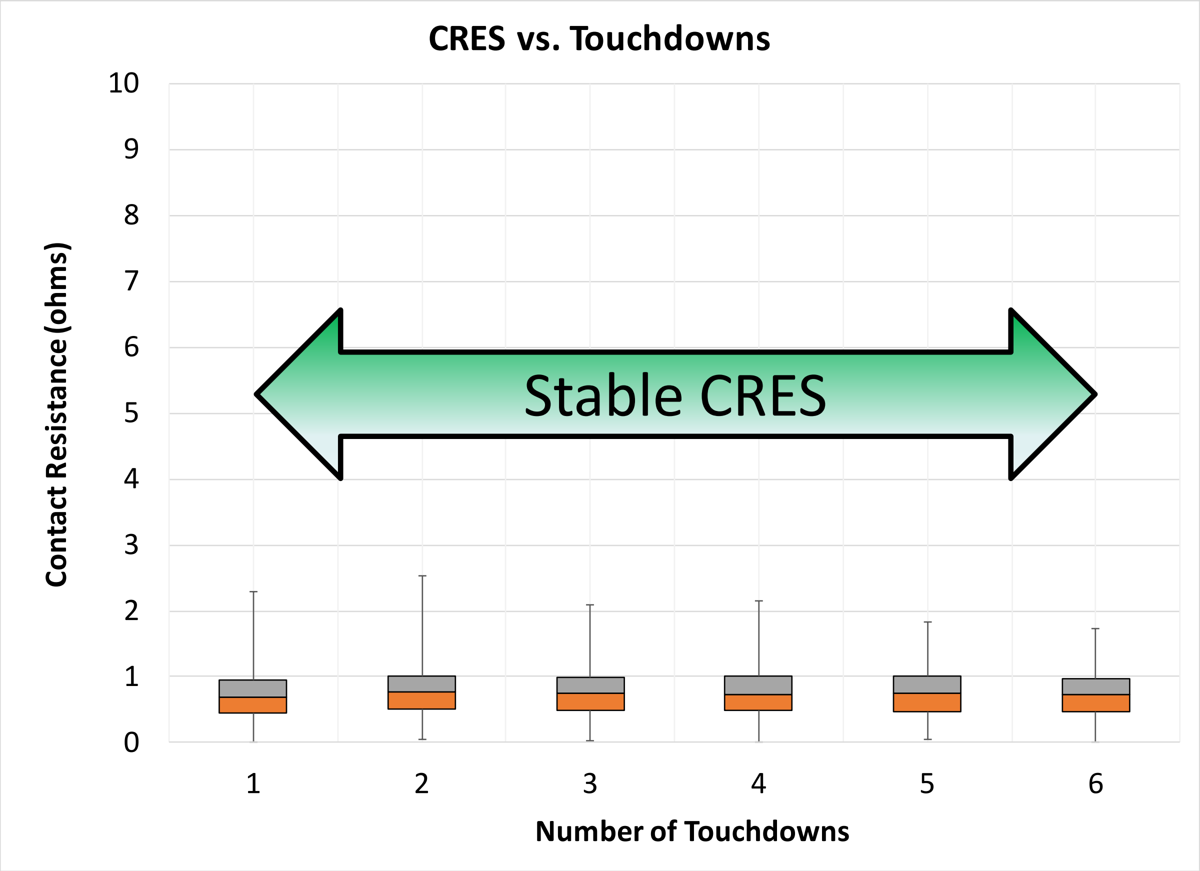
Multi-Touchdowns vs. CRES

- **Touchdowns Applied to Wafer**
  - Overtravel = 150um
  - Number of TDs = 1 to 6
    - Function Test @ 1TD
    - CRES Test @ 2 to 6TD

- **Electrical testing performed across 10-critical pins.**

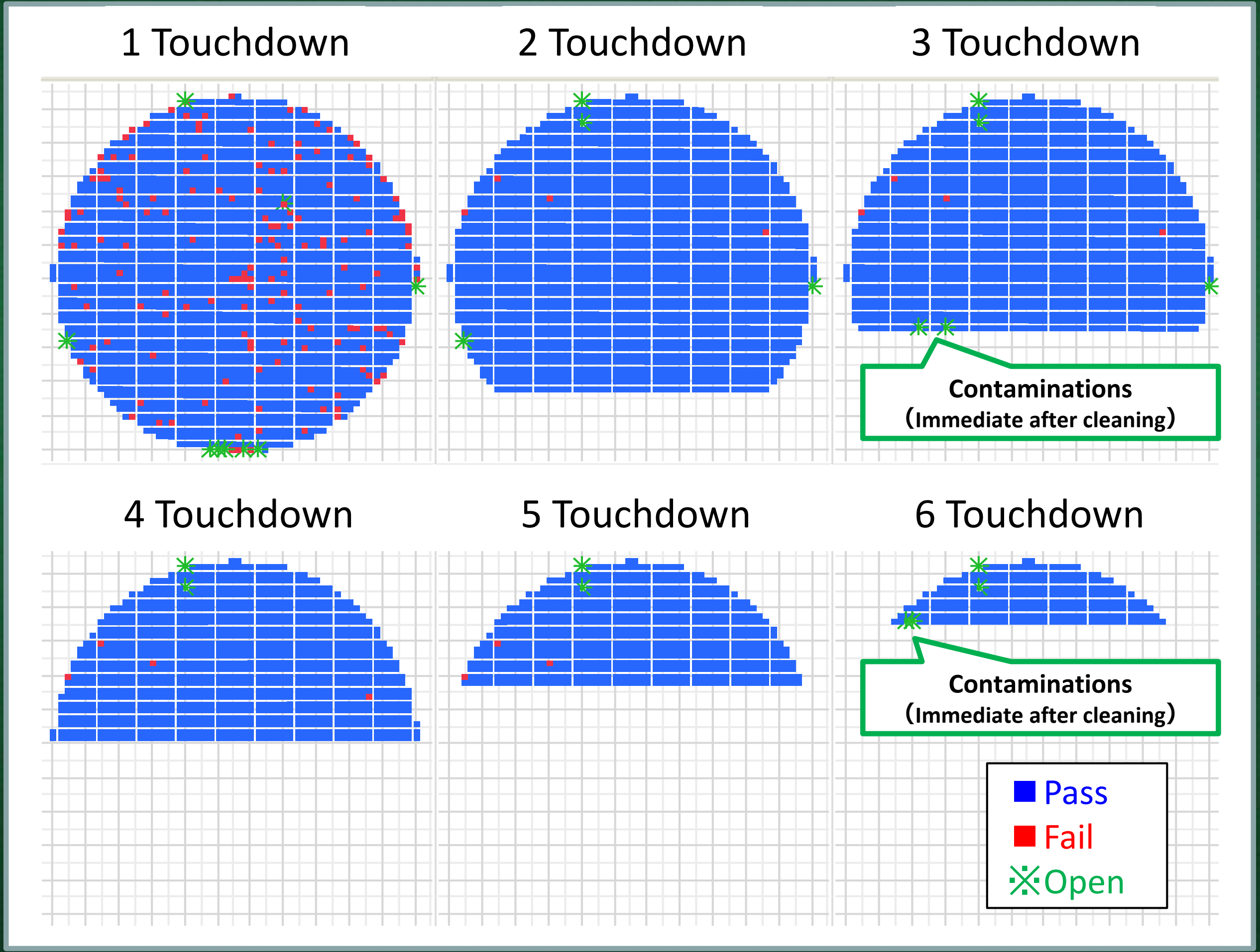
Touchdowns	Electrical Tests Performed
1	2442
2	2013
3	1583
4	1150
5	714
6	281

Stable Contact Resistance @ TD 1 to 6



Multi-Touchdowns vs. Correlation Wafer Yield

- **Touchdowns Applied to Wafer at OD = 150um**
  - Number of Touchdowns = 1 to 6 (Function Test @ 1TD w/ retest check; CRES Test @ 2 to 6TD)

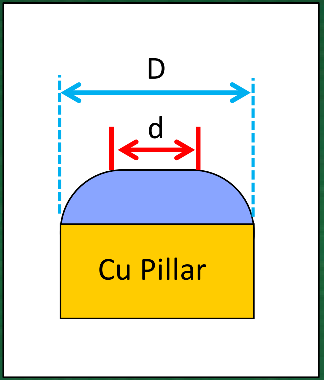


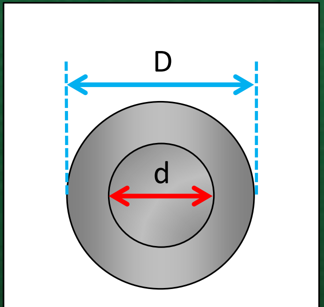
1st Pass Yield	91.5%
1st Pass Fail	8.5%
1st Pass Open	0.7%
Retest Recovery	13 Chip

- 1st Pass Correlation Wafer Yield = 91.5%
- Re-Test Recovery ⇨ 13 chips were recovered
- No further recovery for TD = 2 thru 6
- Pass / Fail / Open of each touchdown sequence were well correlated.

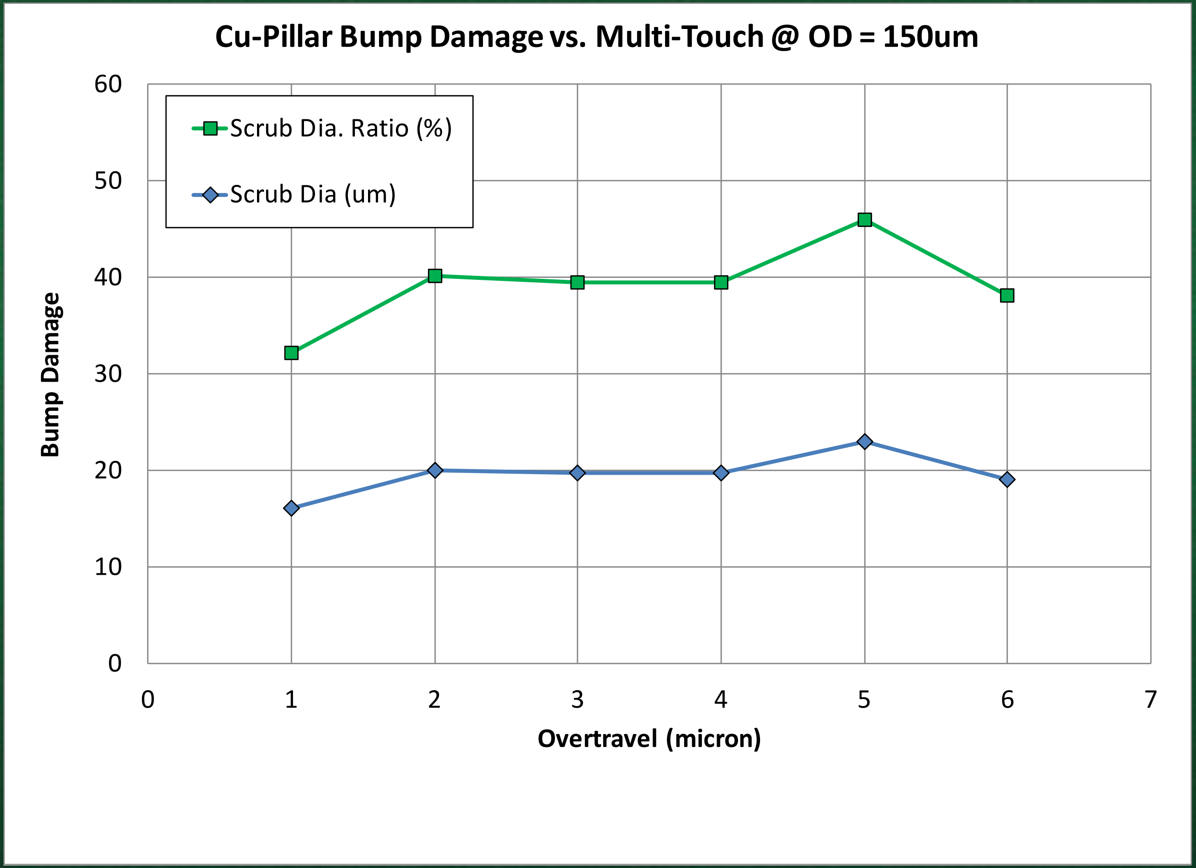
Multi-TD vs. Bump Deformation and Damage

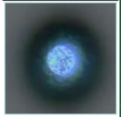
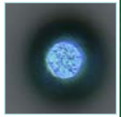
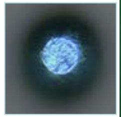
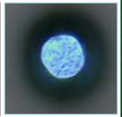
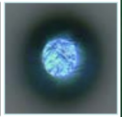
- After multiple touchdowns at OD = 150um, the bump are more deformed and have higher damage.
- After 2 x TDs, the %-Damage is remains constant and less than the specification limit (% Damage < 50%)





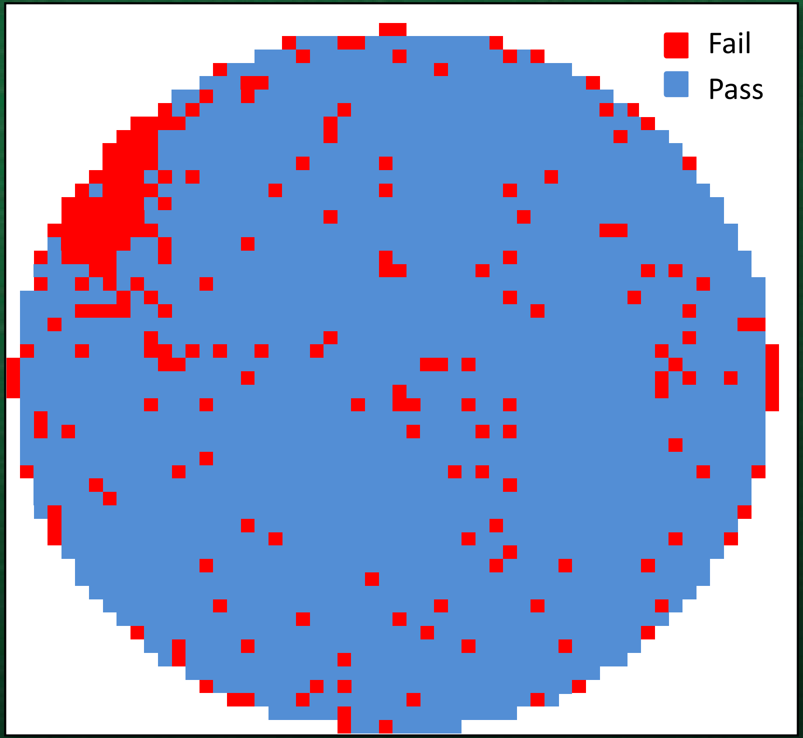
Scrub Dia. Ratio (%) = d/D



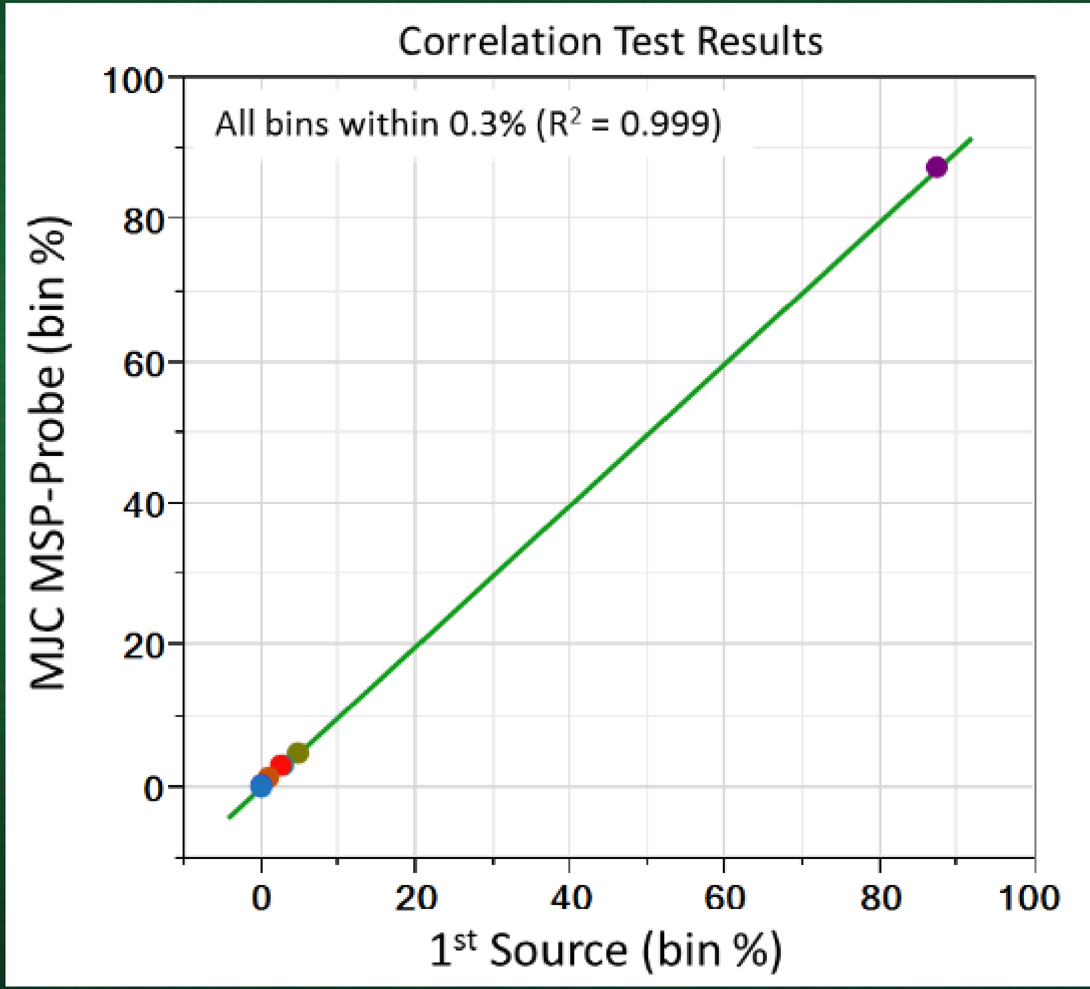
Touch Down	Scrub Diam. (micron)	Scrub Ratio (%)	Scrub Mark
1	16.1	32.2	
2	20.1	40.1	
3	19.7	39.5	
4	19.7	39.5	
5	23.0	46.1	
6	19.1	38.2	

Correlation Determination > 99%

- **Test Conditions**
  - Wafer Overtravel = 150um
  - Octagonal movement
  - Cleaning Overtravel = 100um
  - Cleaning Frequency = 1 clean per 200 wafer TD



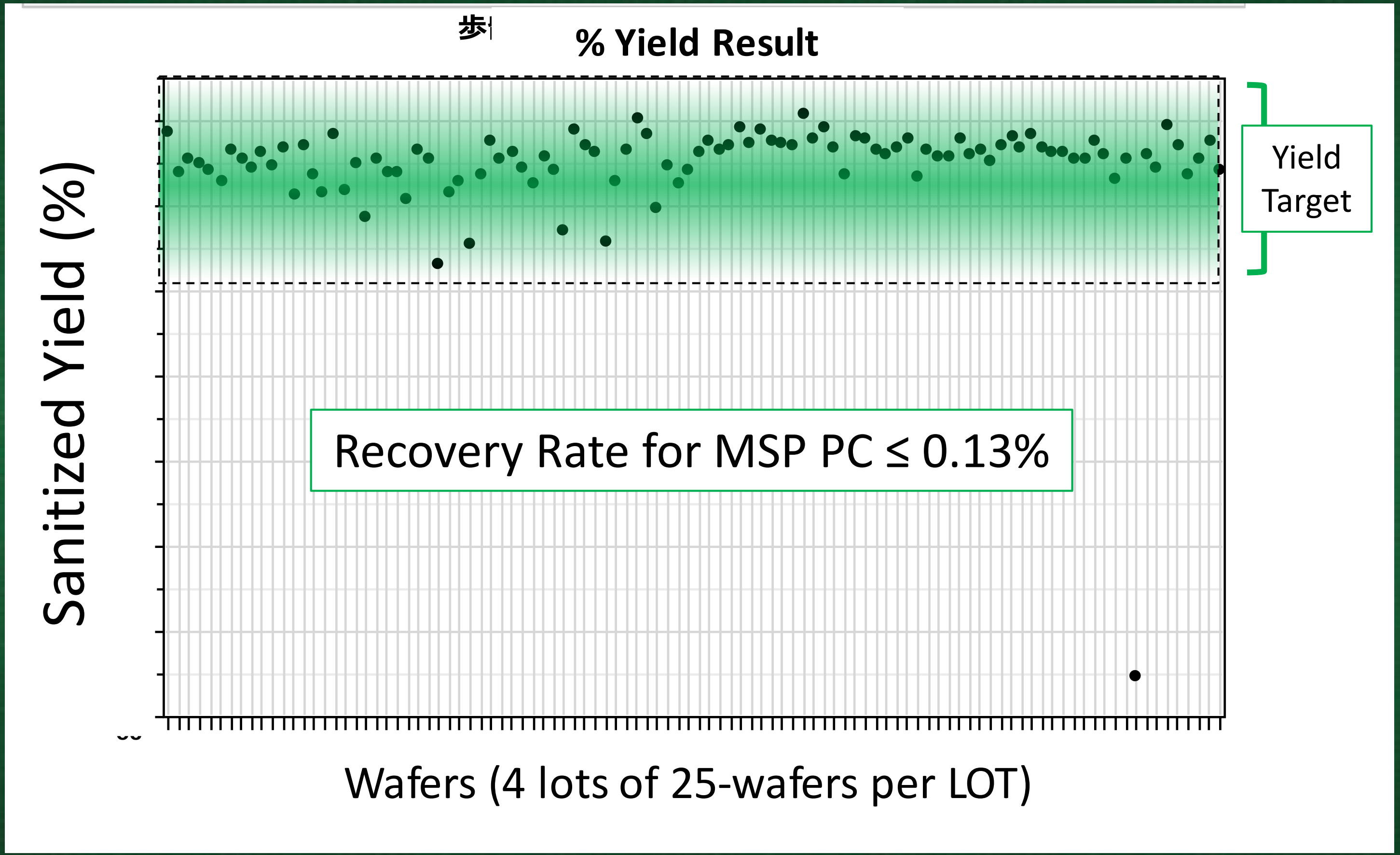
Highly significant positive correlation confirmed



4 x Wafer Lot % Yield Results

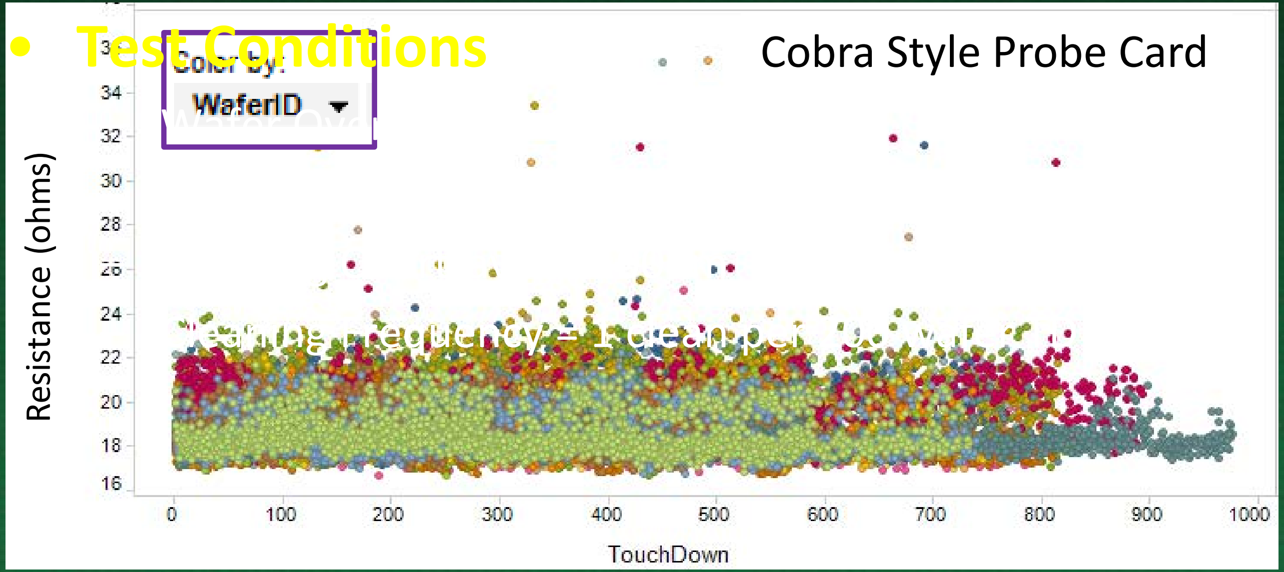
- **Total Yield Average for 4-LOT**
  - First Pass Yield Target was attained and confirmed
  - MSP card had significantly better first pass yields than a comparable Cobra card.

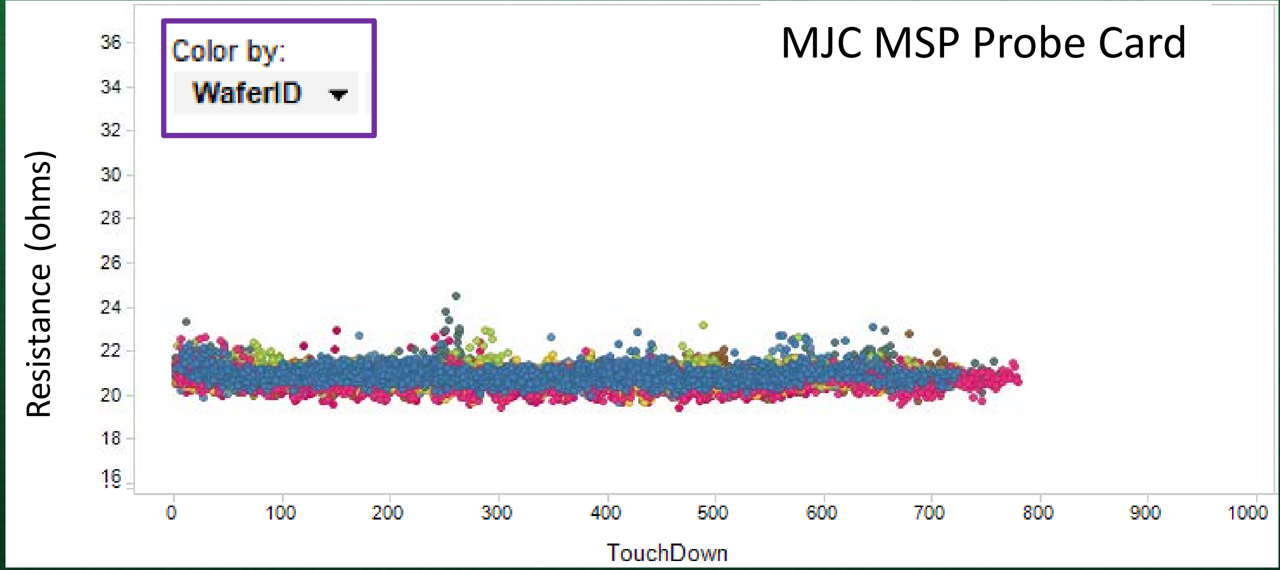
- **MSP card had low recovery rate vs. a high recovery rate observed with the Cobra card.**
  - Recovery Rate for MJC MSP PC ≤ 0.13%
  - Recovery Rate for Cobra PC ≥ 0.50 %

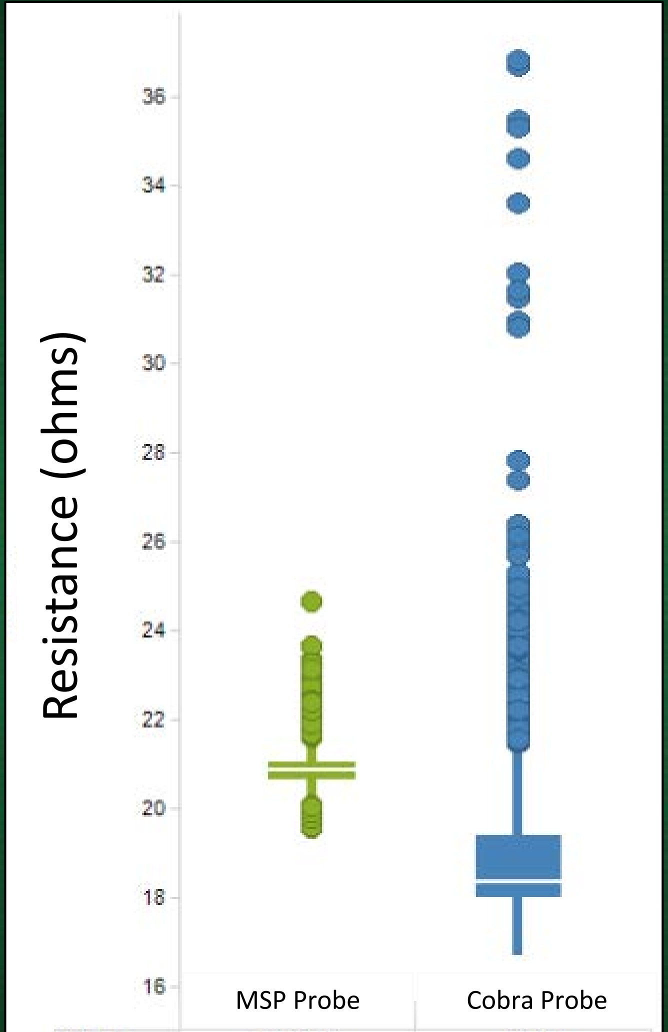


MJC MSP vs. Cobra Probe CRES Trending

- Test Conditions







	MSP Probe	Cobra Probe
Median	20.8629	18.321
Outliers	576	1265
StdDev	0.327531	1.16891
Var	0.107276	1.36635

Summary of Qualification

Property	Requirement	Result	Assessment
CRES vs. OD	OD = 75 to 200um Target OD = 150um	Stable CRES at OD ≥ 50um	✓
Correlation Yield vs. OD	OD = 75 to 200um Targety OD = 150um	Stable Yield at OD ≥ 75um	✓
Bump Damage vs. OD	% Damage ≤ 50% OD = 75 to 200um	% Damage ≤ 40% Max. OD = 200um	✓
CRES vs. TD	TD = 1 to 6	Stable CRES at Max. Allowable TD = 6	✓
Correlation Yield vs. TD	TD = 1 to 6	No additional recovery after 1st retest	✓
Bump Damage vs. TD	% Damage ≤ 50 % at OD = 150um	% Damage ≤ 40% Max. Allowable TD = 6	✓
Test Reproducibility	Statistical Correlation better than 99%	All bins within 0.3% (R^2 = 0.999)	✓
Wafer Lot Result	High 1st Pass Yield Low Recovery Rate	Recovery Rate ≤ 0.13%	✓
Resistance Variance	Improved Stability over Cobra Type	Statistically Reduced Variance	✓

Agenda

- Background
- MJC MEMS Spring Probe (MSP) for Solder Bumps, Cu Pillars, and Pads
- Qualification of MJC MSP Probe on Cu Pillar Devices at End User
  - End User Objectives
  - Qualification Test Plan
  - Results Summary
- **High Volume Manufacturing Validation**
- Summary / Conclusions

High Volume Manufacturing Validation

- **Production Qualification Overview**
  - More than 5000 production device wafers were split across multiple test cells
  - Split Lot Ratio ⇨ MJC MSP (15%) and Cobra Style (85%)
- **Production Metrics comparison for MJC MSP vs. Cobra Style**
  - First Pass Yield Improvement ⇨ <u>0.37% increase in FPY</u> over Cobra Style
  - Significant Reprobe Rate Reduction across 5000 wafers:

Card Type	Average	StdDev
COBRA	0.34%	0.83%
MJC MSP	0.09%	0.08%

  - <u>Avg. 2.69% wafer test time reduction</u> was realized with MJC MSP Probe

Agenda

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Summary / Conclusions

- **Bumps, Pillars, and Pads of next-gen devices continue to shrink in size for higher pin counts with tighter pitches requiring precise and low force contact under various test conditions.**

- **MJC MEMS SP has “tune-ability” of probe force, plunger shape, and contactor metallurgy.**
  - Engineered low probe forces facilitate high pin counts with reduced %-damage
  - Tip geometries designed for CRES stability with low %-damage after multiple touchdowns
  - Contactor shapes and metallurgies optimized for high CCC, low CRES, and %-Yield stability

- **Under HVM conditions at End User, MEMS SP had superior performance over Cobra Style probe technologies.**
  - A 0.37% improvement in First Pass Yield
  - Significantly reduced reprobe and recovery rates
  - Overall 2.69% reduction in average wafer test times

- **Future work**
  - Production probe card performance and lifetime characterization
  - Elevated temperature (125C) test conditions

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- Hideo Kuroyanagi (Micronics Japan Co., LTD)
- Keita Kudo (Micronics Japan, Co., LTD)