"Emerging Test Methods -- *How Auto IC Requirements, Adaptive Testing and Multichip Products are Changing the Industry*"

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GLOBALFOUNDRIES®

Thanks

Disclaimer / Abstract

- *Some of the material in this presentation are my thoughts on these topics.*
- *That is, some comments are NOT the official GLOBALFOUNDRIES position related to future offerings.*

Abstract

Key Industry trends are changing how we Test ICs -- and how we guarantee Quality, Reliability and Yield during the production process. The number of ICs in Automobiles is dramatically increasing -- and these ICs have very unique requirements. Leading-edge companies are using more & more "Adaptive Test" methods -- that are challenging given our dis-aggregated production test processes. Also, multichip products (including ICs from multiple suppliers) are finally emerging; but the challenge is that adequate industry support practices are not yet in place. This talk will both describe these challenges and recommended practices to move the industry ahead.

Outline

- Foundry support for IC Testing
- Multichip Packages – Test Challenges
  - *Heterogeneous Integration – where are we headed ?*
  - *What are industry gaps in supporting advanced packages ?*
  - ***Wafer-level (probe) testing – need to drive improvements***
- How should industry evolve to overcome these challenges ?
  - *Drive to true KGD*
  - *Cross company collaboration, standards enabling test collaboration, more test transparency, …*
- Automotive – Auto ICs vs. consumer ICs – what's different ?
- Adaptive Testing & Advanced Statistical Test Analysis
  - *End-to-End Data Integration and WW / Cross Company Collaboration*

GLOBALFOUNDRIES Fabs

GLOBALFOUNDRIES (GF)

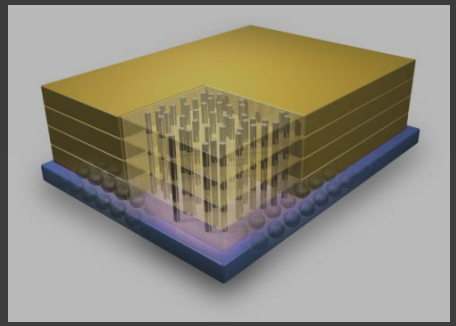
- **GF's primary business is wafer foundry**
  1. *Dresden*
  2. *Singapore*
  3. *Fishkill, NY*
  4. *Burlington, VT*
  5. *Malta, NY*
  6. *China (future)*

Test Engineering for a variety of Technologies

- *FinFet: 14nm, 7nm*
- *ASICs: Cu32, FX14*
- *22FDX®, 12FDX™*
- *8XP SiGe RF (mmWave)*
- *22FDX-MRAM, eNVM*

- **Most of these ICs are designed by other companies.**
  - *e.g., IBM, AMD, … and quite a few other companies.*

- **Over time, GF will be more than "just a wafer fab".**
  - *ASICs, Design methodologies, IP (building blocks), advanced packages (Post Fab services)*
  - *In some cases, GF will offer "products". (e.g., sub-assemblies)*



GLOBALFOUNDRIES Test Facilities

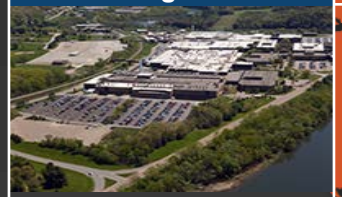
Plus Inline / eTest at each fab

Burlington
Production Wafer Probe Test Center

OSAT – IBM, Bromont, Canada

Dresden
Production Wafer Probe Test Center

Burlington VT



East Fishkill, NY

Dresden, Germany

New fab in China

OSAT Partners

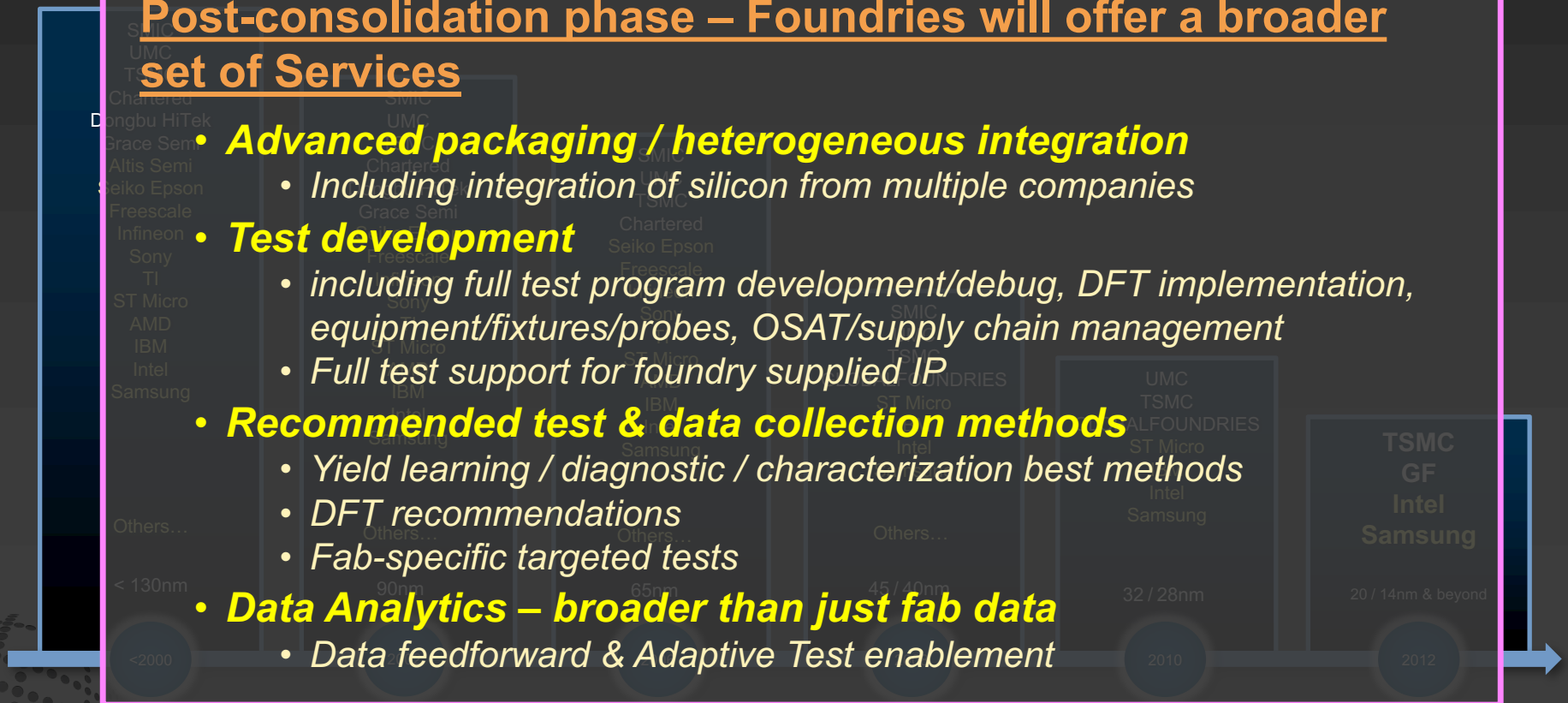
Malta, NY

Singapore

Malta, NY
Technology Development
14nm – 7nm
Test & New Product Introduction

Singapore
Test Development, OSAT support

Consolidation of Semiconductor Fabs



Post-consolidation phase – Foundries will offer a broader set of Services

- ***Advanced packaging / heterogeneous integration***
  - *Including integration of silicon from multiple companies*
- ***Test development***
  - *including full test program development/debug, DFT implementation, equipment/fixtures/probes, OSAT/supply chain management*
  - *Full test support for foundry supplied IP*
- ***Recommended test & data collection methods***
  - *Yield learning / diagnostic / characterization best methods*
  - *DFT recommendations*
  - *Fab-specific targeted tests*
- ***Data Analytics – broader than just fab data***
  - *Data feedforward & Adaptive Test enablement*

Test Support by IC Foundry

Historical View

- **Foundry builds wafers – including etest/Inline Test**
- **Test for technology development** *(testsites, etc.)*
- **Foundry supports product wafer probe test for select products**
  - *Fabless customer supplies test solution*

Future??

- **Product Test is an integral part of the foundry offering**
- **Foundry provides wide range of Test & DFT services.**
  - *Test Development*
  - *Test for foundry IP*
  - *Production Testing*
  - *Test for Yield learning*
  - *Test recommendations (e.g., based on fab learning)*
  - *Outlier screens*
- **Foundry supports Advanced Multichip Packages**
  - *Including integration of silicon from multiple companies*

Test Support Models

	ASICs	"Hybrid"	Foundry
Product Delivery	Fully tested modules		Tested wafers or tested dies
GF's Role in Testing	GF owns all components testing.		Wafer probe test as a service – enabling yield learning
Test Program Development	GF		Customer delivers wafer test program to GF
Yield/Quality/ Reliability Ownership	**Supplier Provides Full Test Solution**	***Collaboration between Customer and GF***	Customer owns Quality / Reliability and Test & Circuit portion of yield **Customer - driven Solution**
IP / DFT Definition / Ownership	GF owns all embedded IP – including DFT / Test Methods		Customer owns DFT & IP testability.
Yield Learning / Diagnostics	GF		GF provides a level of yield analysis / diagnostics
Test Data Analytics / Stat Methods	GF applies advanced data methods as required		Test data analytical methods are defined by customer

Design Enabled Manufacturing (Y2011)

From Bob Madge, GLOBALFOUNDRIES

Major Foundry Challenges:

1. **Technology Bring-up** – *need early design/process correlation data. DFM simulation/testchips losing effectiveness (complexity)*

2. **Volume Product Ramp** – *need yield/quality/rel feedback. Need to "teach" in-line metrology/tools so issues can be identified in-fab.*

3. **Cost/Capacity** – *need more flexibility in test capacity. Foundries currently too dependent on customer tester, DFT, S/W*

How can Test help?:

- **Volume test data and Diagnostics** *on early product-like vehicles. Need much faster, much more adaptive and easier to use and correlate to design.*

- **System Test correlation to Fab.** *Outlier screens have reached their limit. Need system correlation back to fab. tool (e.g., Variability, defect)*

- **Test program/pattern conversion and Adaptive test** – *enable flexible control of the "virtual test floor". Resolve data security through standards.*

Design *Enabled* Manufacturing (Y2011)

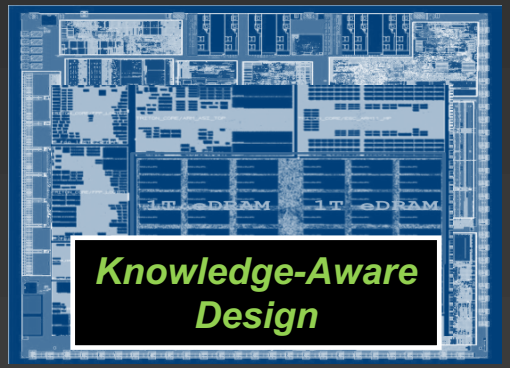
Foundry / Design / Test Co-optimization

Data

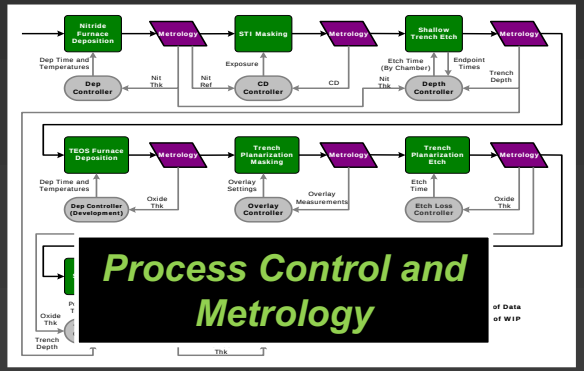
Process Statistics and capability

Data

Design-based Yield Diagnostics



Knowledge-Aware Design



Process Control and Metrology

Adaptive Test

Design statistics & care-abouts

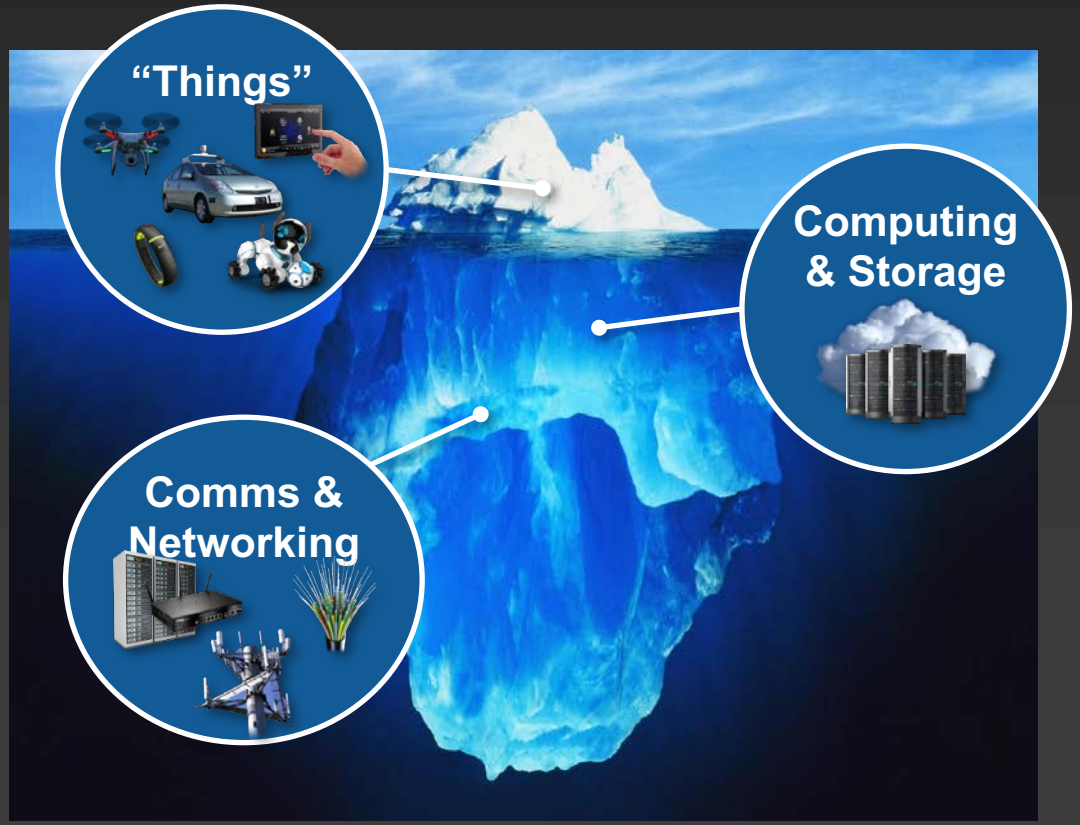
Data

Process/Design Sensitivities

Data

What Will Drive Growth…

2016	
$16B	IoT
$32B	Automotive
$0B	5G
$4B	AR/VR
$5B	AI

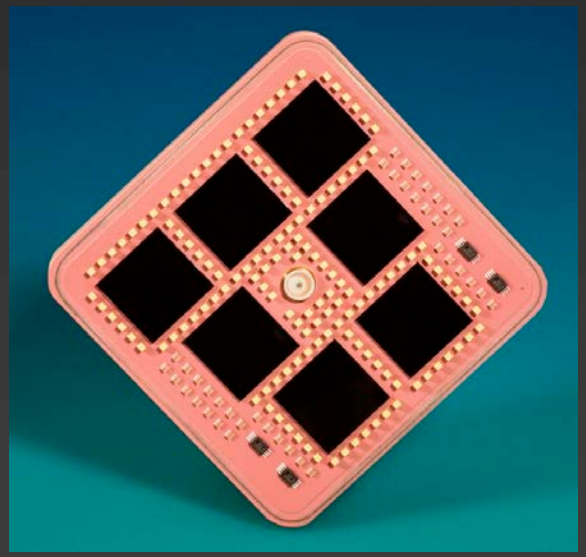


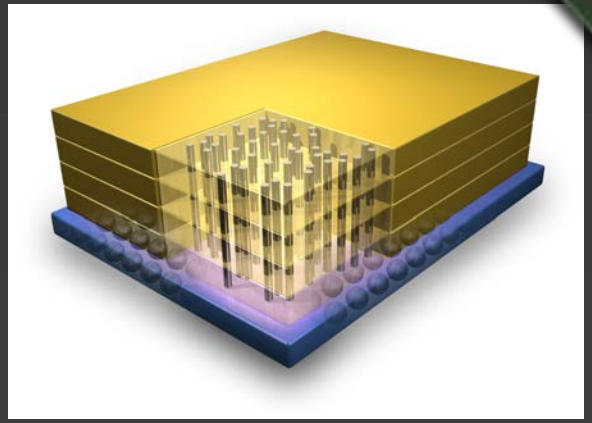
Sources: (a) IoT; GLOBALFOUNDRIES estimates on Gartner data; (b) Automotive: GLOBALFOUNDRIES projections on Gartner and IHS actuals and forecasts; (c) 5G: Mobile Experts; (d) AR/VR: GLOBALFOUNDRIES projections on Goldman Sachs and Bank of America and Gartner data

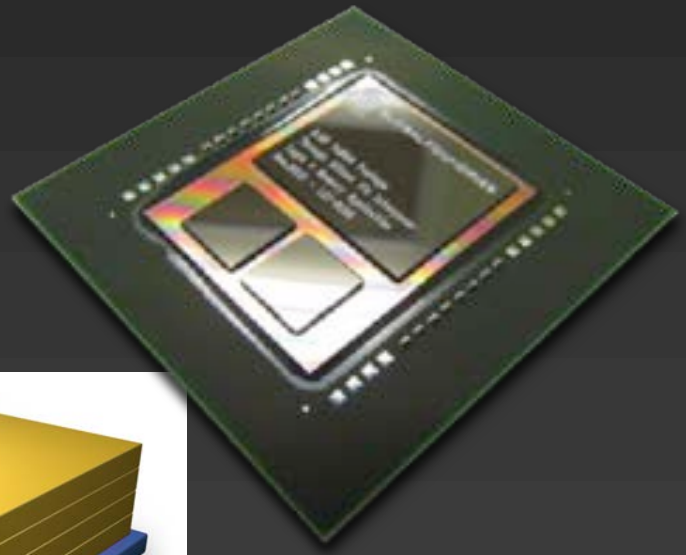
Crazy Growth of Data -- How much will we store ?

Estimates for number of "things" by 2020 range from 25B to 14T

Multichip Packaging Trends



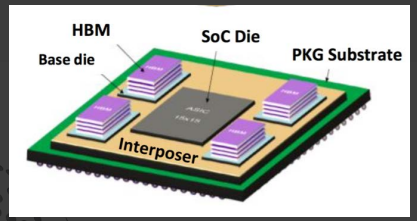


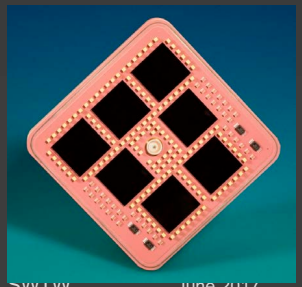


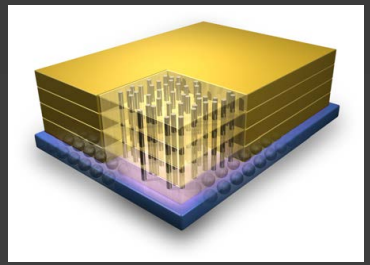
Industry Trends driving Multichip Packaging

- **Moore's Law is slowing down. Semiconductor scaling is not achieving historic levels of higher densities, lower cost and higher performance.**
  - *Move to newer technologies provide less performance gains and the improvement in cost / transistor has slowed.*

- **Another approach to higher density is to integrate multiple bare dies onto the same package .. or to "stack dies".** *("heterogeneous integration")*
  - *2.5D, 3D, MCMs (multichip modules), Wirebond Chip stack, WLFO, …*







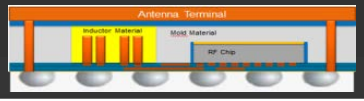
Silicon Scaling Alternatives – Packaging Services

Cost & Power

IoT/RF

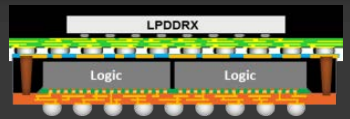
Mobile

ASIC/Server

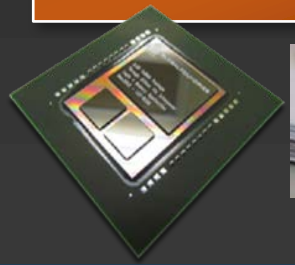


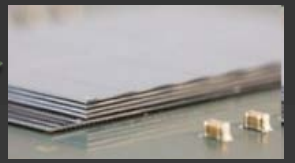
Substrates + Integrated Passives

Wafer Level Packaging



2.5D
3D
Photonics



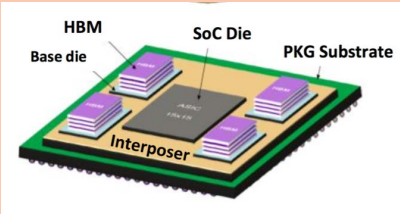


Bandwidth and Interconnect Density

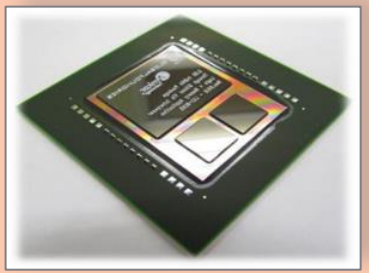
Requirements	IoT/RF	Mobile AP	ASIC Server
Interconnect	Low cost multi-chip	Wafer level packaging	High bandwidth
Development Focus	Lowest cost processes	RF differentiation	Large thin 3D die stacking Photonics
Supply Chain	Partner for high volume	Partner for high volume	Internal development for value extraction, IP protection

Advanced Packaging / Multichip Examples

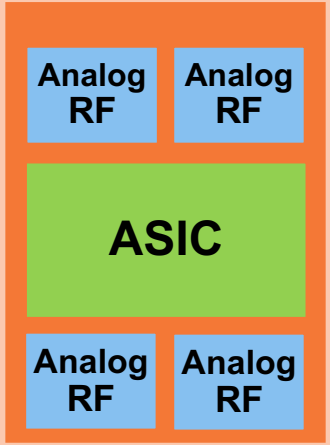
2.5D HBM

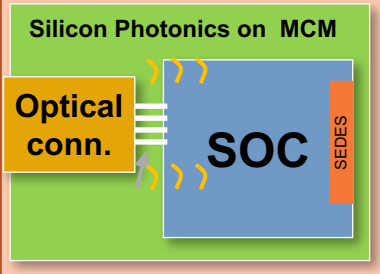


ASIC / SOC
plus
2-4 HBMs / Product



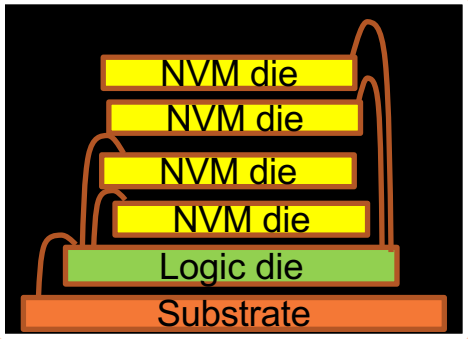
MCM

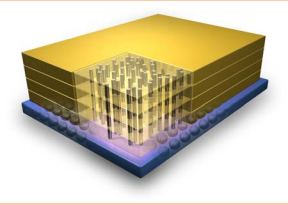




Chip Stack / 3D

ASIC/SOC plus memory





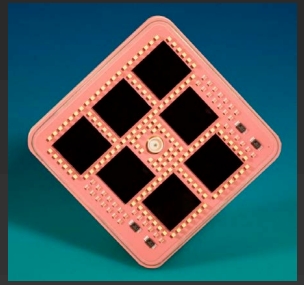
Heterogeneous Integration Industry Roadmap

- **There is an industry group defining the "Heterogenous Integration" roadmap – including test.**
  - *Dave Armstrong of Advantest is leading the test section.*

<u>The roadmap (e.g., Y2027) is interesting to think about</u>

- ***Is the roadmap vision that any IC can be purchased as a bare die ?***
- ***Can anyone purchase these bare dies and be the integrator ?***
- ***Will all required test information be provided ?***
- ***Will there be "plug & play" capability ?***

Test for Advanced Multichip Packages

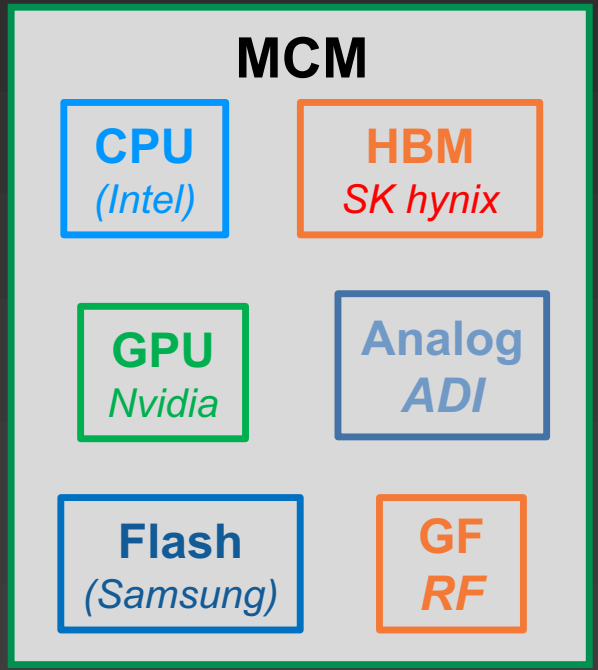


- **Multichip package (MCP) testing has been around for many years**
  - *e.g., >90 chips on MCMs in the mid-1980s*
- **ICs on emerging MCPs include RF/mmWave, Silicon Photonics, Analog, ASICs/Processors and DRAM/memory**
- **GF has a number of advanced packaging solutions currently in production – with more in development.**
- **We're finding deficiencies in current industry practices for multichip testing.**

Challenges of Testing Multichip Products

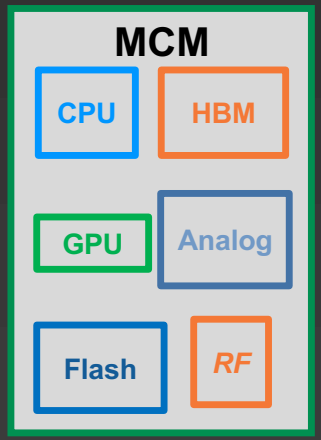
Example MCM *(obviously made up)*

- ***What is KGD quality of each component ?***
- ***Package test – will all companies share all Test information to enable thorough testing ?***
- ***Yield/Quality/Reliability Management – the company who is the "integrator" is the owner for the entire packaged product.***
- ***Do the "business incentives" encourage these companies to collaborate ?***
- ***What does the optimized test flow look like ?***



As the Integrator – what Test details do I want ?

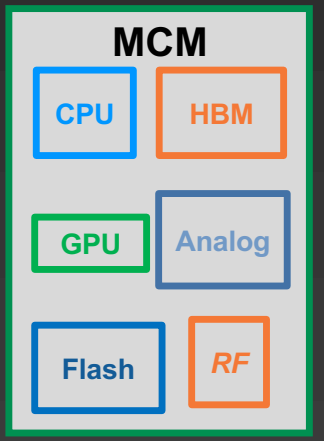
- ***All Test Patterns / Test Content***
  - *Option of complete test content at Final Package Test*
  - *Production (sync?), diagnostics, characterization, …*
    "the kitchen sink" patterns
- ***All details related to DFT***
  - *e.g., DFT ports, 1687, diagnostic data collection, …*
- ***Full Test Specs*** *(voltage, temp, IDDQ, retention, refresh, …)*
- ***All details related to circuitry calibration & tuning***
- ***Memory Repair & Logic Repair***
- ***Embedded sensor access information***
  - *Monitors: voltage, Vdroop, temperature, noise injection, …*



As the Integrator – what Test details do I want ?

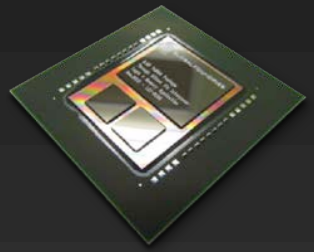
- ***Except for 2.5D – there are not industry standards or accepted practices for addressing these test issues.***

- ***Does P1838 standard address this issue?***
  - ***Not Really.***
  - *P1838 " … description of the Test Wrapper features in a standardized human- and computer-readable language. ... The proposed standard does not mandate specific defect or fault models, test generation methods, nor die-internal design-for-test, but instead* ***focuses on generic test access to and between dies in a multi-die stack."***



2.5D HBM Test Flow

(Potential Test Steps in orange blocks)



Silicon Interposer Wafers

- Inline
- Frontside
- Backside
- Laminate → Assembly
- Interposer + Laminate

ASIC/SOC/CPU

- Wafer / Hot
- Wafer / COLD
- Assembly
- Partial Assembly

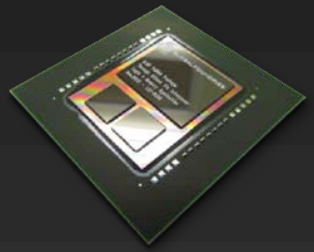
HBM

- Assembly

- FT: COLD
- Burn-in
- FT: HOT
- Component SLT
- ship

2.5D HBM Test Flow

(Potential Test Steps in orange blocks)



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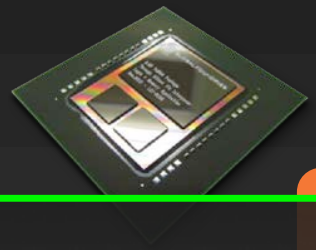


ship

- **Worst Case: ~11 test steps**
- **Clearly, that isn't affordable**

Interposer test:

- ***Probing fine pitch ubumps is very expensive – and will be even more difficult/expensive with next generation interposers.***
- ***Goal is to drive yield to level where interposer electrical testing is not required***
- ***But – what are the best practices to drive diagnostics / yield learning?***

Component SLT

FT: HOT

Burn-in

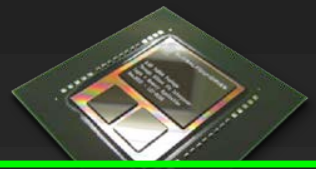
FT: COLD

Assembly

+ Laminate

2.5D HBM Test Flow

(Potential Test Steps in orange blocks)



ship

ASIC/SOC Wafer Testing

- ***Goal is to drive testing content back to wafer test.***
- ***Challenges:***
  - ***Additional test insertion (compared to single chip package)***
  - ***Full ASIC IO probing (possible)***
  - ***Wafer probe test environment (noise)***
  - ***High-speed Serial (HSS) IOs (e.g., 28G, 56G)***

Silicon Interposer

Component SLT

Wafer / Hot

Frontside

Wafer / COLD

Burn-in

Assembly

Assembly

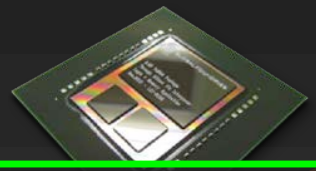
HBM

Interpose

Laminate

2.5D HBM Test Flow

(Potential Test Steps in orange blocks)



ship

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  - *Wafer probe test environment (noise)*
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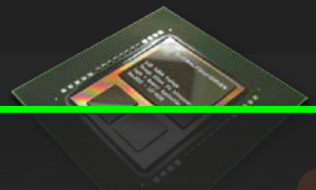
Partial Assembly Test

- *Only test for IO interconnect ?*
- *Are there any assembly-induced failures that must be tested ?*

Laminate

2.5D HBM Test Flow

(Potential Test Steps in orange blocks)

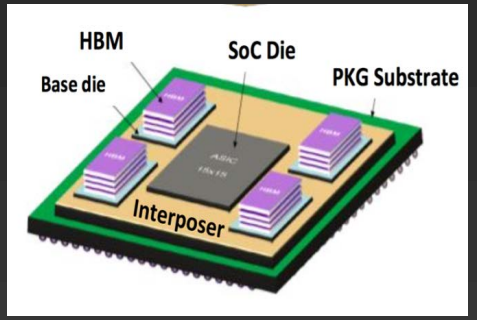


Final Package Testing

Ideally, we'd only test for chip-to-chip interconnect and package IOs.

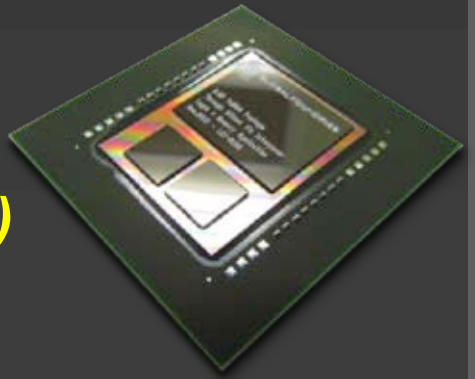
- ***BUT – will KGD quality be sufficient to enable skipping testing of internal circuitry of ASIC and HBMs?***
- ***Is testing at multiple temperatures required ?***
- ***HBM testing – is running memory BIST required ?***
  - ***Is HBM memory repair required ?***
  - ***Is "DA Port" testing of HBM required ?***
- ***Is "Lane Repair" testing / configuration required ?***
- ***Is Final Test on ATE sufficient ?*** *(SLT test step not required)*
- ***Is calibration or tuning required after packaging ?***
- ***Does the packaging process induce any internal faults either in the ASIC or HBM ? What test content is required to detect these faults ?***

Other challenges related to 2.5D HBM Test



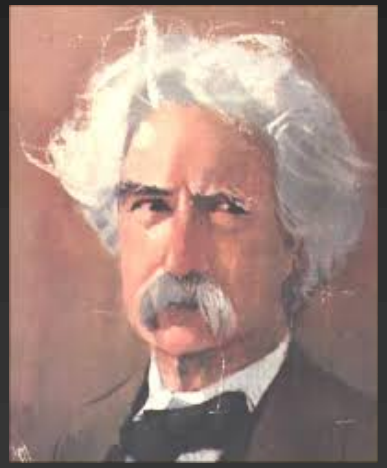
- ***What about testing customer returns ?***
  - *Do returns have to visit both the integrator and the HBM provider (and ASIC provider) for extended characterization / diagnostics ?*

- ***If we have a ASIC-to-HBM IO failure – how do we diagnose the failing component ?*** *(e.g., is the fault in the ASIC IO … or interposer … or HBM IO ? .. or ubumps?)*
  - *Improvement of PFA methods*



- ***Can HBM testing be "plug & play" (transparent) using HBMs from different suppliers ?***

What is a KGD ?



- ***Known Good Die (KGD)***
  - *"Known Not Bad Die", KTD: "Known Tested Die"*
  - *KSD: "Known Sellable Die" … "Known Salveable Die"*
- ***What is the expected level of fallout at Test after we package KGD components?***

- ***The problem really isn't "Test" – the problem is yield/fallout/cost.***

KGD proposed definition:

- ***"The shipped quality & reliability levels of the bare die are equivalent to the single chip package version of the die."***
  - *BUT … we still have to package the device.*
  - *Also … there may not exist a single chip package version.*

Wafer Probing Test Challenges

- ***Probing / electrical testing each uBump on Interposer?***
  - ***It may be possible today … using expensive solutions (cost!)***
  - ***Future generations will even be more expensive.***
- ***ASIC / SOC / CPU testing – will the probe electrical environment allow us to drive all testing content back to wafer test ?***
  - ***Target probe size & pitch & probe count & current density ?***
    - *20um size ? 40um pitch ? 30K probe count ?*
  - ***Noise (e.g., full test without package-level capacitors)***
  - ***HSS test at >28G … probe & external loopback ?***
  - ***RF frequency requirements … >40GHz***
- ***Test Temperature requirements (Automotive … >105C ?)***

Multichip Modules (MCMs) – besides 2.5D

- ***Diverse set of technologies (test req.) on the same package:***
  - *CMOS, RAMs, FDSOI, RF/mmwave, SiGe, Silicon Photonics, …*
- ***JESD235 defines much of the design-for-test details related to HBMs on a 2.5D package.***
- ***There is no similar spec for other multichip packages that do not have HBMs.***
- ***So … MCMs have many more testing challenges compared to 2.5D HBM. For example:***
  - *Test methods, content for each die*
  - *High-speed Analog: IO access, post-package calibration*
  - *RAMs (besides HBM): direct access, test & repair*
  - *Thermal management (particularly 3D & chip stack)*

Challenges related to Multichip Package Test

- Handling
- Failure Modes introduced during Package build
- KGD
- Thermal

Automotive Semiconductor Testing

Rapid Technological Advances
New York City, 1900

One Automobile

Lars Reger, NXP
ETS, 2016

Rapid Technological Advances
New York City, 1913

Zero Horse-drawn Carriages

Lars Reger, NXP

Automotive ICs

- Automotive ICs is one of the biggest (most impactful) trend in the Semiconductor industry right now.
- Today, most ICs in cars perform video-assist and entertainment.
- Self-driving cars (or at least driver assist)
  - *Semiconductors will be controlling "everything".*
- Robust, resilient, fault-tolerant Semiconductors are critical for Automotive ICs.
  - *Next generation Auto ICs will be at N-1 technology (e.g., 14nm)*

Self-Driving “Platoons” of Vehicles

A number of companies in Europe have collaborated with demonstrating self-driving vehicles on the Autobahn in Germany.

“If an object is within 10 feet – stop”

Lars Reger, NXP

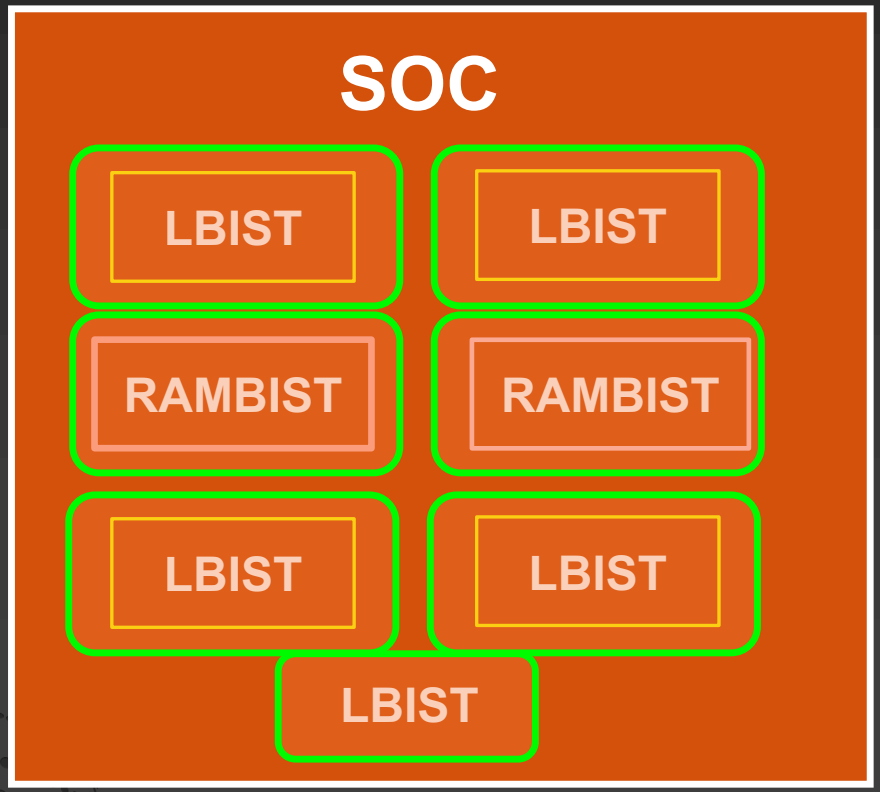
“Self-driving Automobiles”

Lars Reger, NXP

How are Automotive ICs different from “normal ICs” ?

- **Automotive requirements include having all ICs constantly testing themselves.**
- **The Quality & Reliability requirements for Auto ICs are 10X-100X more challenging than consumer ICs.**
  - *For many applications, if IC has a failure – the effect is relatively minor compared to a failing Auto.*
- **An emerging requirement is that ICs need to be fault tolerant. The goal is that single faults will not cause a functional failure.**
- **Many of the required best processes for Automotive ICs are good practices that can be applied more broadly.**

Auto ICs – Continuously Testing Themselves



- ***Embedded processors (ARM) and logic blocks will be continuously running built-in self-test*** *(IOS26262)*
  - *"rotating" operation / BIST*
  - *e.g., every 200ms core goes offline and runs BIST in 20ms* ***(report to system if failure)***
- ***Embedded memories will also be continuously running BIST & repair.***

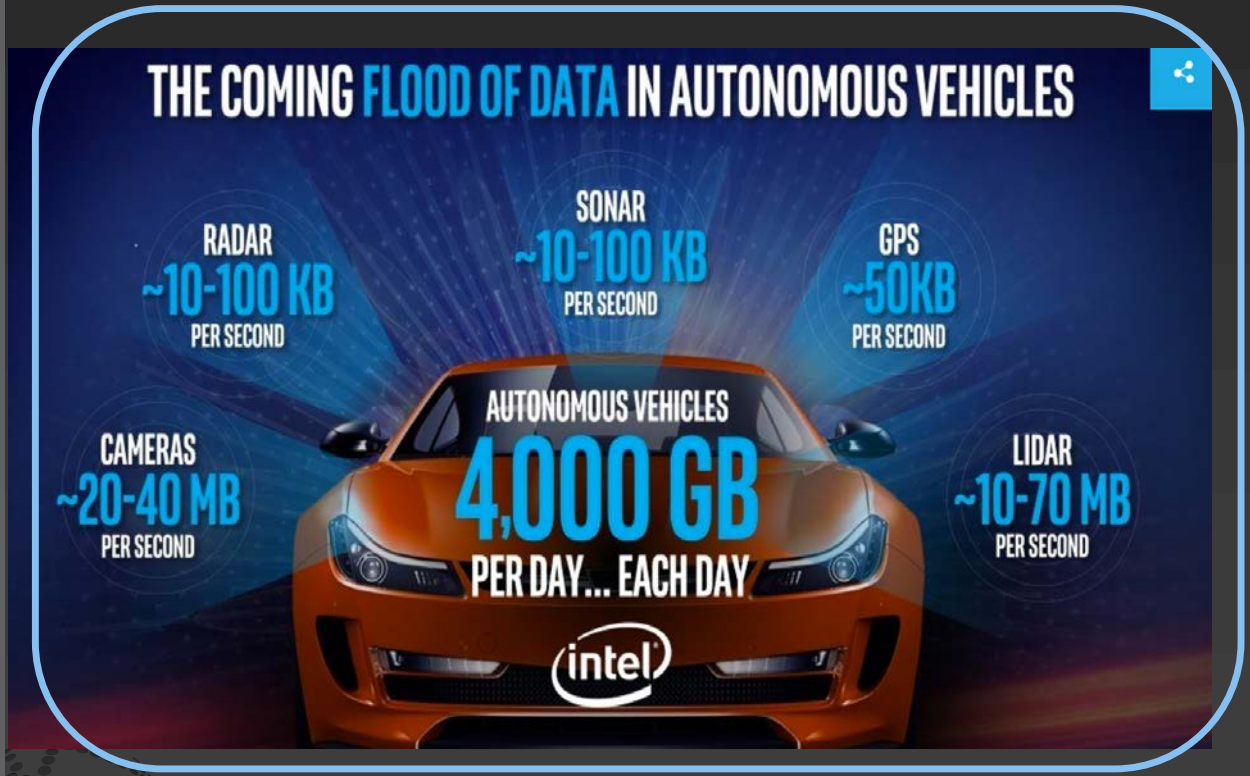
What is next for Auto IC testing ?

- **BIST for other circuitry.** *e.g., PLLs, IOs, analog (ADCs, DACs)*
- **More thorough quantification of test completeness**
  - *Test coverage of all circuitry (including analog), more complete fault models (Cell Aware + all extensions, bridging, etc)*

Fault Tolerance / Resilient Operation

- ***Design practices to avoid marginalities.*** *(e.g., VDD, timing, DFM/layout sensitivities)*
- ***Multicore architectures – where operation continues if one core fails.*** *ICs will "heal" themselves.*
- ***Voltage margining during application.*** *BIST or online test at extended conditions – then dynamically adjust voltage or clock frequency to avoid marginal failures.*
- ***Extreme "phone home" data collection -- then analysis and alerts.***

Automotive ICs – Continually gathering data



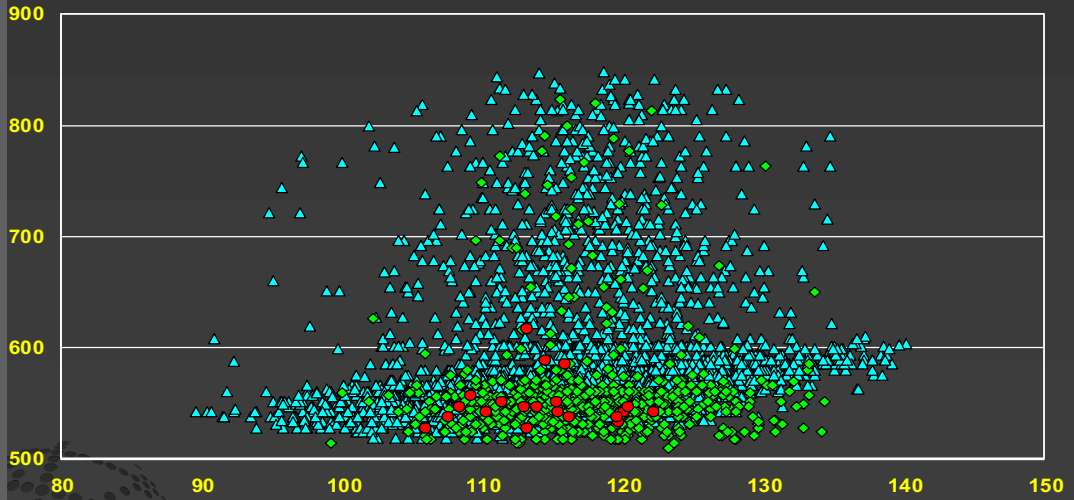
[Intel]

A key question is what data is useful for improving IC quality & reliability and fault tolerance.

Then how to store & transfer key data for analysis & alerts.

Statistical Test Methods

"Advanced Statistical Test Methods" (and Adaptive Testing) must be used to improve IC chip Quality & Reliability – and to reduce Test Cost.



Evolution of the International Test Conference:

What was the test industry drivers ?

Up through the late 1990s

Test Equipment

(Teradyne, Advantest, Verigy, …)

~Year 2000 to ~2013

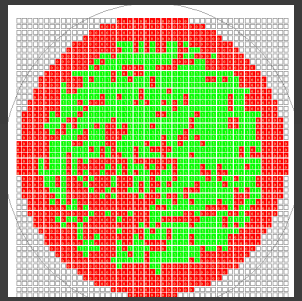
Design-for-Test EDA Companies

(Synopsys, Cadence, Mentor Graphics)

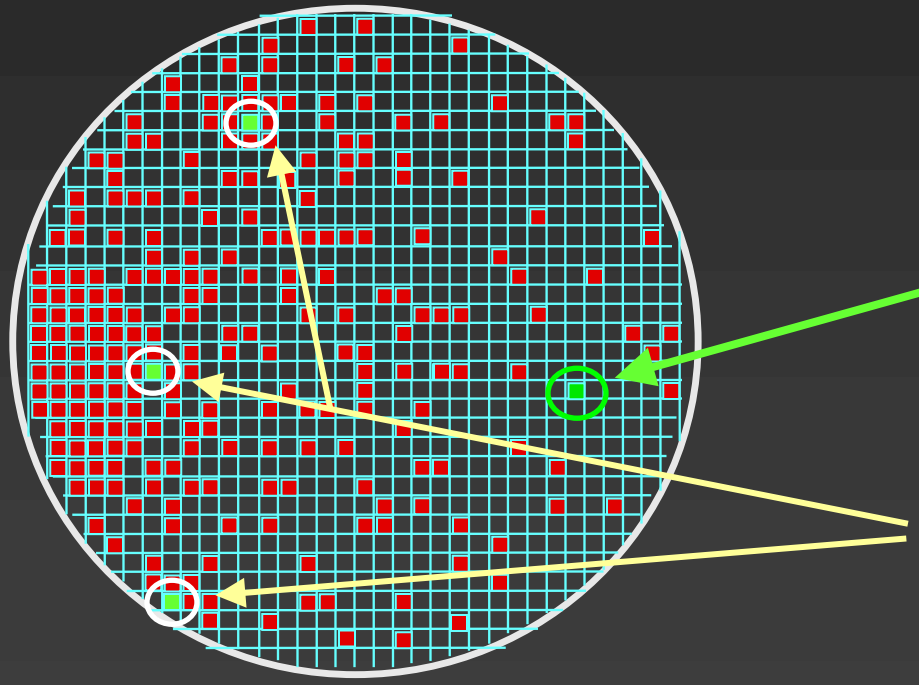
Since Y2013-2014

"DATA"

(Optimal+, Galaxy, PDF Solutions, etc)



“Statistically more Reliable ICs”



Defects cluster

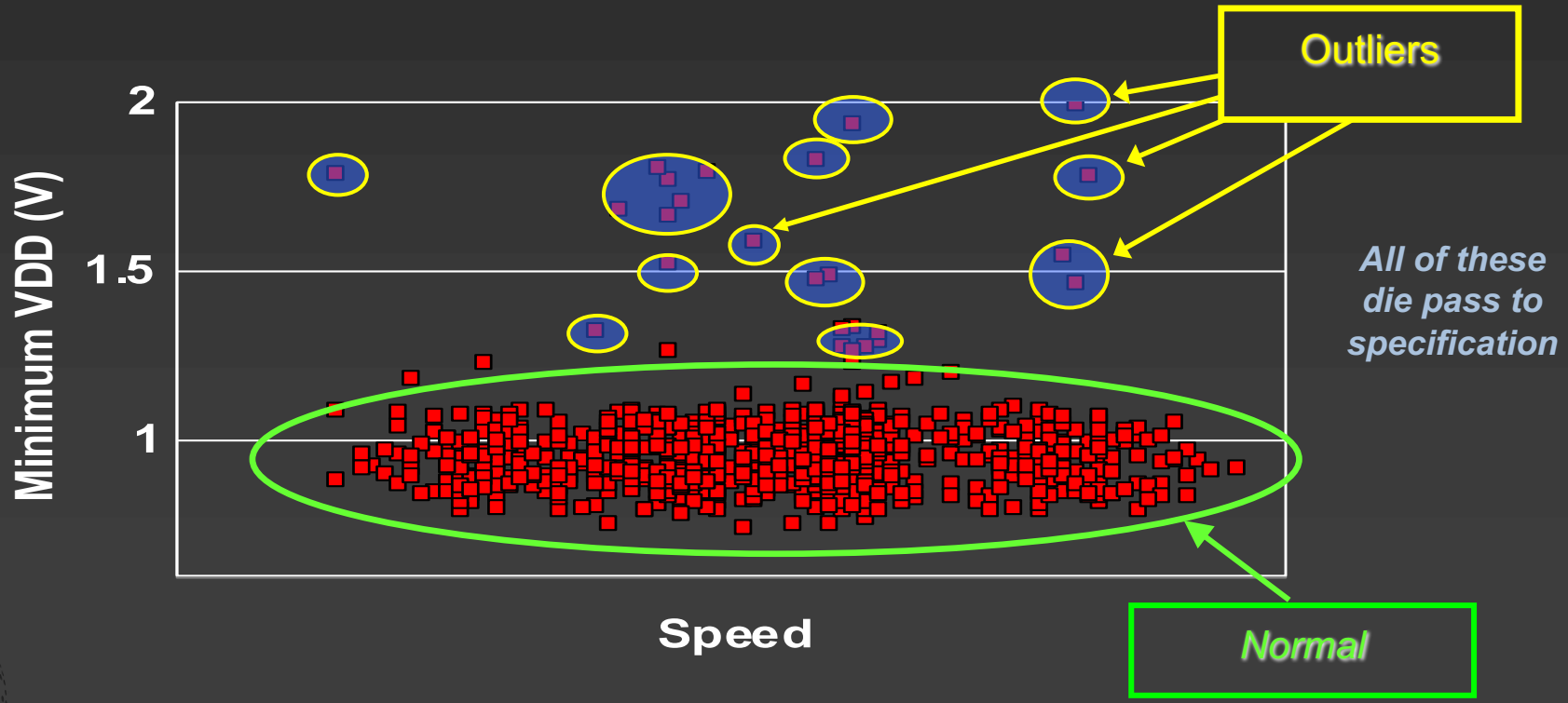
This device

… is statistically more reliable than these three devices

Red chips are fails …
black & green chips are passes.

Statistical Outliers

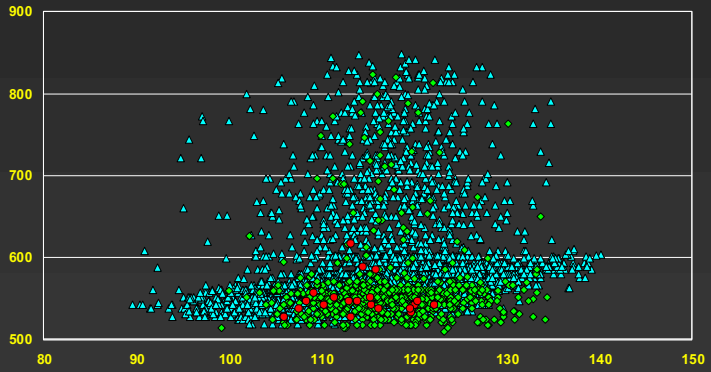
Should we reject outlier die just because they behave a little differently ?

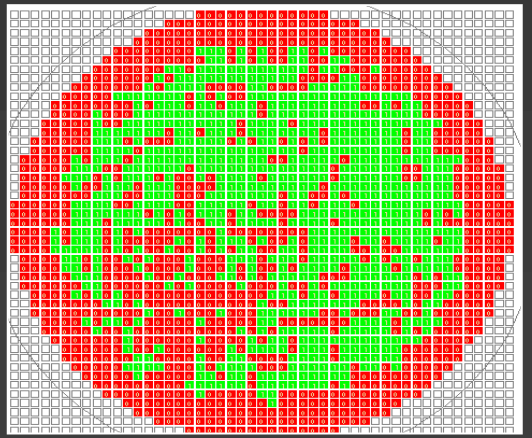


Test Data Analytics required for Auto ICs

Example Statistical Methods

- *Statistical Bin limits (static limits)*
- *Nearest Neighbor Bins*
- *Nearest Neighbor Bins – across wafers*
- *Nearest Neighbor Residuals*
- *DPAT/SPAT*
- *Statistical analysis of Test Data – Post Wafer/Lot (uni/bi/multi-variate analysis*
- *Test Sampling for TTR*
- *Data feedforward – any test data or analysis output from one test step to a future one*





Adaptive Testing

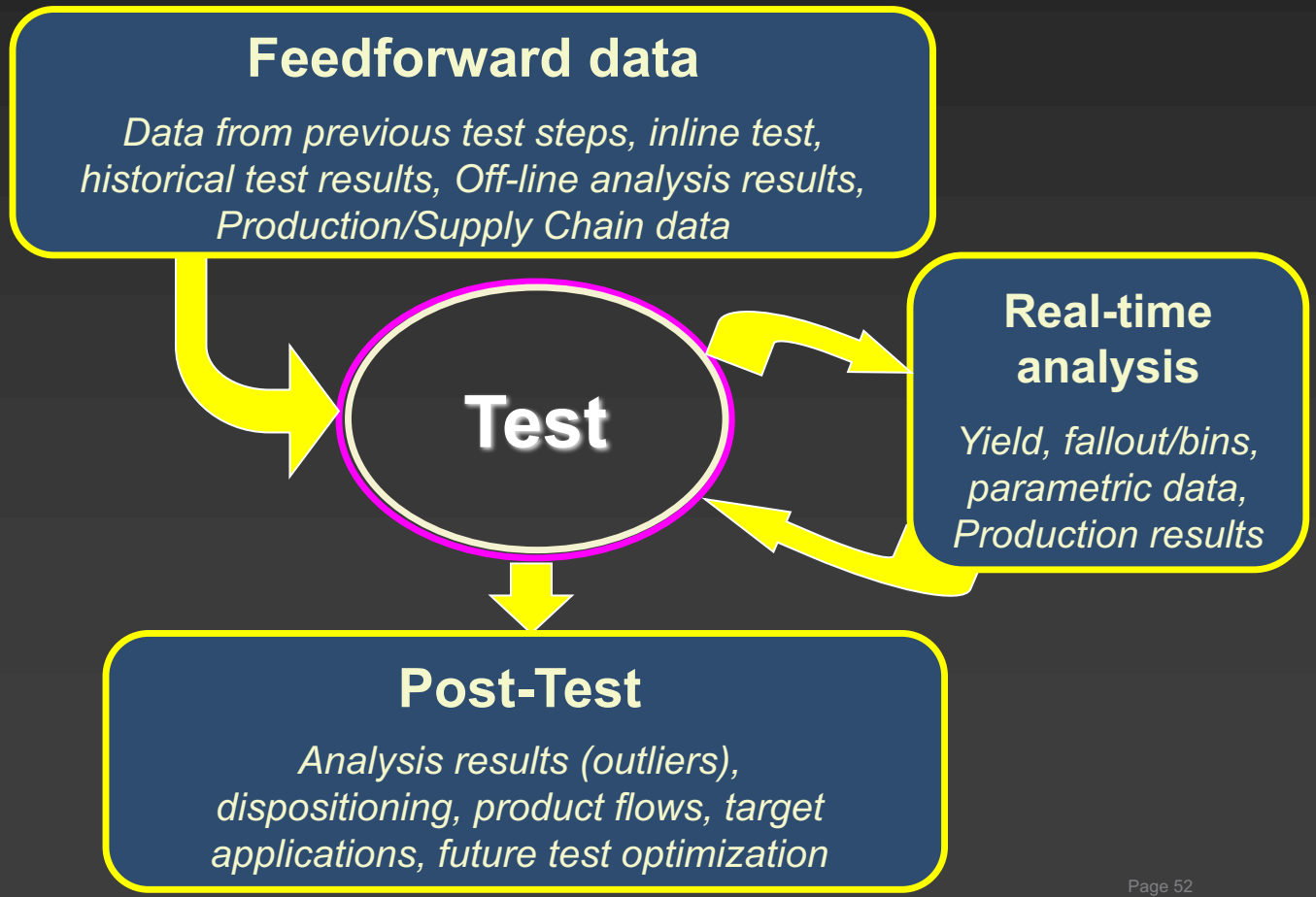
Adaptive Testing automatically changes production test content, flows, limits to provide benefits such as:

- ***Lower Cost***
- ***Better Product Quality & Reliability***
- ***Excursion Prevention***
- ***Improved Yields / Yield Learning***

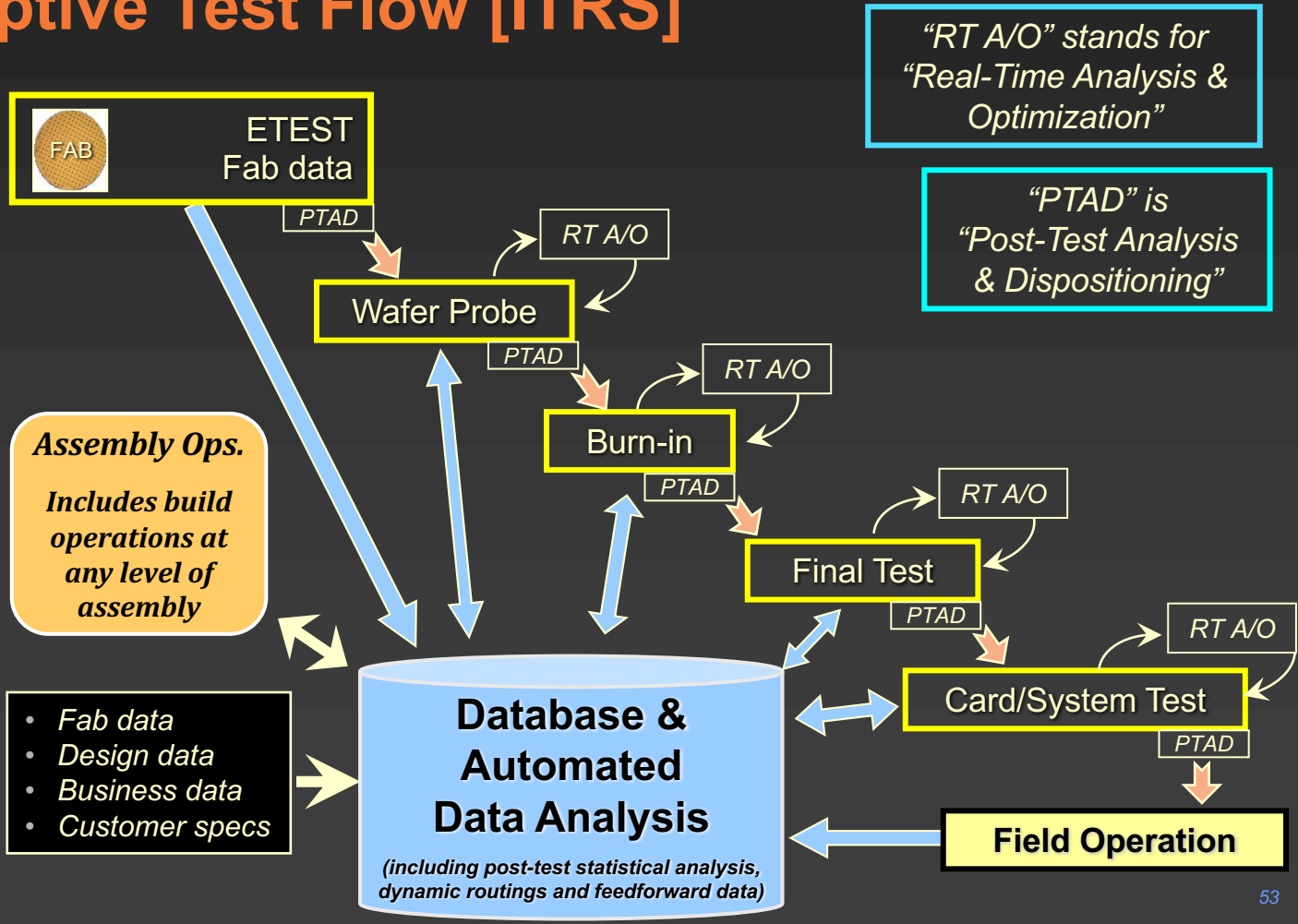
HIR Adaptive Test Roadmap

- *The following slides are from the Heterogeneous Integration Roadmap (HIR – previously ITRS) "Adaptive Test Roadmap"*
- *We have an existing 15-page document that described the Adaptive Test industry roadmap.*
- *We're working on a revision now.*
- *If you'd like to get involved in the review/update – send me an email. (phil.nigh@globalfoundries.com)*

Adaptive Test Flow -- Single Test Step

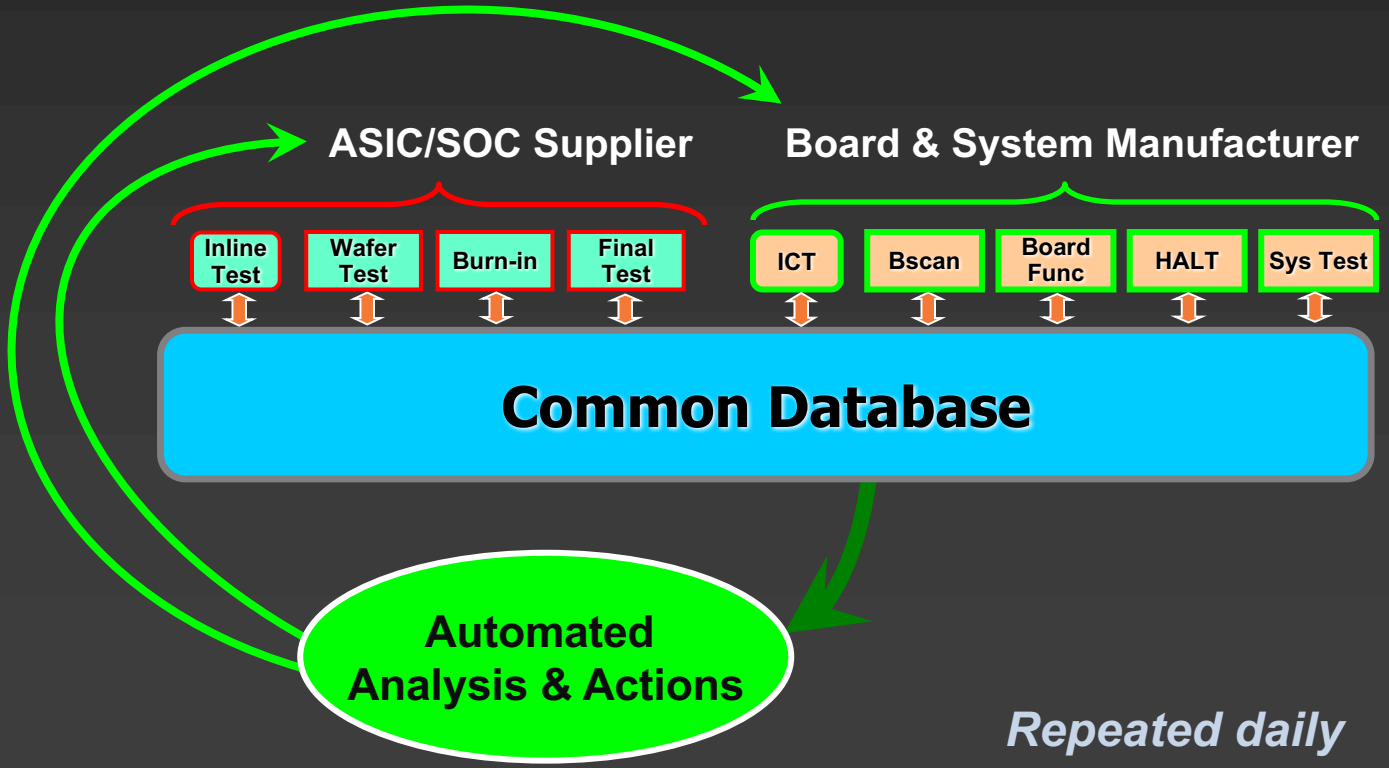


Adaptive Test Flow [ITRS]



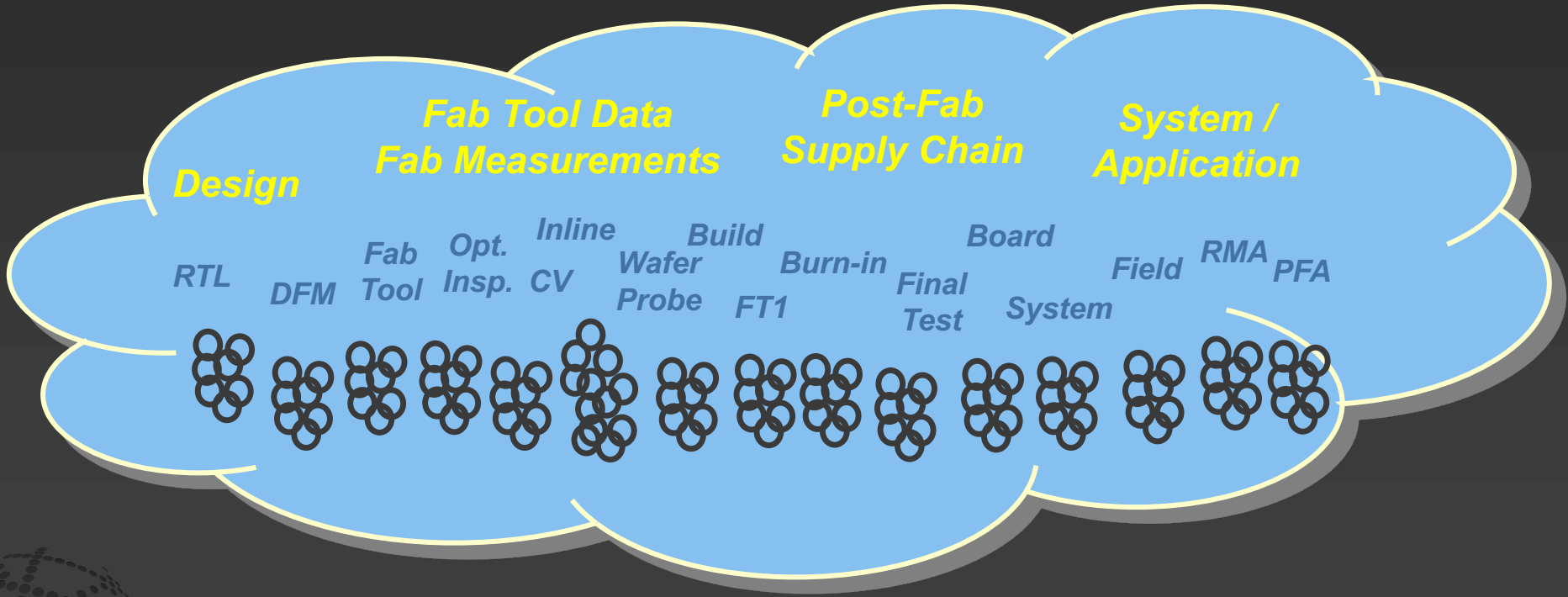
End-to-End Correlation & Optimization

automated … continuously adapting & optimizing



Repeated daily

Continuous End-to-End Statistical Analysis of all data



End-to-End, Cross Company Analytics

- **Today, only limited data is shared between company**
  - *e.g., IC chip supplier mainly ship passing dies – without any data going along with them*
  - *System-level companies using these dies may only share DPM general measurement data. (unless there is a specific problem)*
- **To enable complete E2E analysis … "all data" would be shared.**
  - *e.g., if chip-level yield changes – system company would like to know.*
- **Full data sharing could enable methods like "system-level adaptive Testing"** *(system testing changes based on component data)*
- **In the future, will IC suppliers be supplying an Index representing expected Reliability & Quality with each IC ?**

Summary

- ***Advanced Multichip Packages introduce some unique test challenges.*** *(business collaboration & technical)*
- ***Automotive ICs are increasing and driving more of the semiconductor industry.*** *Quality & Reliability requirements forces improved test-related methods.*
- ***End-to-End Statistical Analysis & Adaptive Testing are an emerging opportunity to improve Product Quality, Reduce Cost and Remove Excursions.***