SW Test Workshop
Semiconductor Wafer Test Workshop

Typical “Pain Points” in Wafer Level Testing of Mixed Mode Sensor SOCs’

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June 4-7, 2017

Foreword

The purpose of this paper is to share a customer engagement experience in wafer probing mixed mode sensor SOCs' and related devices. The so-called "**pain points**" are test and product engineering related issues that could possibly affect productivity and end customer commitments.

These pain points and learning experiences candidly shared by a customer served as opportunities for innovation that were eventually converted to a core technology of a wafer probe system solution.

Outline

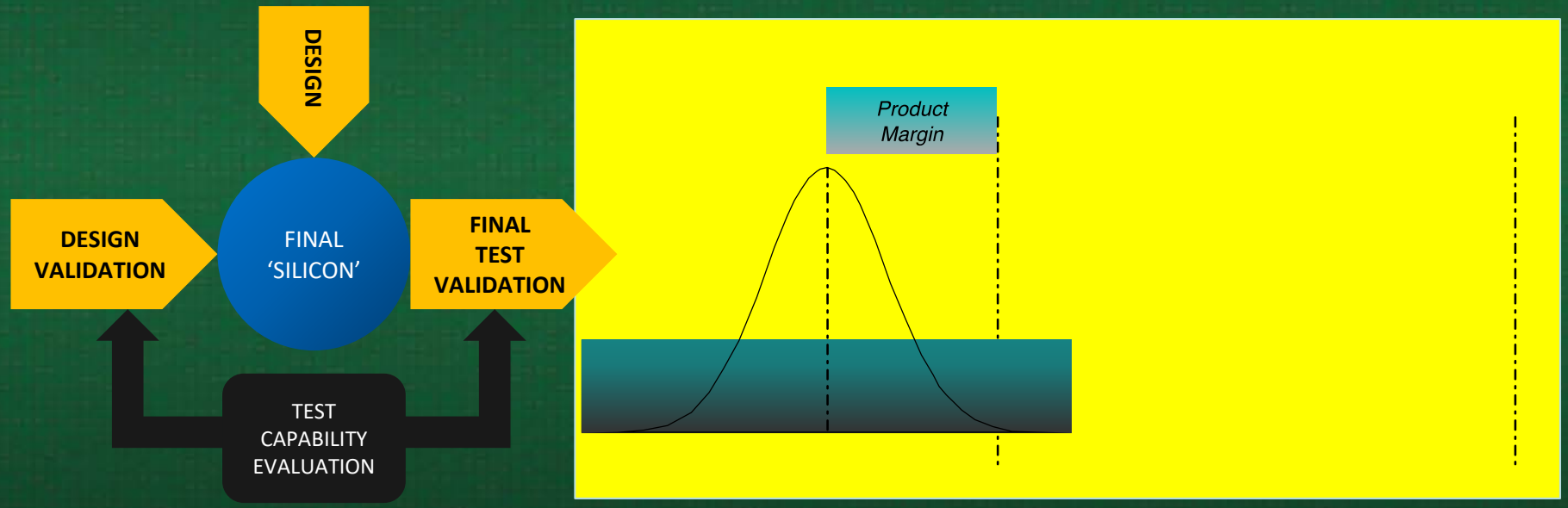
- Best Practices in Test & Product Engineering Revisited
- Sensor SOCs – Looking at the Critical Signal Path
- Customer Case Study – Dealing With Wafer Level Test Related Pain Points
- Comparative Results (Before and After)
- Lessons Learned

From Design-to-Final Test

Best Practices (that we know of)

Under “typical” conditions, we normally expect:

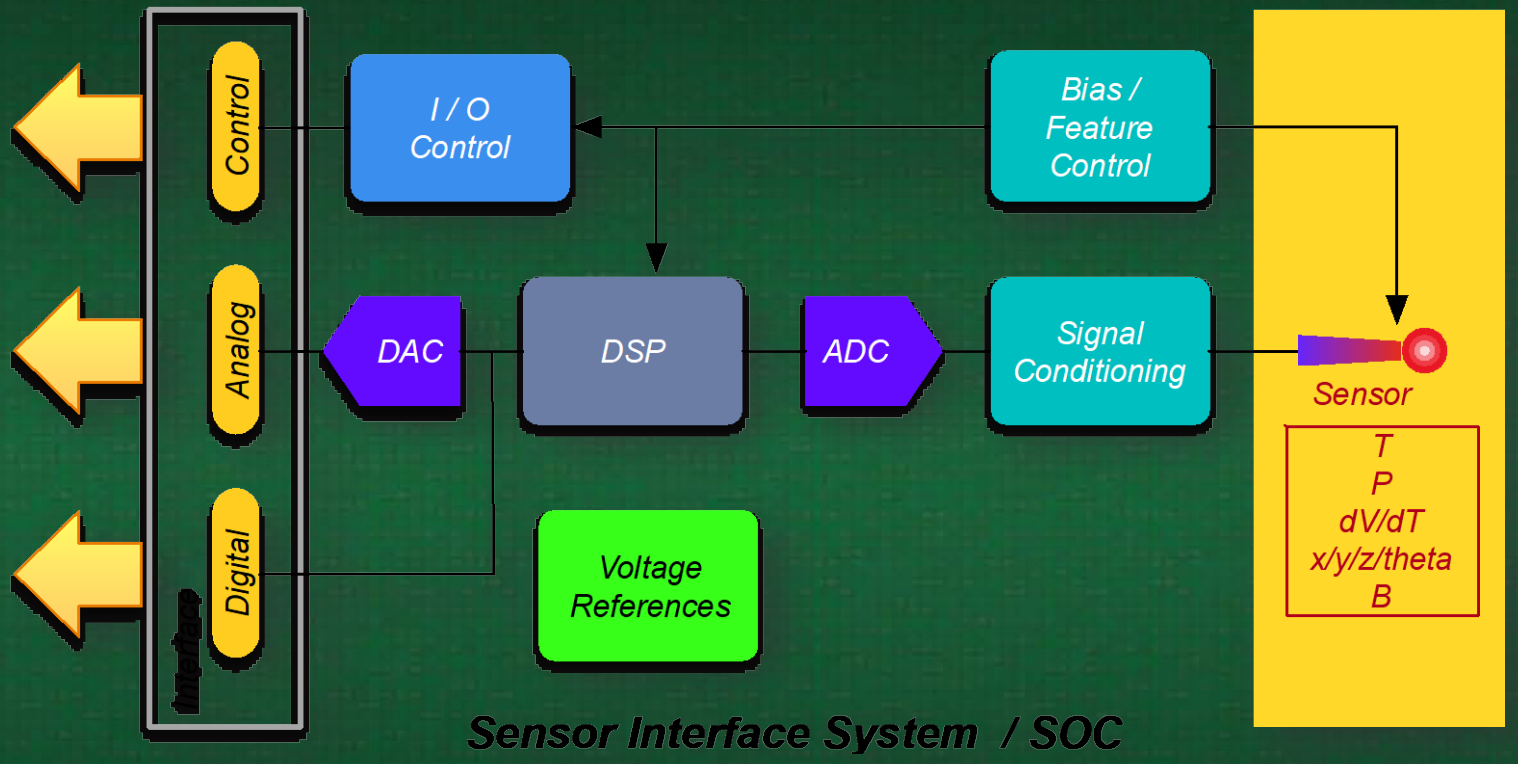
- A device performance distribution for each test parameter to set up test limits (Comfort Zone)
- Test capability evaluation to match test system against device observability requirements
- A guardband that provides the extra safety margin to ensure performance within the product specification



Graphics Reference: Sherry L. Read, Timothy Read, Statistical Issues in Setting Product Specifications, Hewlett-Packard Journal, June 1988

Mixed-Mode Sensor SOC System Block

A Generic Architecture

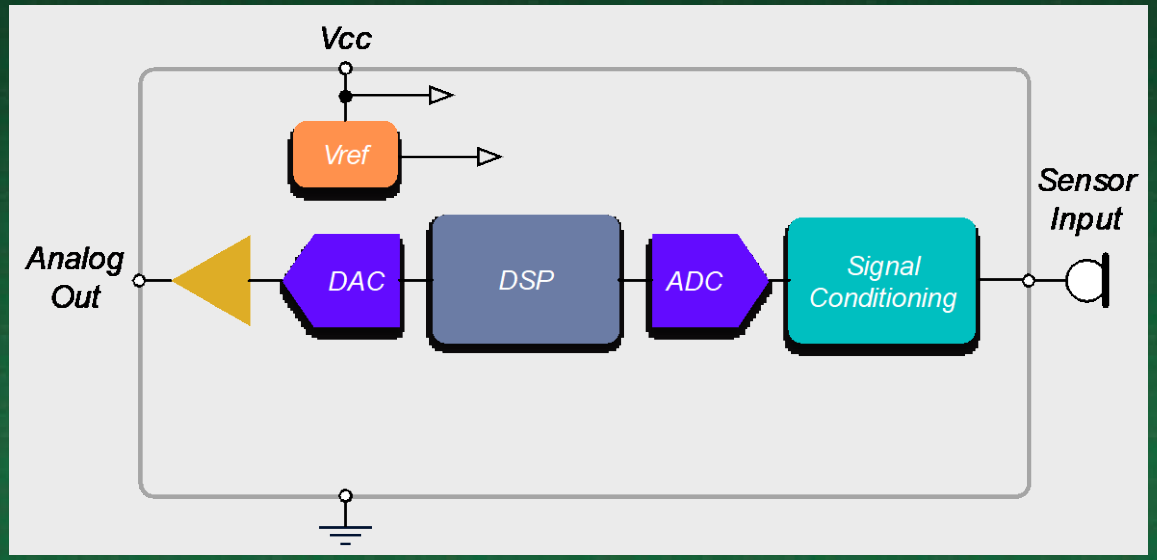


A Generic Sensor System SOC With Key Blocks:

- Sensor block (embedded or discrete), powered or self-powered through the SOC's bias/feature control
- Sensor signal path blocks from signal conditioning to final analog and/or digital outputs
- I/O control interface for sensor and signal processing
- Power management and voltage references (internal / external)

Customer Case Study

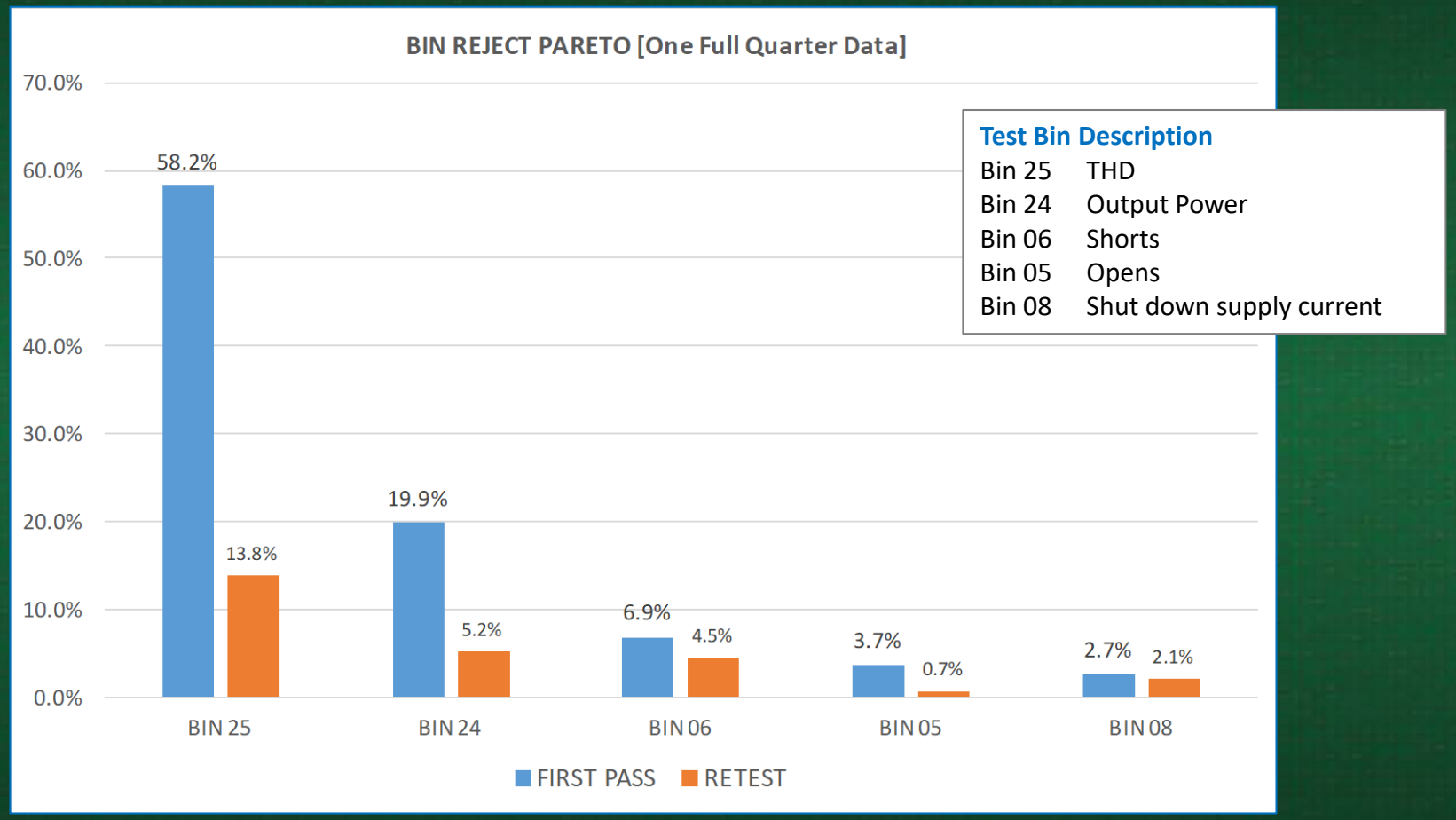
Sensor SOC Output Signal Path Yield Issues



Device Application:	Sensor SOC for portable medical and mobile wearables
Product Compliance:	Some end customer OEMs may be under regulatory compliance requirements
Product Package:	350µm pitch, WLCSP, final test for KGD
Process Node:	180nm BCD
Primary Pain Points:	Unacceptable (<90%) first pass yields, excessive retests for yield recovery
Secondary Pain Points:	Bump damage and package planarity issues post retest causing visual rejects
Wafer Probe Array:	Spring Pin type

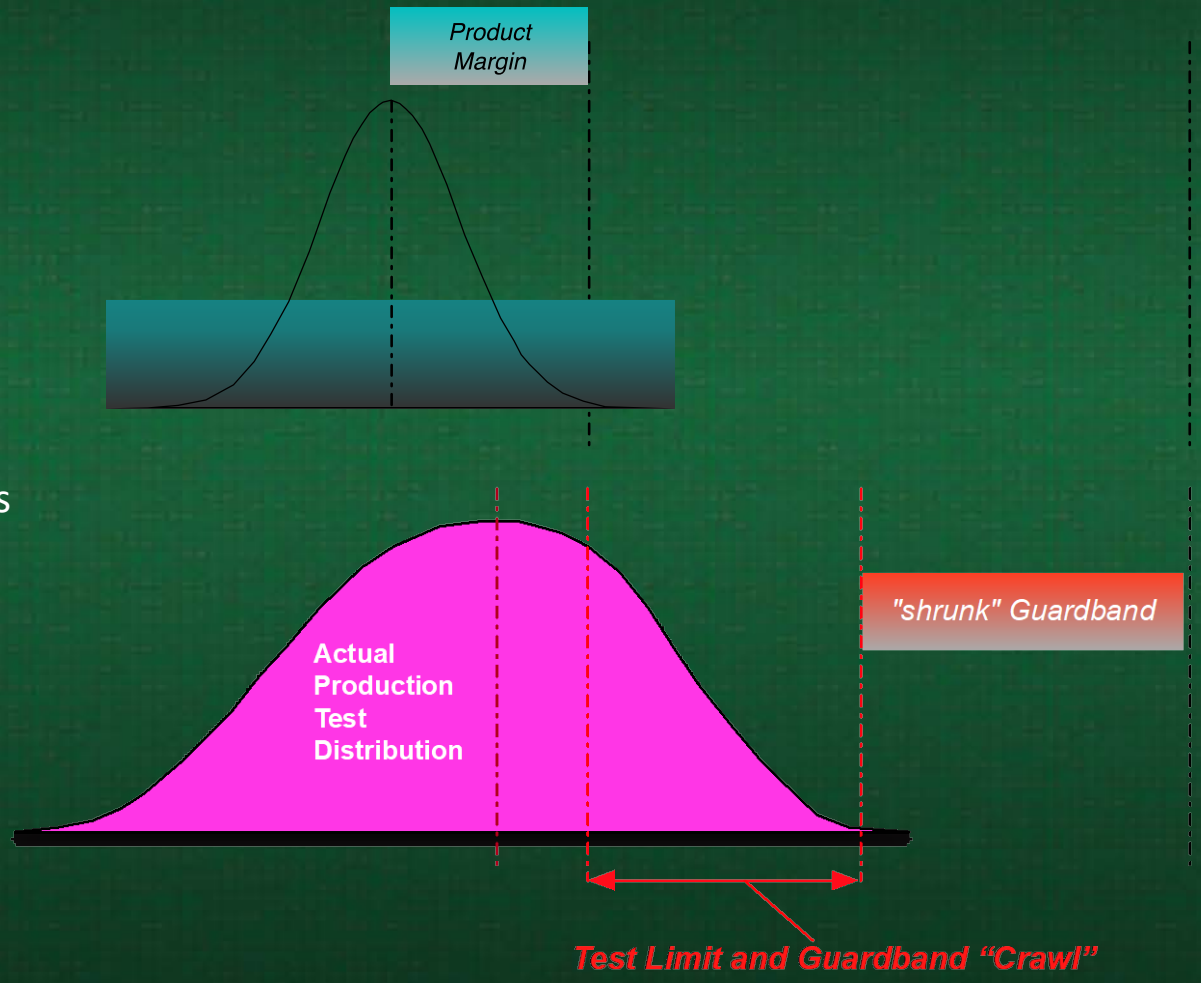
Customer Bin Reject Data

"Pain Point" in Graphics



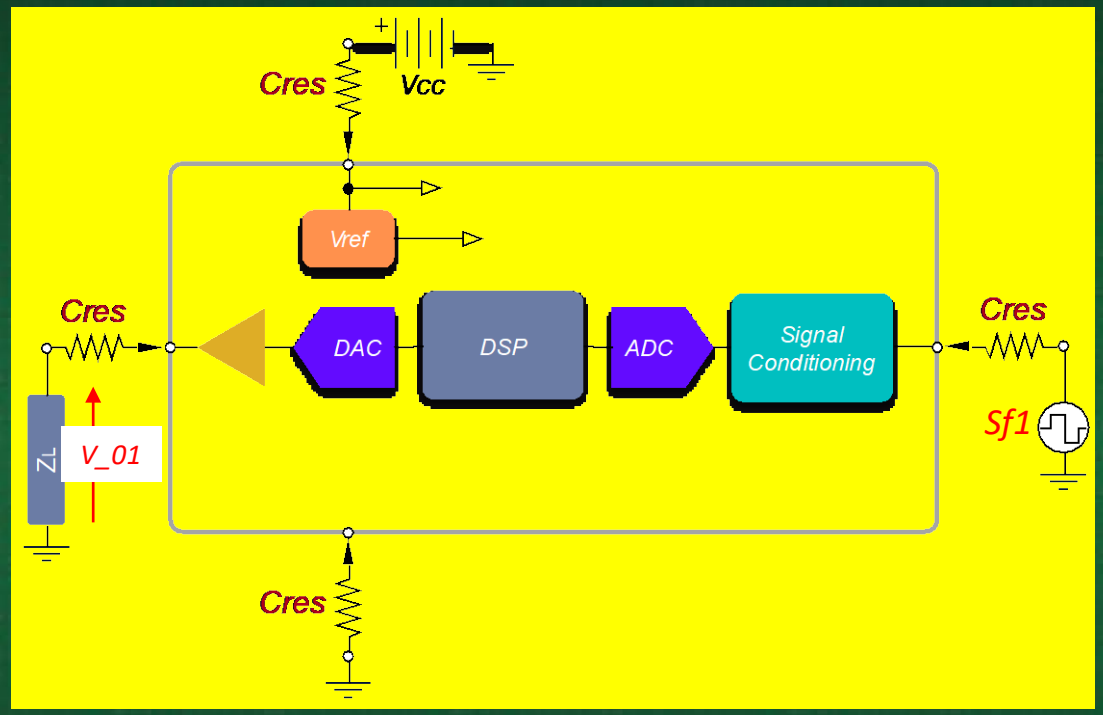
Primary Paint Point Realities

- Some key test parameters exhibit skewed and/or wider distributions
- Anomalous correlations between bench tests and wafer probe tests
- Adjustment of test limits to meet test environment encroach established guardbands
- Uncertainty in test capture confidence level

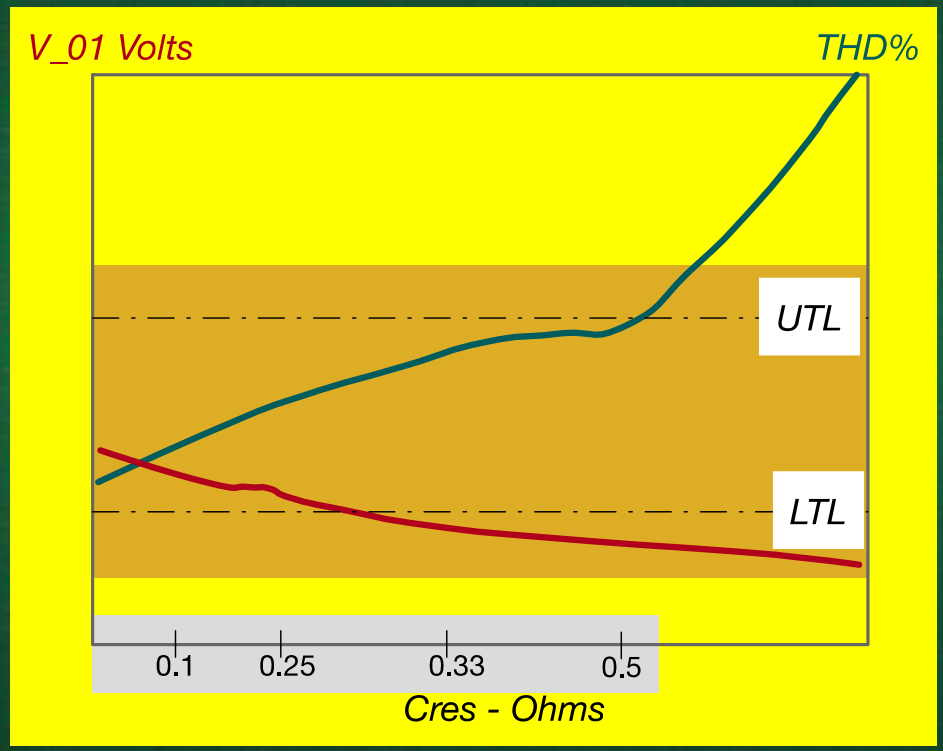


Customer's Fault Analysis

Cres Sensitivity Correlation (2nd Pain Point)



Test Performance Distribution Correlation Results



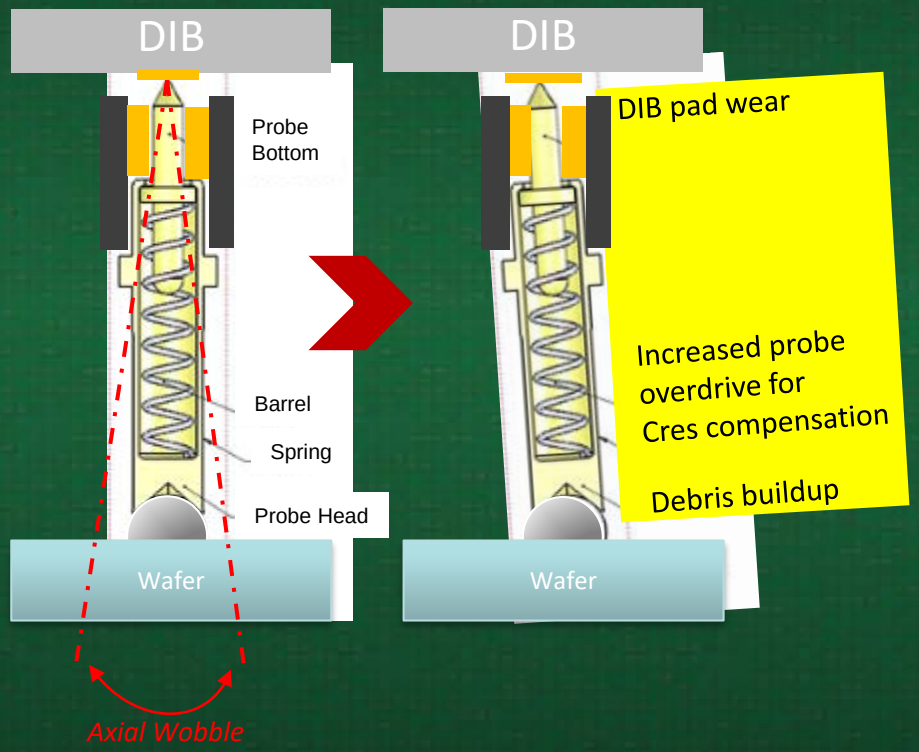
Significant Cres variance influence on

- Load, analog ground and supply impedances
- Vcc supply voltage
- SMU forcing function [Sf1]
- Measured voltages across Z_L
- The established UTL for THD and power output did not represent production predicted test distributions

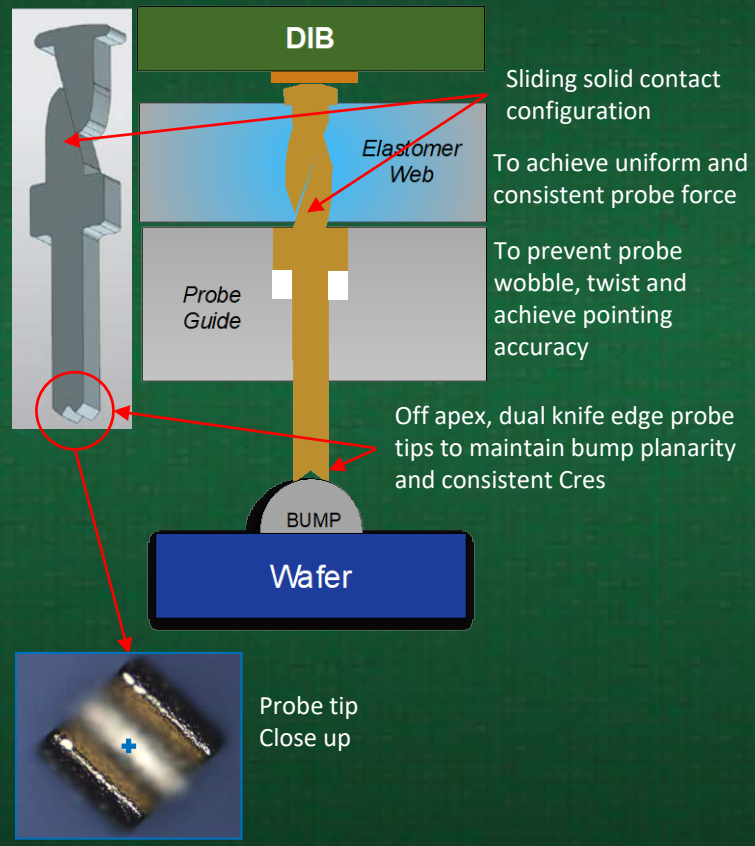
Customer Root Cause Analysis

Resulting Probe Array Solution Proposal

Incumbent Probe Array

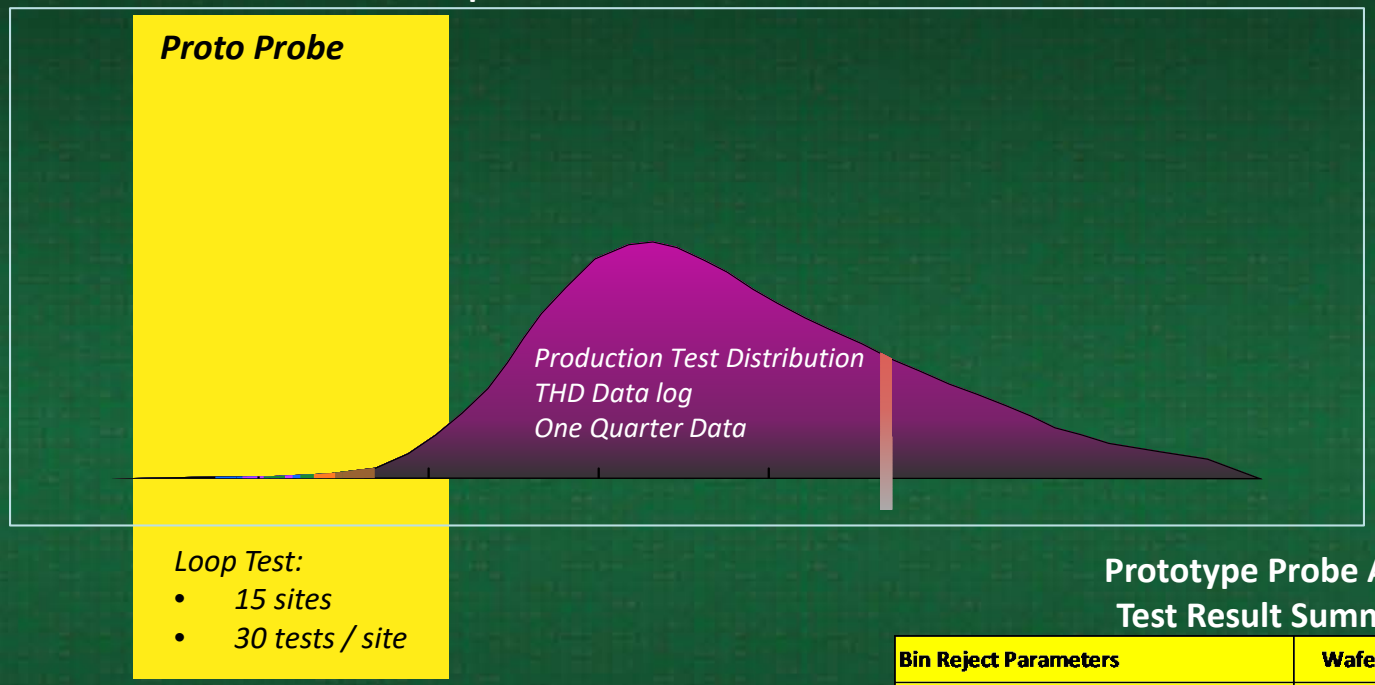


Proposed Probe Solution
Solid Contact Concept



New Probe Array Validation

Comparative THD Test Distribution



Notes:

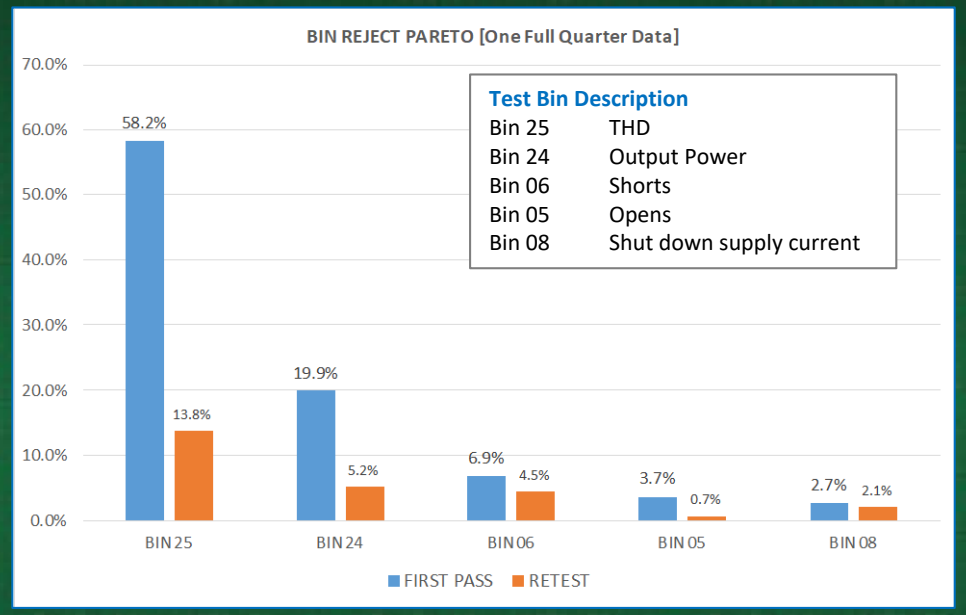
- Loop tests done prior to full wafer tests to validate initial Cres correlation
- 3 wafers from 3 different wafer lots
- No online cleaning during test (all 3 wafers)
- Historical first pass yield is 77% (1 quarter data)
- Zero retests using new proto probe array
- New THD Cpk is 4.5 (better than 6 sigma)

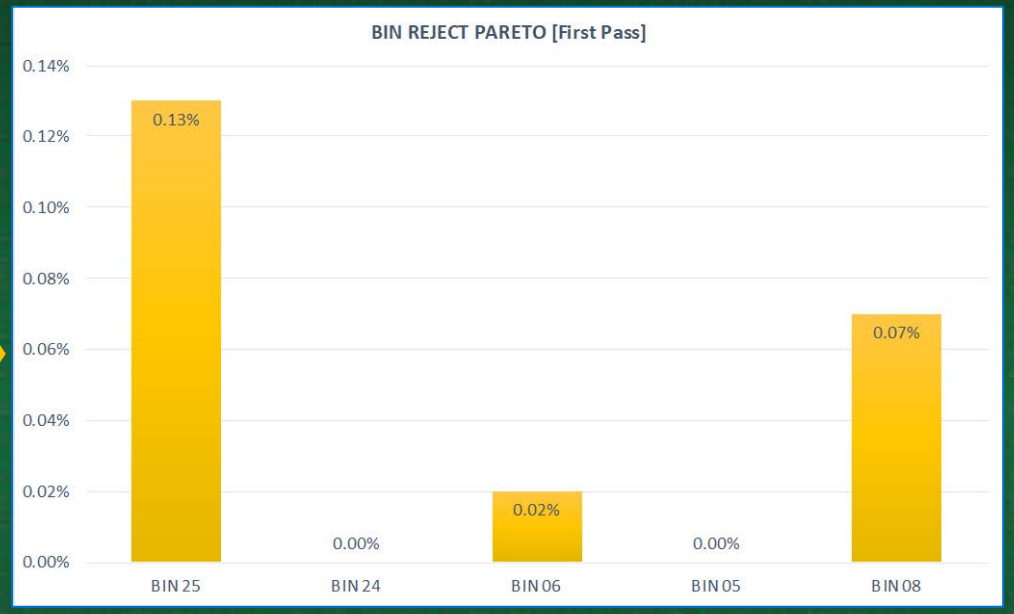
Prototype Probe Array Test Result Summary

Bin Reject Parameters	Wafer 1	Wafer 2	Wafer 3
First Pass Yield %	99.67	99.28	99.69
Opens [Bin 05] %	0.06	0.00	0.00
Shorts [Bin 06] %	0.08	0.07	0.06
Shutdown supply current [Bin 08]%	0.04	0.10	0.08
Output power [Bin 24] %	0.00	0.00	0.00
THD [Bin 25] %	0.00	0.41	0.06

Nine Months Later ….

First Full Production Run Using New Probe Array

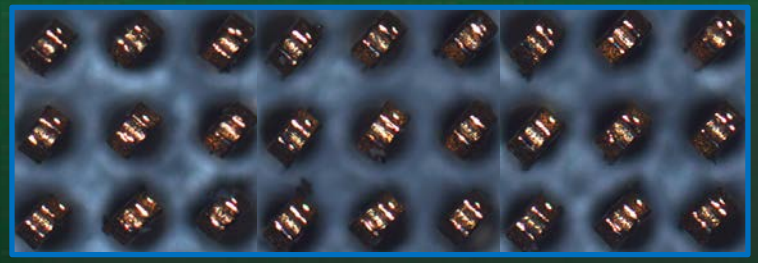




Production Run Notes:

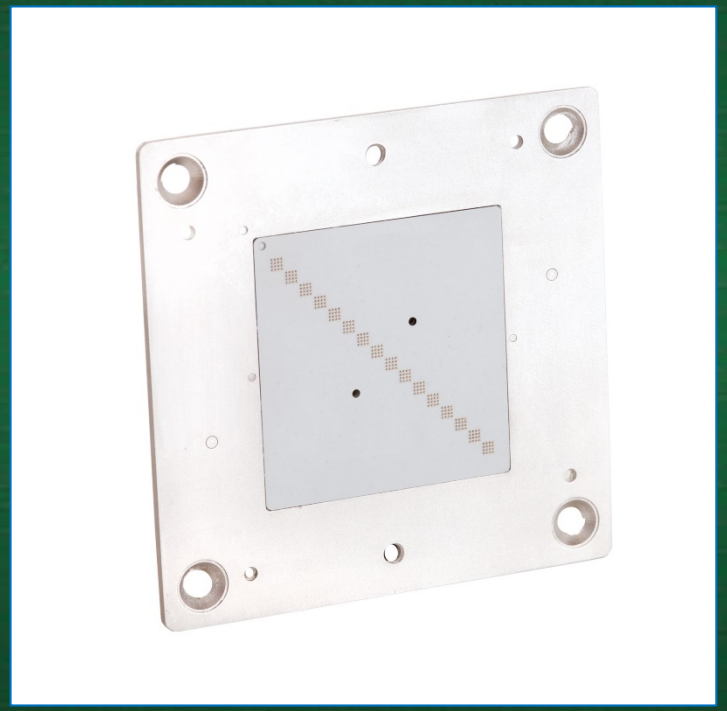
- Pre-production probe array released 9 months post prototype validation
- Shippable production wafers used for production test run
- Per customer shared data, OEE increased from 82.2% to 93.1% due to retest and maintenance interrupt reductions

Probe Tips at Various Sites in Array
37,012 Landings – No Online Clean Interrupts

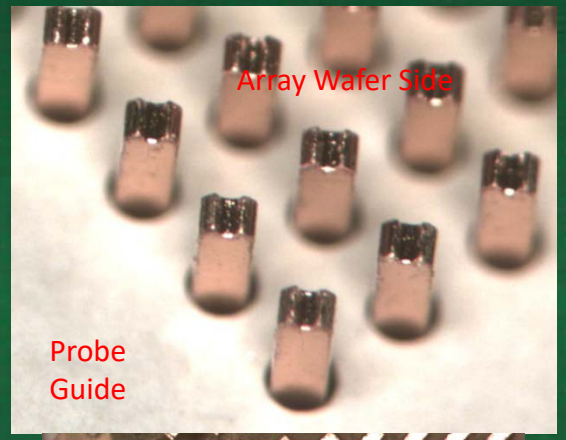


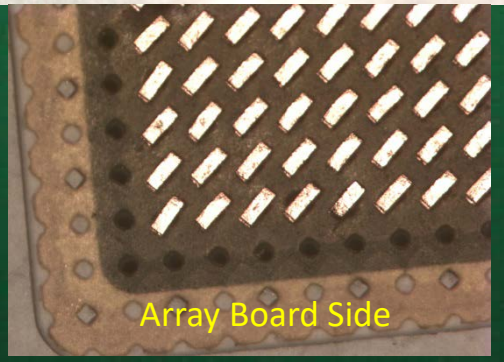
Probe Array – As it Looks Today

Complete 16-Site Probe Array
Wafer Side



Close Up Examples





Lessons Learned

- "Pain Points" can be converted as opportunities that generate innovative products and solutions
- Sometimes, implementing established good practices are not sufficient for successful product launches
- Candid and transparent supplier – customer collaborative partnerships provide valuable strategic leverage that are mutually beneficial