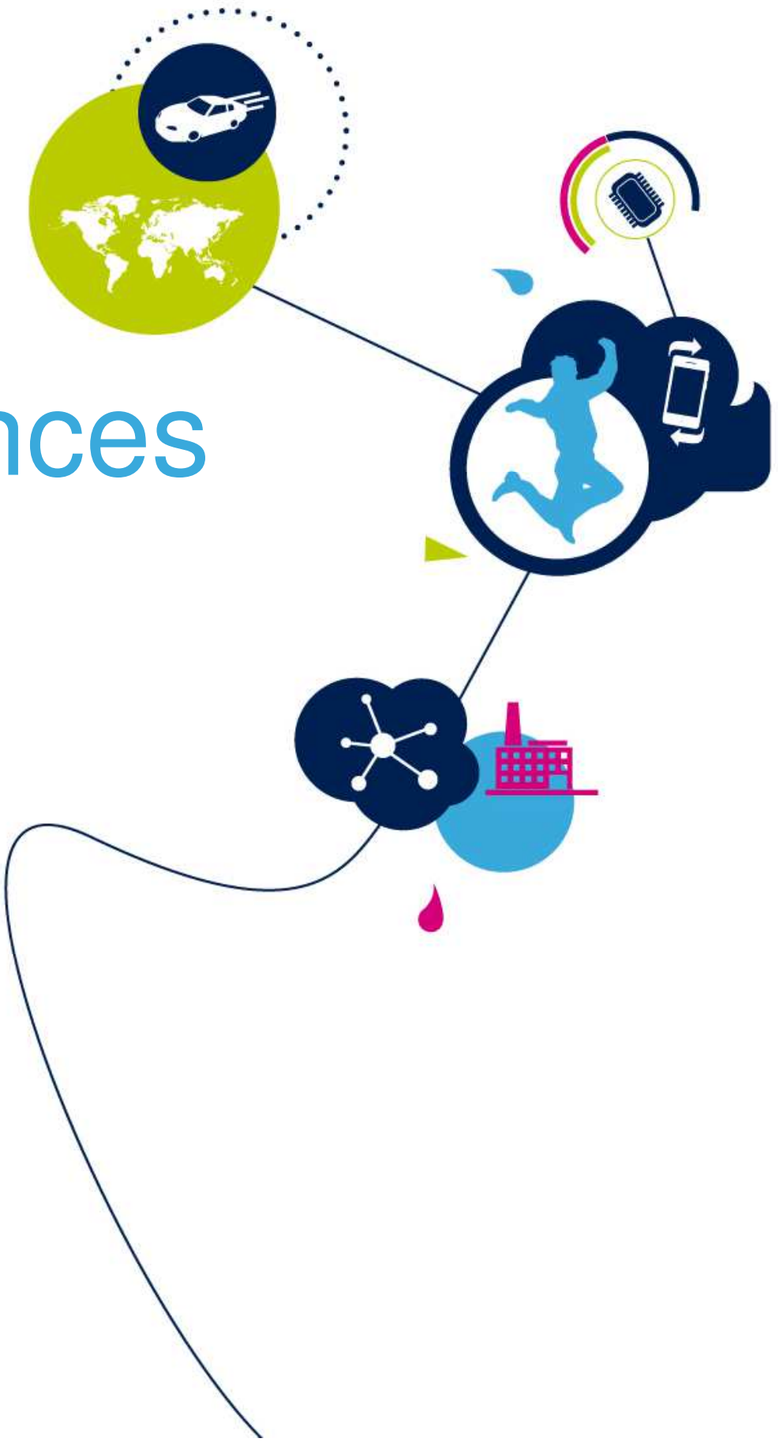
Automotive, the Roadmap of Technologies and their Influences on Testing



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Automotive & Discrete Group

STMicroelectronics

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Abstract

An apparently invisible revolution is crisscrossing the semiconductor industry developing components targeted to the automotive market. Until recent days, **this industry usually behaved unadventurously**, adopting technology and solution previously experimented by other industry applications. The sudden increase of the required performances pushed to the adoption of very advanced technology nodes.

We expect that all these will also have an impact on the methods and solutions applied during production test. The talk will develop some of the factors proposed in the remainder of this abstract together with other elements.

A very popular topic is **functional safety (FuSa)** whose requirements are nowadays pervading the majority of new designs. FuSa is indeed an innovative element of our industry essential to the actual development of autonomous driving. It is already a consolidated solution present in many safety applications including for example braking, steering and passive safety devices. Test engineer welcomed the introduction of FuSa. Many advanced testability features became part of the functionalities offered to the customer and therefore no more seen as overhead for the SoC implementation. Nonetheless, other criticalities and additional factors are present.

Two additional key factors, though not orthogonal each other, might drive changes to the traditional test practices:

- **The correlation of performances between functional activation and test is progressively loosening**
- Parametric variations linked with new advanced technologies like FdSOI and FinFET are breaching typical test paradigm (e.g. divide and conquer or implication test)

Finally, we shall concentrate on the role and the weight of assembly technologies. The complexity of packages needed by high-power digital SoC is huge if compared with consolidated packages used in automotive like QFPs. A combination of reliability pitfalls is implicit with **advanced packages** because of the mix of materials, processing technologies, mechanical and thermal factors they are featuring.

These are samples of the signs arising from the **quiet revolution running** in our SoCs for automotive, which will be further discussed along with possible implications with usual test steps at wafer, package and system level.

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Outline

- STMicroelectronics introduction
  - Business data and products

  Digital products
  - Smart driving, autonomous driving, safety, connected vehicles
  - Architectures, relevance of data processing
  - Automotive transformation

  News

- Automotive roadmap
  - Impact on testing technologies: overview
  - Effects on front-end testing
  - Effects on back-end testing
  - Equipment, DFT and testing flows

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STMicroelectronics

- Among the world's largest semiconductor companies
- Serving over **100,000** customers across the globe
- 2018 revenues of **$9.66B,** with year-on-year growth of **15.8%**
- Listed: NYSE, Euronext Paris and Borsa Italiana, Milan
- Signatory of the United Nations Global Compact (UNGC), Member of the Responsible Business Alliance (RBA)

- **~46,000** employees worldwide
- **~ 7,400** people working in R&D
- **11** manufacturing sites
- Over **80** sales & marketing offices

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As of December 31, 2018

Automotive	Industrial	Personal Electronics	Communications Equipment, Computers & Peripherals

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Automotive and Technologies Trends

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Automotive Smart Driving

Megatrend Convergence

Electric Vehicles

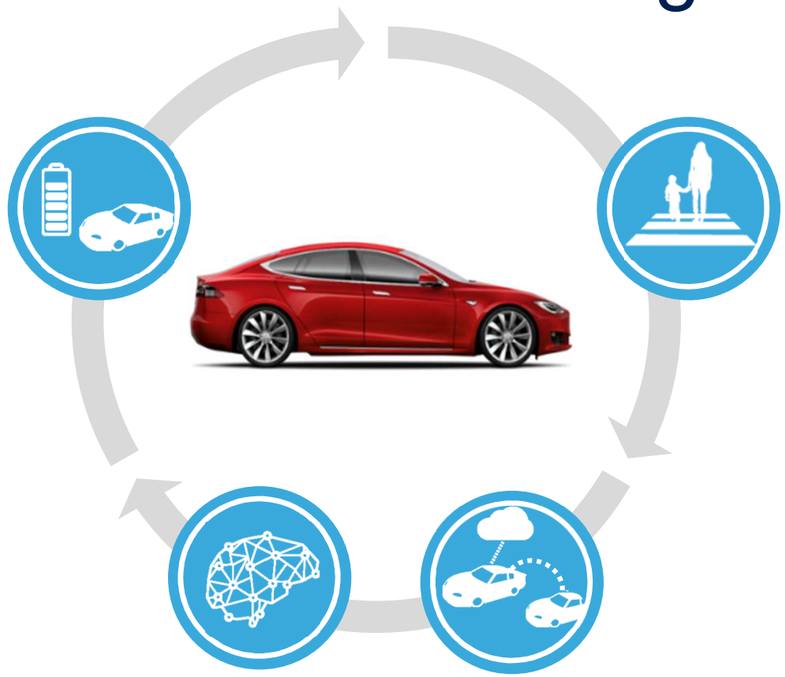
10cent/Km as mobility cost target

40% Electrified Vehicles by 2021

-35% CO2 by 2030

Zero Emission by 2040 in City
Zero Net Emission by 2050

Multiple vehicle configurations to support multiple mobility needs (Hybrid, Plug in, Electric, Fuel cells…)



Connected, Assisted, Autonomous

Zero accident risk by 2050

2050 mobility target: 90% of population vs. today 60% due to assisted vehicles

Supporting shared mobility by 2030 with one car in ten shared

Cheaper mobility proliferation with “Robo-taxis”

New Digital Architecture to Enable Software Reconfigurable vehicles

Data enabled services are estimated to provide ~30% of Car Makers revenues by 2030

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Data Enabled Services

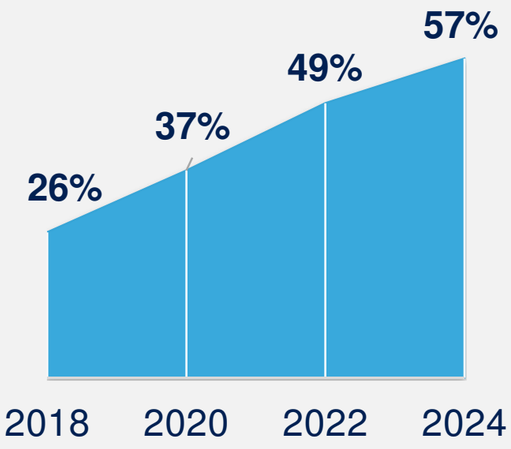
Shared Mobility

Active Safety and Autonomous Driving

Several Developments to Increase ST Silicon Content in ADAS Systems

ADAS Market Acceleration

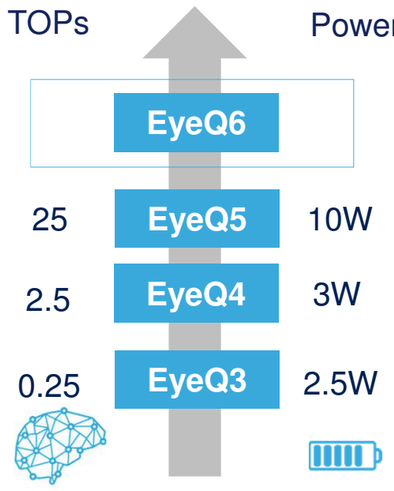
ADAS System Penetration in Car Production



$350 Average ADAS Content per Car **$900**

Level 2+ → **Level 4+**

Leading Vision-based system with Mobileye



MOBILEYE An Intel Company

78#
2018 New Car Models Launched

32M
EyeQ System delivered by Mobileye to WW OEMs

EyeQ5

- 1st product designed for automotive in 7 nm FinFET suitable for both ADAS and autonomous driving market
- Functional samples delivered to customer in Dec 2018
- High volume business already acquired with car makers

Moving forward to autonomous vehicle with Auto-parking ability

Panasonic

- Advanced solution for mobility and autonomous parking
- Co-development leveraging ST expertise in designing safe and secure automotive SoCs and Panasonic leadership in image manipulation and system design
- 16 nm technology samples delivered

Source: Strategy Analytics Automotive Electronics System Demand Forecast, ST Internal

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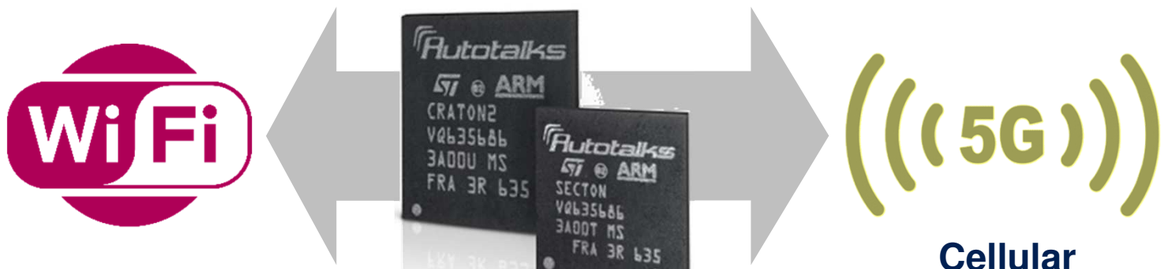
Connecting Vehicles

From Wi-Fi-based V2X to Dual Mode Wi-Fi & 5G -V2X

Market 1st dual-mode V2X solution to enable multi-standard connectivity



Wi-Fi 11.p
(for Automotive)

Cellular
(Automotive low latency 5G)

Market success of the partnership

Autotalks solution awarded for mass-production:

- 4 of the top 10 automakers plan to deploy our V2X solution
- Over 10 Tier1s awarded the chipset
- Start of Production by 2020

BOSCH DENSO HARMAN Valeo

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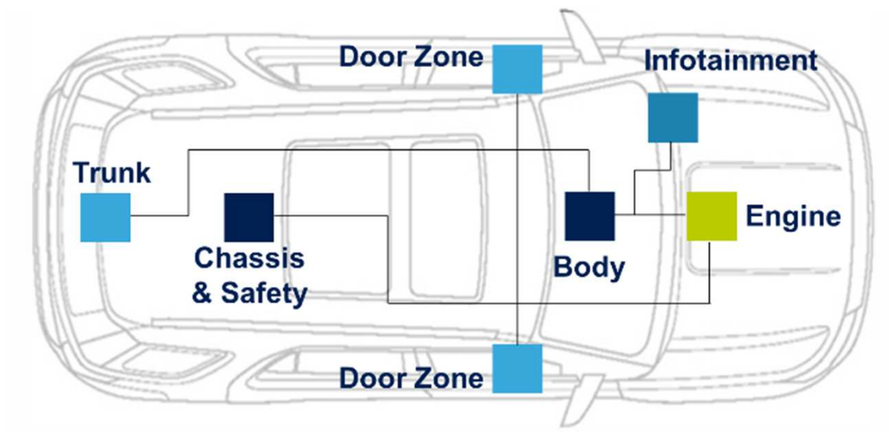
Car Digitalization: New Architectures

…Software Accounting for 30% of Vehicle Value by 2030

ST Technology enablers: FD-SOI 28nm with embedded Phase-Change Memory (PCM)

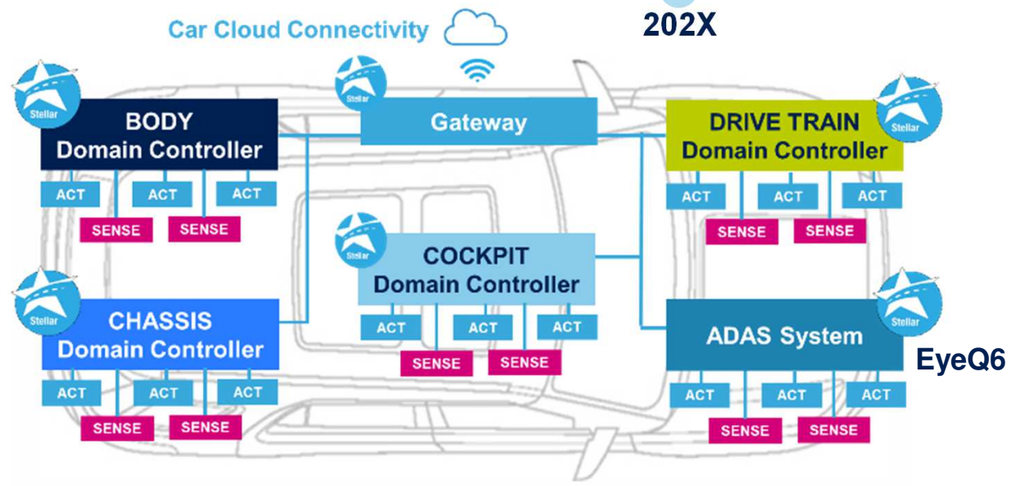
2017



x10

Car Computational Power

202X



Distributed Architecture: 9k DMIPs per Car

- Local Control Units with up to **130 ECUs/Car** (with 8-16-32-bit MCUs)
- Limited connectivity and in-vehicle data-flow (up to 10 Mbit/s)
- Heavy and expensive harness
- Extremely complex car Software management
- No car functionalities upgrade

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STM8 A

SPC5

Integrated Real-time Domain Architecture: 90kDMIPs per Car

- ~5 Domain-Control Units with higher power computation
  - **Stellar** with multiple Arm® Cortex®-R52 cores embedded Phase-Change Memory (PCM)
- Autonomous Driving Super-computer (MPU ext. Memory) ~**100 Trillion Operations per second**
- Architecture simplification, SW rationalization, harness drastic reduction
- Easy car functionality reconfiguration and SW upgrades
- High-speed in-vehicle communication
- Over-the-Air Software upgrade capability

SPC5

Stellar

Data Harvesting in Automotive

Vehicle sensors for assisted driving

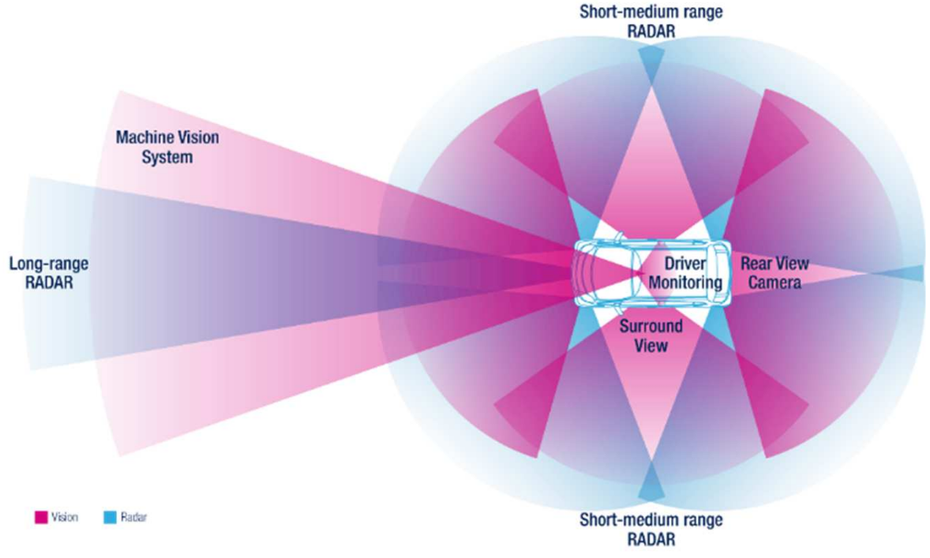
- High-definition cameras
- High-precision positioning
- Long-range Radar
- Time-of-Flight Lidar
- Vehicle dynamics gyroscope & accelerometers

What latest semiconductor sensor technology nodes bring

- Higher accuracy in sensing
- New sensor type capability at acceptable cost
- Higher performance

High performance digital processors with AI accelerators enable metadata extraction from raw data

To reduce data to transferred and make continuous streaming cost efficient



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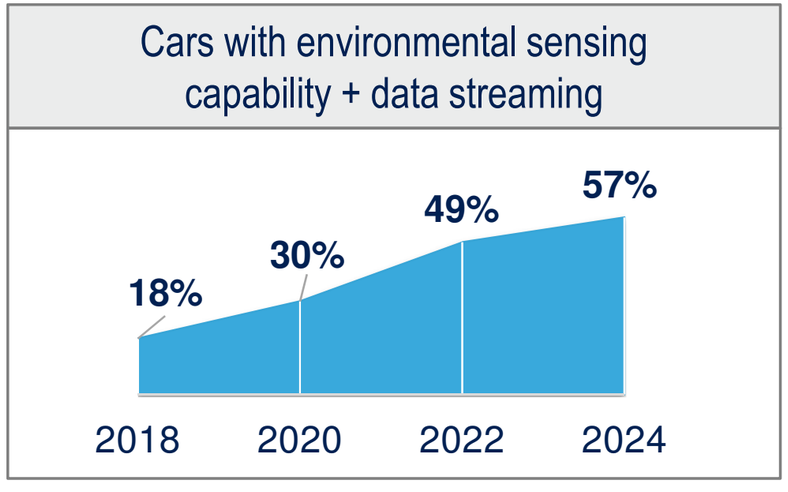


(*) Strategy Analytics, internal data

Automotive Transformation

Environmental Transformation

17% Transportation Emission vs. Total **24%**

1995 → 2018

-90% Noise Reduction since 1970

-36% C02 Emission since 1995

-90% NOx Emission since 1995

Architectural Transformation

~30 Average ECUs per Car **>100**

1995 → 2018

~100M Lines of Code in latest vehicle generation → **x15** latest-gen commercial airplane

50% 2016 ADAS Program vs. Total Automotive Market R&D Investments

Business Model Transformation

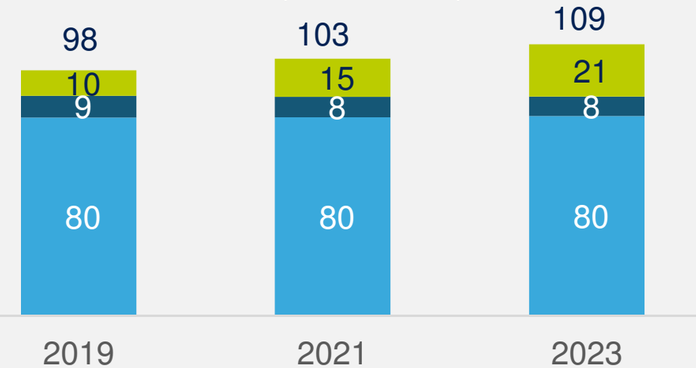
$8B Automotive Semiconductor Sales **$38B**

1995 → 2018

>$100B Investment in Mobility start-ups since 2010 → **94%** from Non-Automotive Industry

Worldwide Car Production

(Million units)

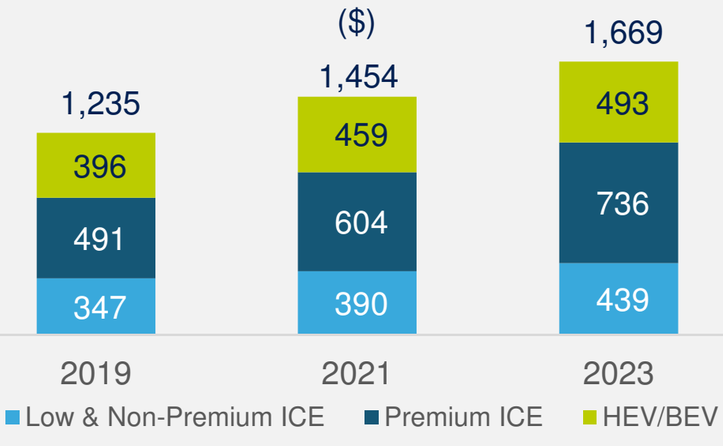


Content evolution driven by

- Electrified car volumes (24% CAGR)
- ADAS (16% CAGR)

Auto Silicon Content Evolution

($)



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Source: Automotive news, McKinsey center of future mobility, Strategy Analytics, ST Internal

ADG Automotive Business Evolution

Digitalization & Electrification Driving ADG Growth

ADG Automotive Revenues:
2.5B$ FY'18

~30%
Digitalization & Electrification

~70%
Traditional Automotive Core Electronics

Car Electrification

ADAS Vision

Networking

ADAS Radar

Positioning & Connectivity

Engine Control

Safety

Body & Convenience

Car Audio

~50%
Digitalization & Electrification

~50%
Traditional Automotive Core Electronics

Today

In 5 Years

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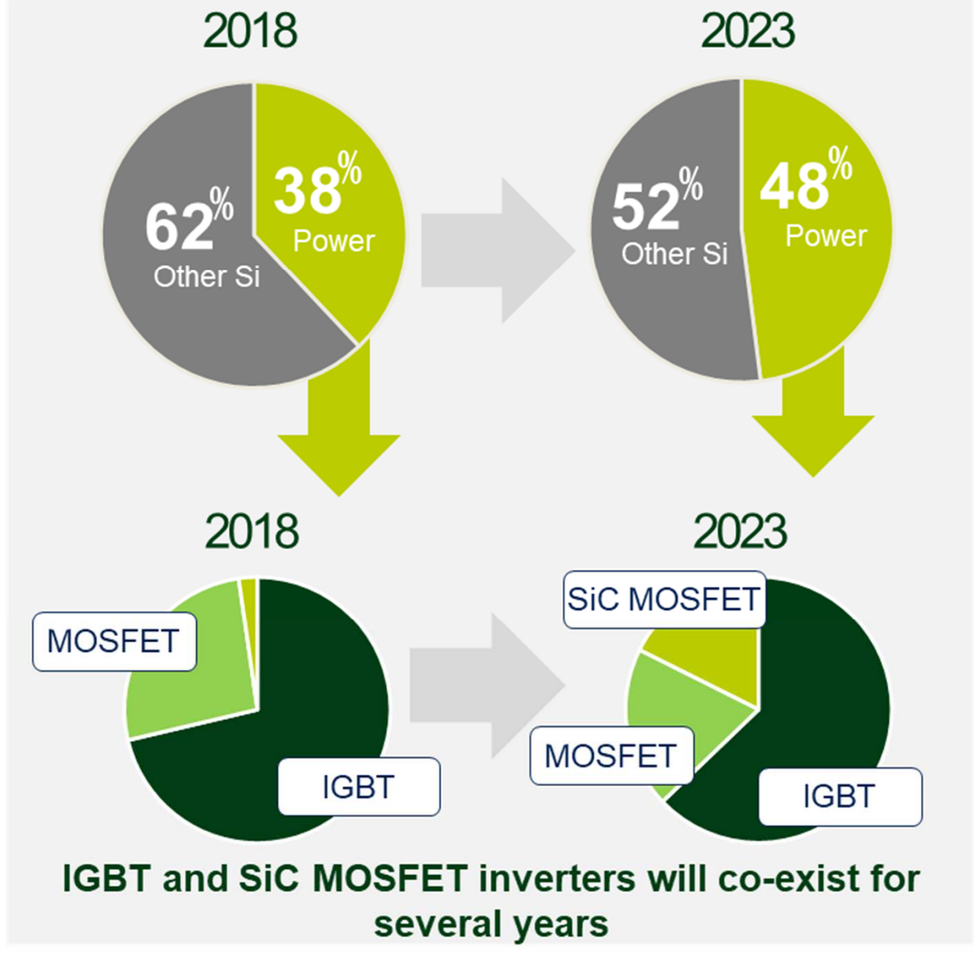
Car Electrification Boosts Power Content

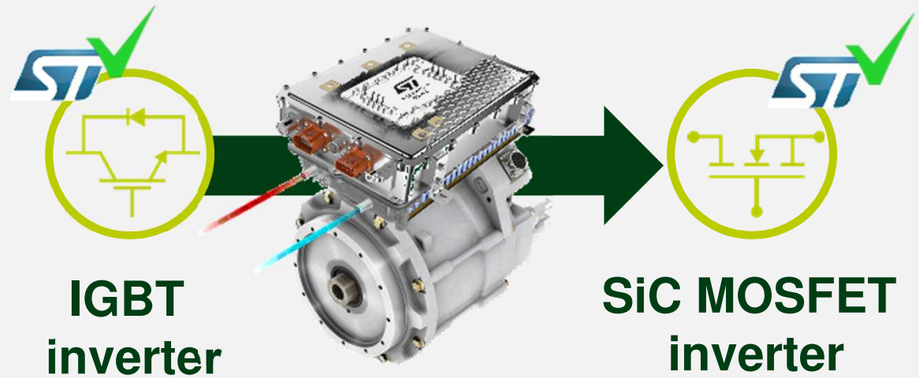
Powertrain TAM Evolution



IGBT and SiC MOSFET inverters will co-exist for several years

SiC MOSFET Vs. IGBT Advantages in Traction Inverter

Electric car motor and inverter



- 80% switching loss saving
- Direct inverter integration
- No separate liquid cooling
- Better thermal management
- Faster charging time

Potential saving thanks to SiC MOSFET usage in electric car

+300 $
Sic MOSFET Additional Cost (*)

~2000 $
Estimated Saving (*)

SiC MOSFET market size **by 2030** estimated to be **> 10B$**
representing ~**50% of the incremental growth** of power semiconductor in 2019~2030

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ST has the full technology and product offer to support the two solutions

(*) Source: Goldman Sachs

ST Silicon Carbide

In Line with our Target of >30% Market Share by 2025

Silicon Carbide: Business Status

>$100M
SiC MOSFETS /Diodes Revenues in 2018

>$200M
2019 Projection

#1 WW **Automotive** Supplier with SiC MOSFETs

Awards rate acceleration: More than **20 Car Makers** engaged

>10# OEM in production with ST SiC MOSFET

8 European Car-Makers ramping-up by 2019-20

RENAULT NISSAN MITSUBISHI

Partnering with **Renault Nissan Mitsubishi** on several SiC projects

HYUNDAI

Cooperating with **Hyundai Kia Motor** on several **SiC** MOSFET & Diodes

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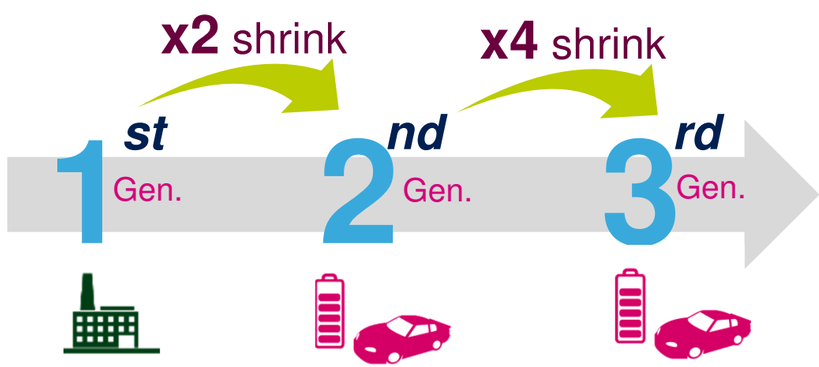
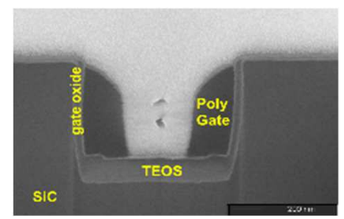
ST Strategy and Execution



Next Gen



Trench Technology

SiC Supply Chain
Vertical Integration Norstel AB

ST acquired majority stake to secure **Internal Supply** for SiC wafer substrates

Extended and **Secured** Supply Chain capability through Multi-Year supply agreement with **Cree-Wolfspeed**

Power Modules

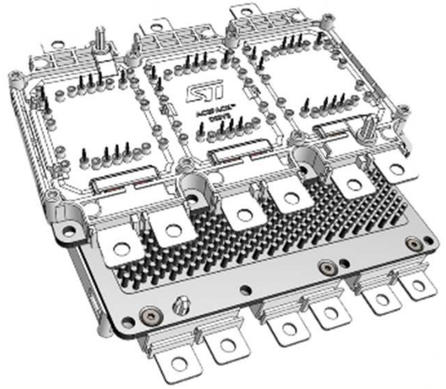
Standard & Custom Solutions Targeting Market Leadership

Broad range Module Portfolio

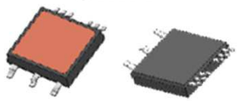
STPAK™

ACEPACK™ 1

ACEPACK™ DRIVE

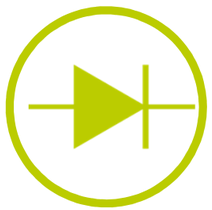


ACEPACK™ SMIT

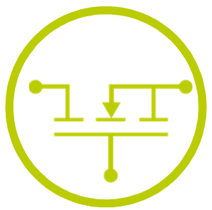


ACEPACK™ 2

Silicon and SiC Technologies Portfolio



Si & SiC Diodes

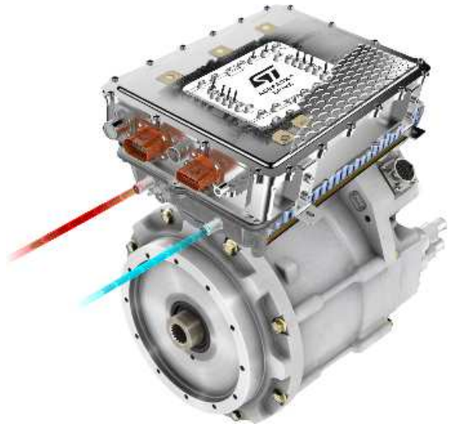


Si & SiC MOSFET

IGBT

Smart Power

Standard & Custom System Solution

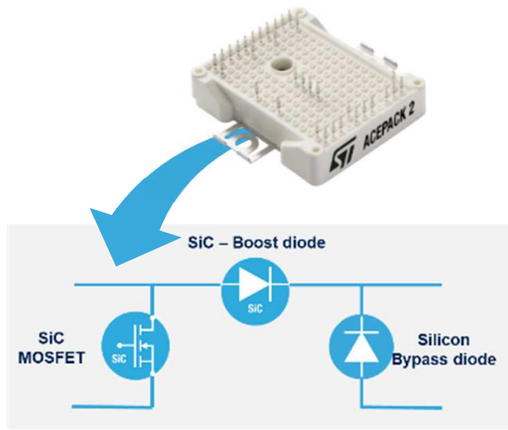


STANDARD Portfolio

Plug&Play Module for Traction inverter, On-Board Charger and DC-DC converter

CUSTOM Solutions

Combining semiconductor and package technologies addressing multiple design topologies tailored to specific customer needs



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Testing technology:
Key factors from the roadmap

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Key Factors

- Functional Safety
- Security
- Increased silicon content
  - Few premium ASP devices
- Access to very advanced technologies
  - FinFet, PCM, advanced packaging
- High-speed interfaces and RF integration in SoC/SiP

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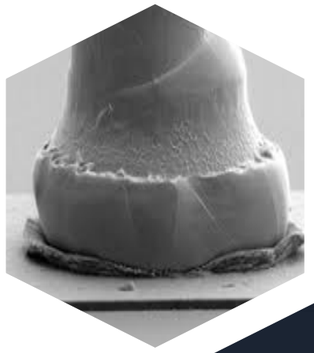
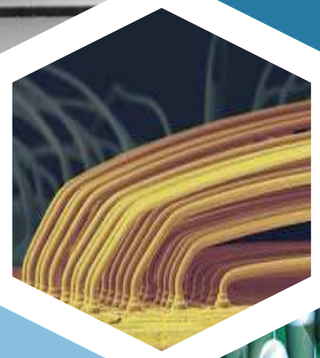
FE and BE

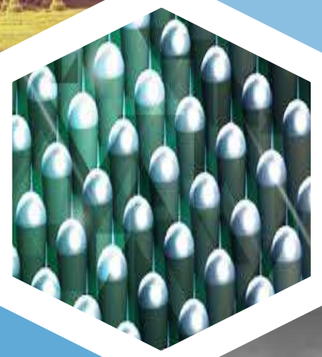


Wide temperature range
Large probed area
Small pad opening
Small pitch



Bonding complexity, electrical detectability of multiple wires,

High temperature, pad damaging, multiple touch, high-parallelism



Reliability of bump/substrate joint, material stack stability, warpage effects on large packages, white bumps

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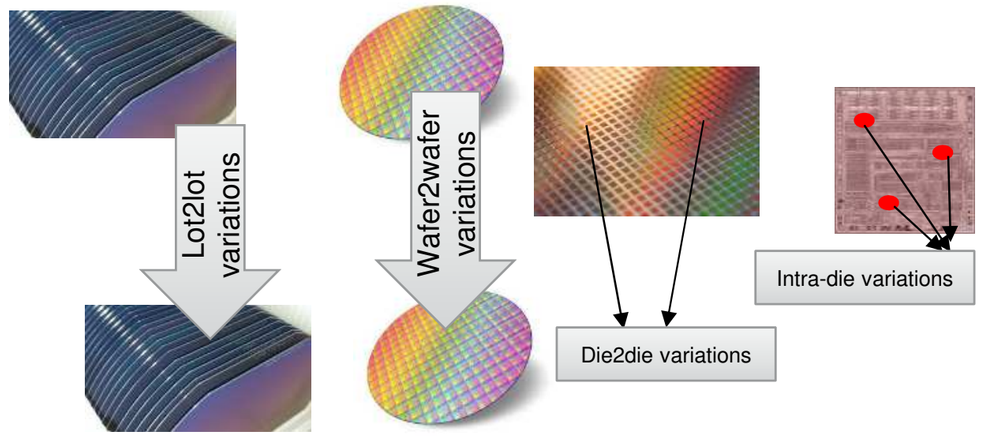
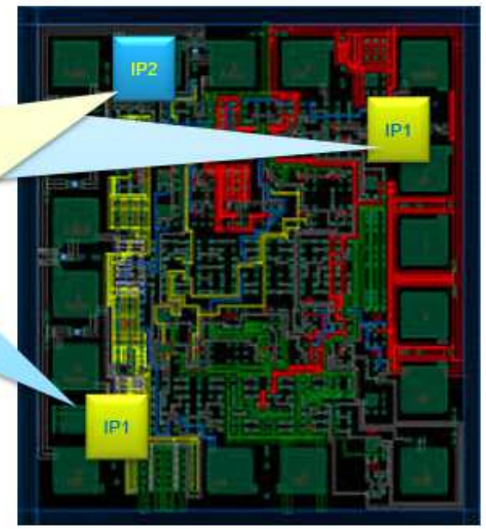
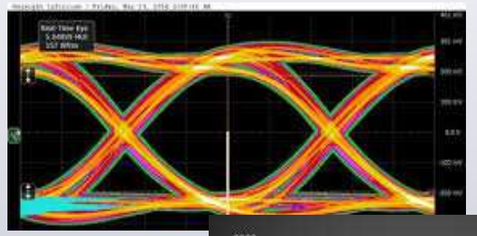
Electrical

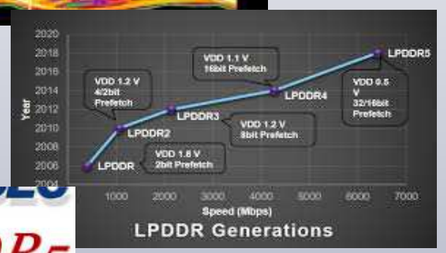


- Interaction performances between IP1 and IP2 may be un-predictably modulated in some PVT spots
- Performances of two IP1 instances in the SoC might be anomalously modulated by intra-die variations



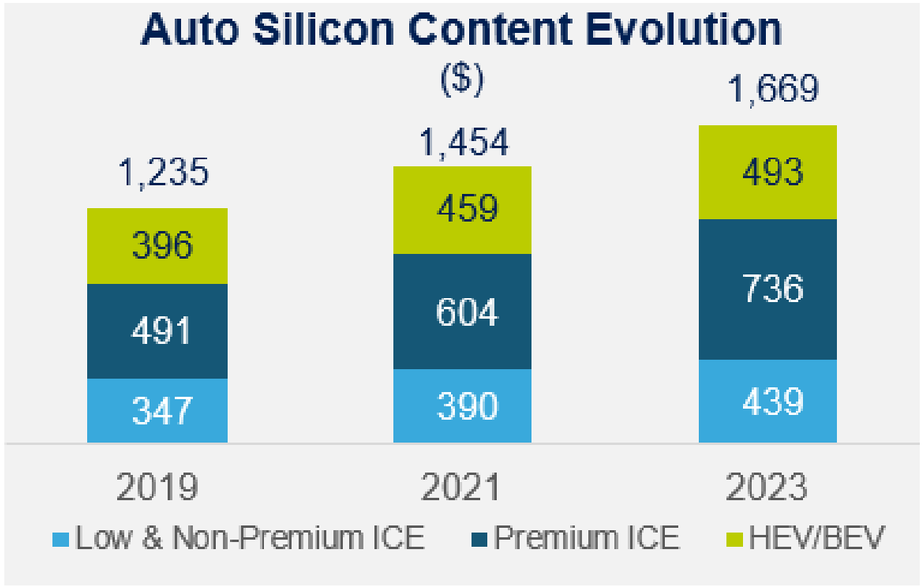
Performances





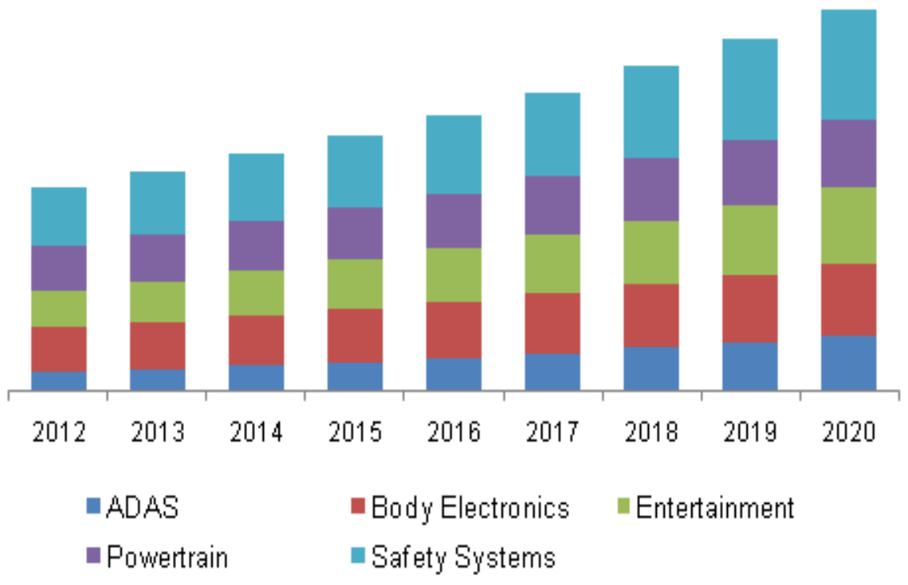
DDR5

Economical



MIND THE GAP

Between Functional and Structural



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Quality

Extended Quality Paradigm

- The level interaction between ICs of the same ecosystem increases the quality and safety challenges
- Key elements: IC level, system level diagnostic and software

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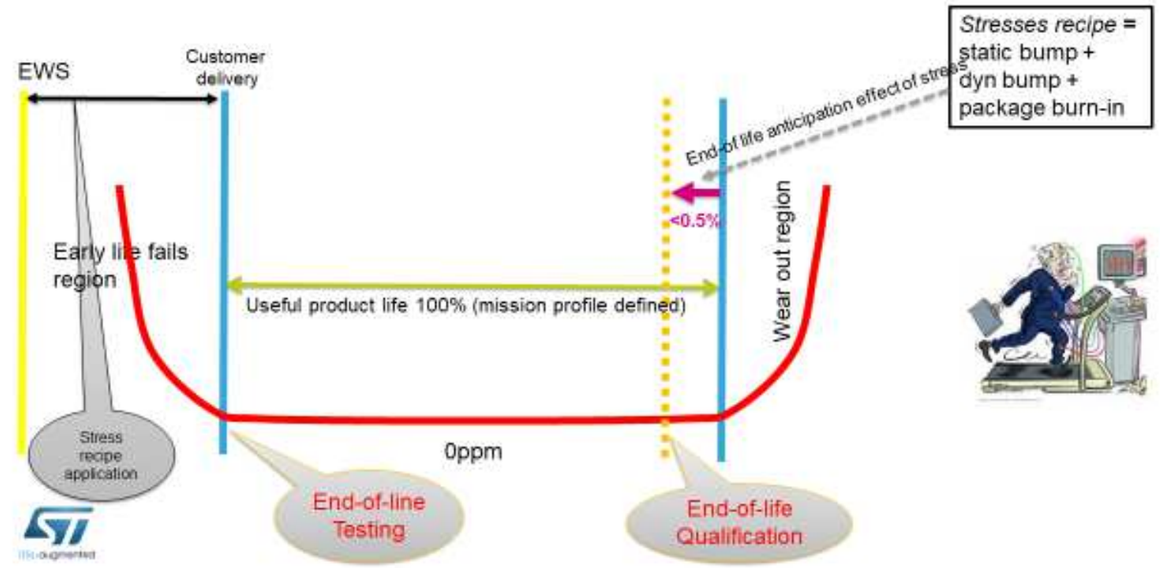
Reliability

Qualifying Stress Tests



Challenges:

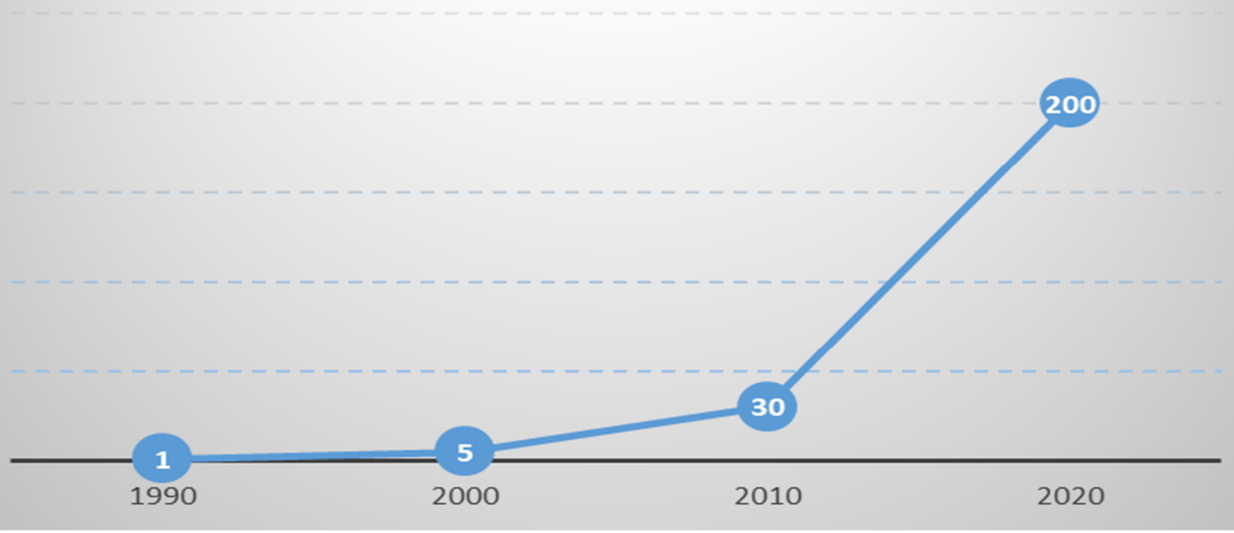
- Progressive relative reduction of overvoltage allowing device functionality along with lithography reduction
- Complex evaluation of effects across PVT
- Early life fail assessment

Factors Trend

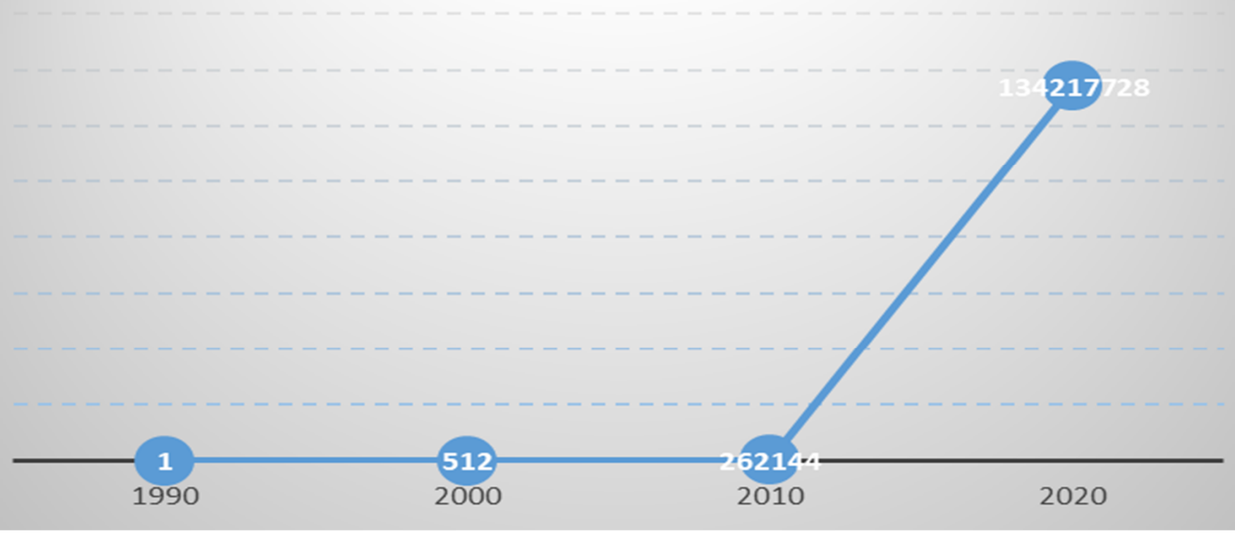
Contacting force, per device [Kg]

Power Integrity Sensitivity - QUALITATIVE

Speed, performances - QUALITATIVE



Density



Key factors

Impacts examples

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Impact on front-end probe

Factors

Fine pitch & Small landing pads/bumps	Large dies & high pad/bump count per die	Temperature range	Long test time → High test parallelism → Large wafer surface per probe step

Impact

Heavy contact force	Probe marks shifts across temperature range, emphasized on probe head corners	Cost and efficiency

Countermeasures

Dedicated PC by temperature	Increase soaking times	Additional metrology and analytics

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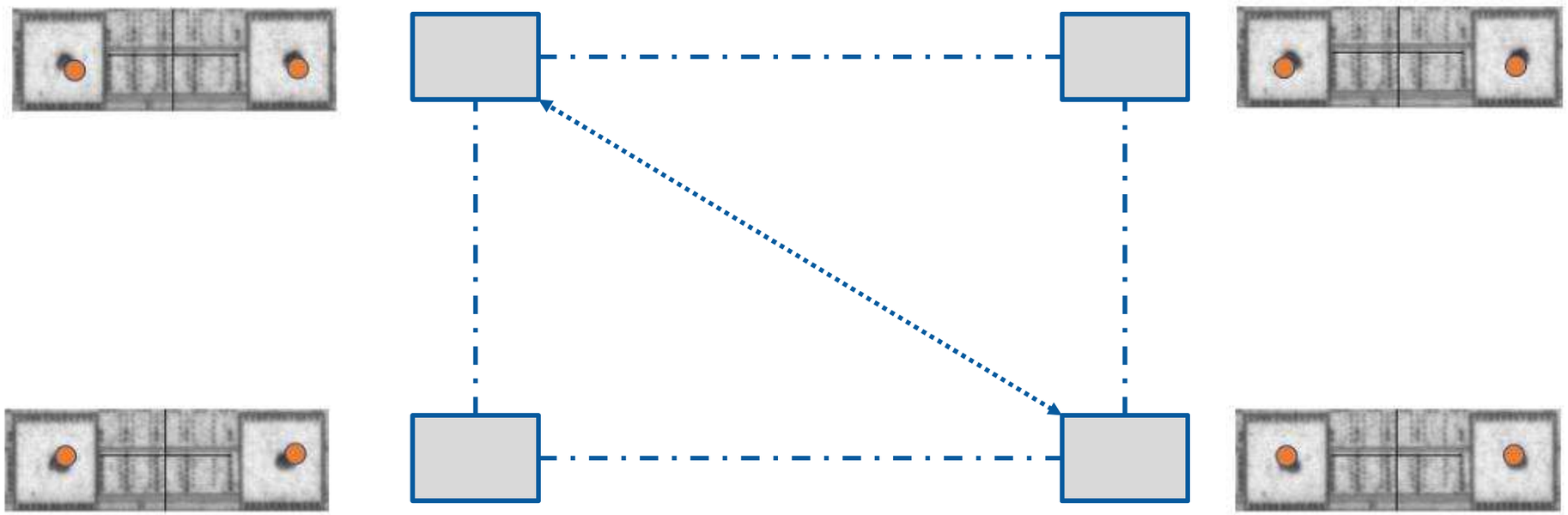
High T Large Array for Automotive grade

Problem statement

- Challenge statement
  - Automotive Customers are requiring more and more large array PHs to work over extended T ranges, from cold to hot.
  - In case of small pad opening, probe marks shifts at the extreme corners of the array can become critical



Source: Technoprobe, SpA with permission

High T Large Array for Automotive grade

Root cause analysis and problem mitigation

- Probe marks shifts between cold and hot probing are mainly related to:
  - Temperature mismatch between lower ceramic plate and wafer
  - Thermal expansion coefficient (CTE) mismatch between lower ceramic plate and wafer

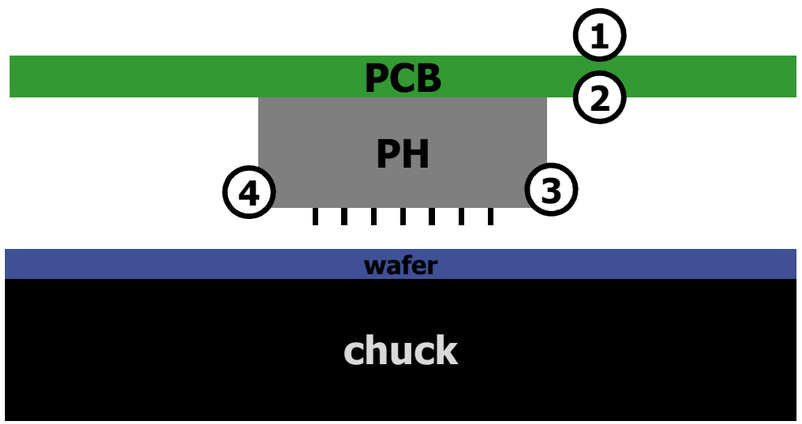
- Problem mitigation
  - Temperature mismatch can be minimized by means of optimized soak time procedure
  - Band guard should be modified in function of pad opening
  - In case of PH active area with a diagonal above 100 mm typical solutions are:
    - Dedicate a PC for cold/RT and one for RT/Hot , with corrected coordinates
    - Evaluate new plate materials with higher CTE to cover the whole probing T range

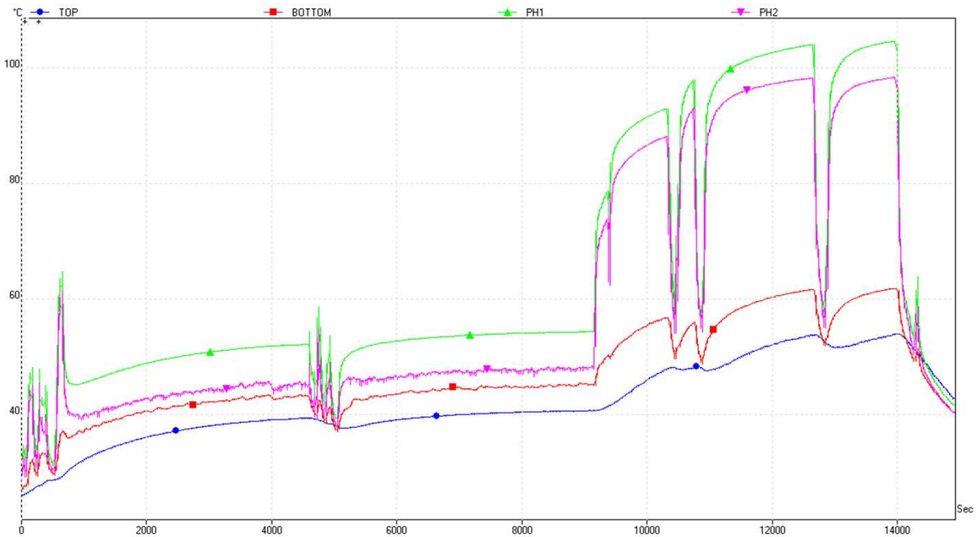
Source: Technoprobe, SpA with permission

High T Large Array for Automotive grade

Importance of probe card soaking

- Thermocouples are installed to monitor temperature:
  1. Bottom PCB
  2. Top PCB
  3. PH @ lower die n°1
  4. PH @ lower die n°2





Touchdown condition	Chuck temperature	Measured LOWER DIE temperature
RT	30 °C	29 °C
HT Without soak time	135 °C	41 °C
HT With soak time	135 °C	102 °C

Source: Technoprobe, SpA with permission

Impact on back-end manufacturing test

Factors

High power dissipation	Large pin/ball count packages	Dynamic Performances	Long test time → High test parallelism → Handling challenges

Impact

From passive to active temperature control	Heavy plunging forces	Signal/Power integrity	Equipment choice Vs number of stages

Countermeasures

Augmented DFT	Data Analytics	Overall review of test concept

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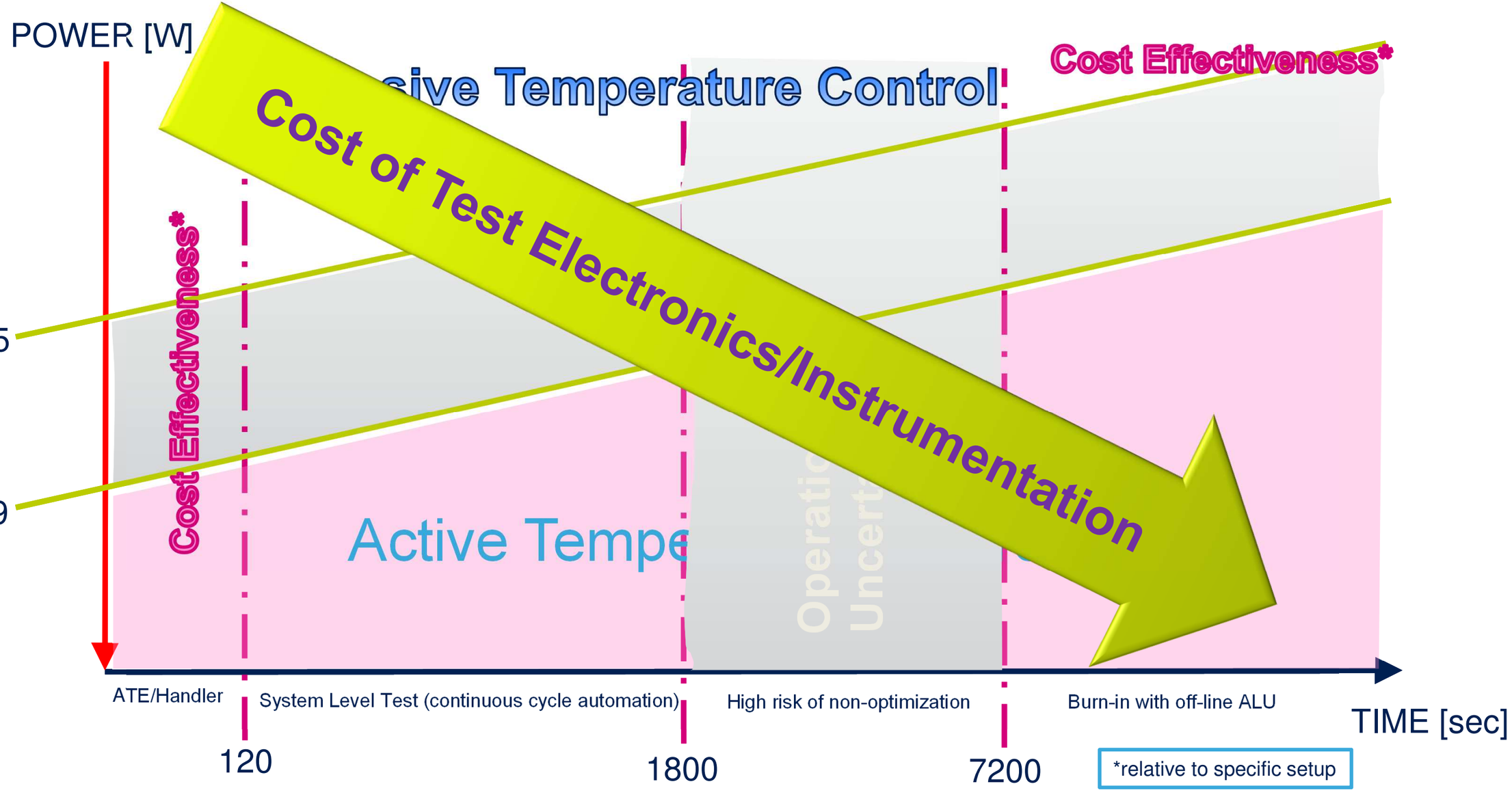
Power Vs test time: choosing the best equipment



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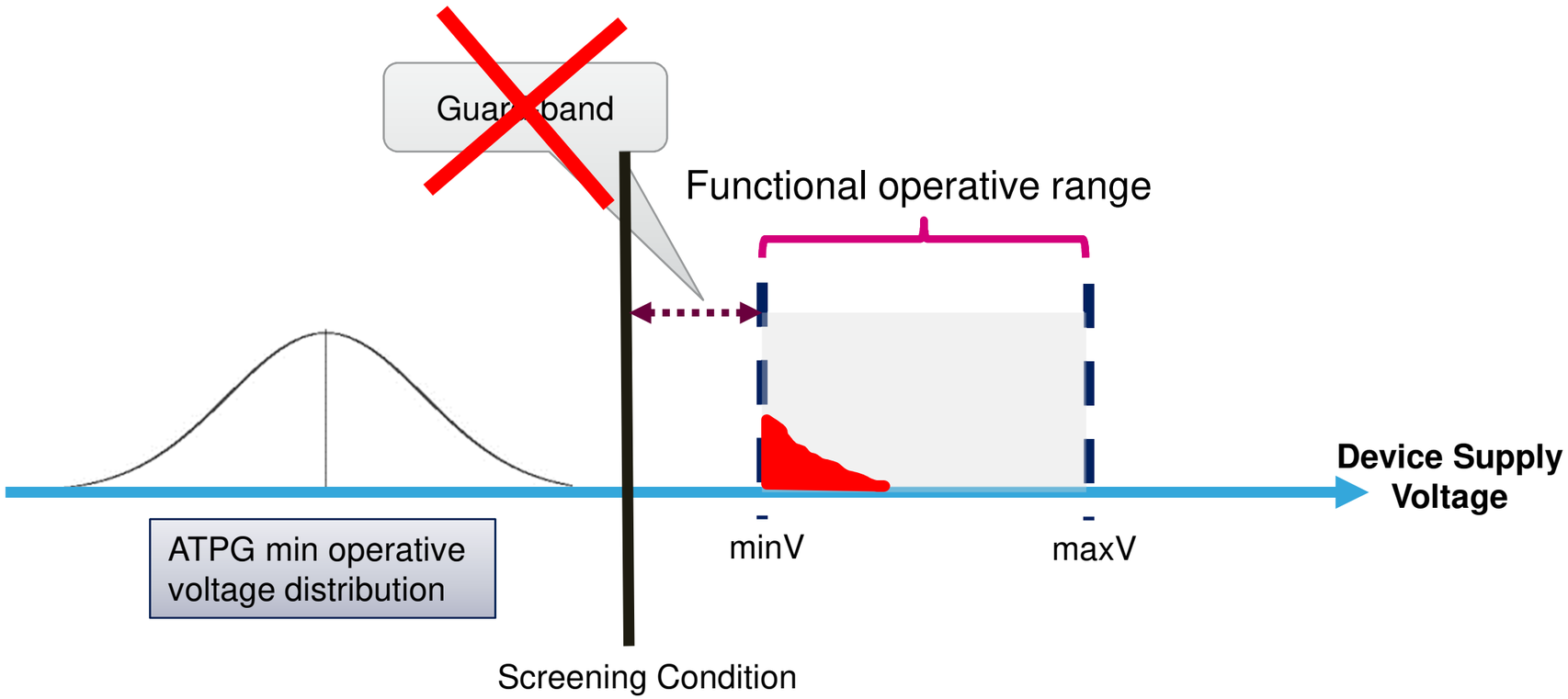
Effects of variability



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Qualitative Coverage Analysis

Stage	Temperature	Tradeoff analysis		Coverage			Other Factors
		Pro's	Con's	Logic & memories	Parametric	H/S I/F	
Wafer sort	COLD	Low static consumption					Parallelism scalability limited by bump count and probe card cost/feasibility
	ROOM	Less demanding industrial setup	Not WC condition for majority of known failure modes				
	HOT		Probe limitations, high static consumption				
Final Test	COLD		Low efficiency and high cost industrial setup				Severe parallelism limitation in case external active components or specific ATE instruments needed to test H/S I/F. Extended test mode testing at COLD might be unrealistic for high dissipation devices. Test mode testing at extreme temperature might determine overkill
	ROOM	Less demanding industrial setup	Not WC condition for majority of known failure modes				
	HOT	Best case for activation of most known package/assembly defects			Ad hoc		
Burn-in	ROOM→HOT	Relatively low cost for <5W devices, with hours duration	Costs not scalable for devices dissipating >5W				Long duration (hours) is not realistically sustainable with tools needed for high dissipation devices
SLT	Multi-temp	Exercise device in true functional conditions	Analytical coverage estimation not available for any fault model beside functional	Functional	Functional	Functional	

COLD = -45ºC

ROOM = 25ºC to 40 ºC

HOT ≥ 125ºC

Screening effectiveness BEST CASE

NEUTRAL

Screening effectiveness WORST CASE

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Key factors

Impacts examples: a special focus on Package Technology

Package complexity: an empirical ranking

Node	Unit	90nm	65nm	40nm	28nm	16nm	7nm
Power	W	1	2	3	6	20	100
Speed	MHz	200	250	500	1600	2200	3600
Dominant Package type	-	QFP	eQFP	eQFP/BGA	FCBGA	FCBGA	FCBGA
Dominant Pad technology	-	Al Pad	Al Pad	Al Pad	Bumps / pillars	SB/CP	SB/CP
Package complexity index*	-	1	2	2	5	6	7

* Qualitative, considers signal count, bonding technology, materials, mission profile

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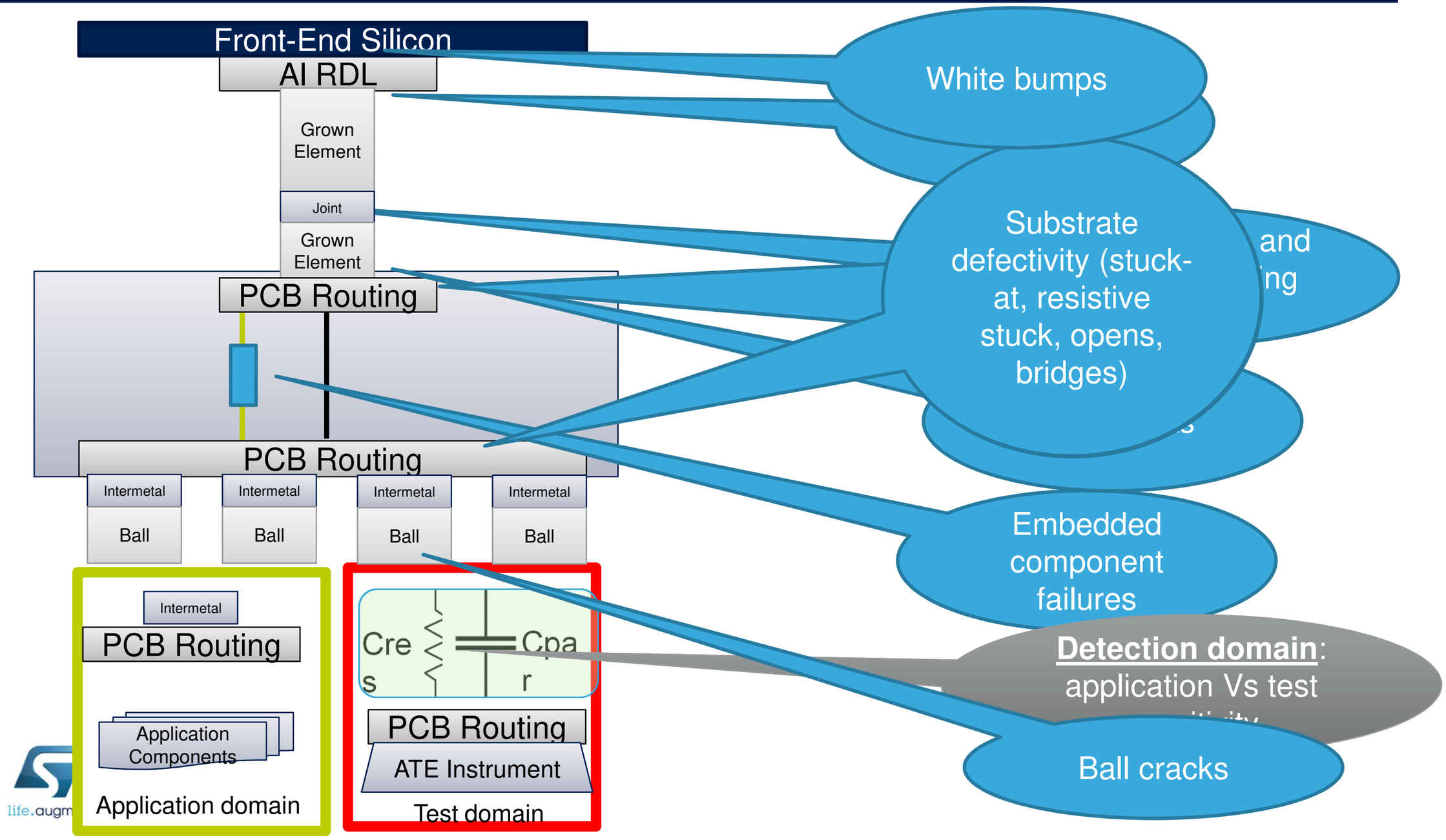
Package-level Testing Challenges: defect modelling



FCBGA Defect Classification

Defect Description	Reliability Sensitivity	Defectivity Dependence	Fault Model	Electrical Detectability
“White” bumps	HIGH	HIGH	Any Stuck model	MEDIUM
Cracks on pillar-silicon joint	LOW	LOW	Stuck-open	HIGH
	HIGH	LOW	Resistive open	LOW
Pillar/bump defectivity	LOW	MEDIUM	Resistive stuck	LOW
Pillar/bump to substrate joint	LOW	LOW	Stuck-open	HIGH
	HIGH	LOW	Resistive open	LOW
Substrate defectivity	LOW	HIGH	Stuck-at, bridge, AC coupling	MEDIUM
Substrate components presence	LOW	HIGH	Stuck-open, resistive open	MEDIUM to LOW
Ball cracks or opens	LOW	MEDIUM	Resistive open	LOW

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High risk: defect might not be active/detectable @ t0

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Extending DFT Scope

Ball Grid Array (BGA) Solder Joint Intermittency Detection: SJ BIST™

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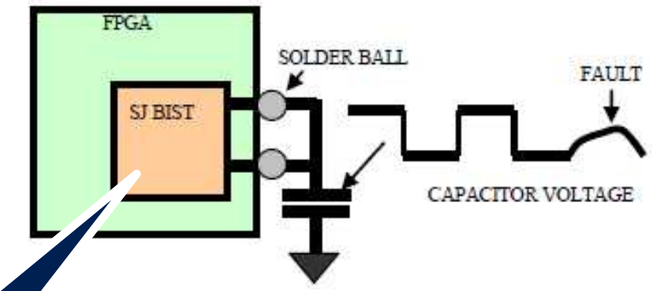

Figure 12: SJ BIST Block Diagram

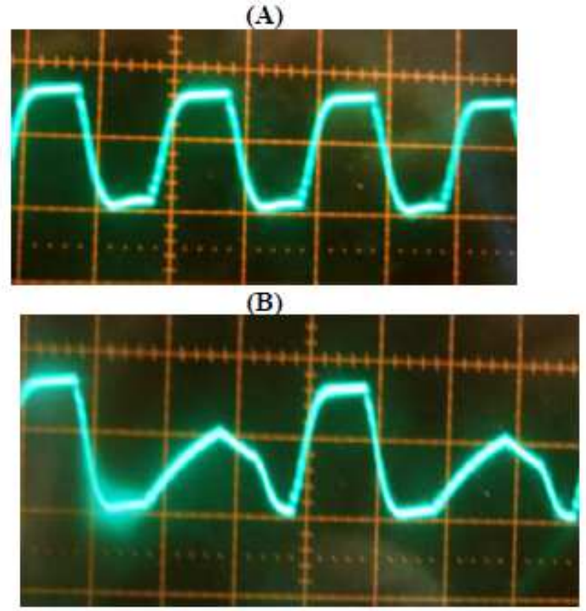

Figure 13: SJ BIST: 1 MHz Capacitor Signal. (A) No Fault; (B) 100 Ω Fault – 0.5 µs x 2.0V Grid.

Extending package co-design concept:
Add DFT IPs into die design to activate defects localized in the package.

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Key factors

Impacts on Test Flow

Cause – Effects diagram

Utilization of very advanced FE technologies	• Relatively lower maturity level of technologies deployed to high-quality sensitive markets • Extreme SoC complexity	Longer test time
Increased data harvesting in the car	• Increased silicon content for data processing in the car • Higher pressure on ASP and manufacturing costs	Higher cost of test impact on device margin
Mechanical and thermal performances (bumps, balls, temperature range)	• Equipment costs • Reliability risks • Parallelism limitation at probe	Higher cost of equipment
Quality and reliability: FE and BE technology, system level effects	• Application dependent risks • Un-modeled defects	Early evaluation of system level marginalities
Coverage	• Evidences of coverage gaps left by structural test • Inefficiency of using	Additional testing types

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Effects on test flow

Wafer Sort ATE/prober-based test cell	**Final Test 1** **ATE + high parallelism P&P Handler**	**Burn-in** Individual Temperature Control	**Final Test 2** ATE + high parallelism P&P Handler	**System Level Test** Active Temperature Control
NEW NEEDS and EFFECTS				
Parallelism limitations Increased test time	Oriented to assembly-defectivity tests	Low density on board, due to power dissipation, individual temperature control	Test time, coverage	Optimized equipment

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Optimizations in The Radar

Optimization directions

- Remove coverage overlaps
- Exploit similarities to merge requirements into single equipment/stages
- Augmented design for test

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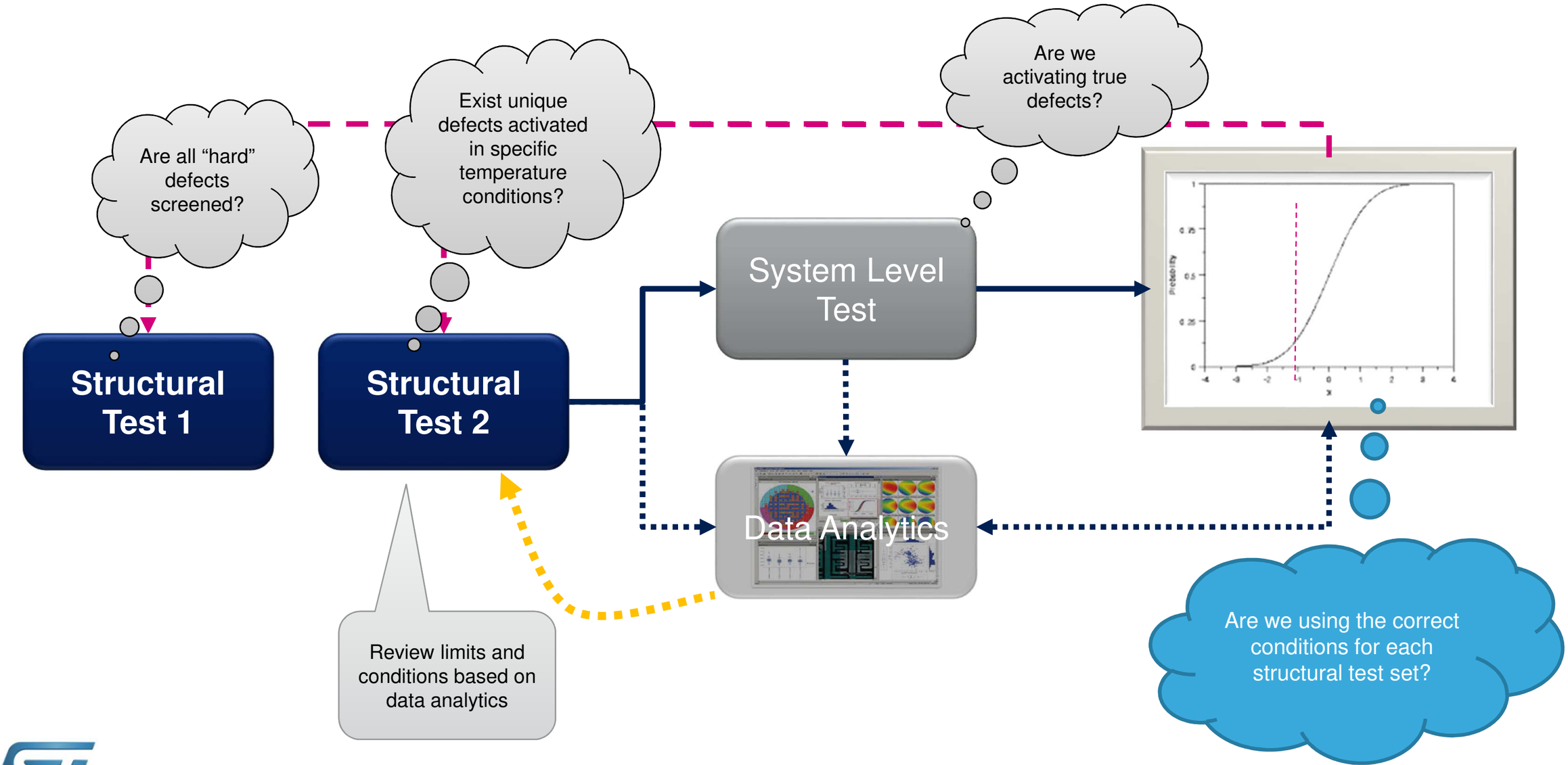
Remove (by understanding…) existing coverage overlaps



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Proven Massively Parallel Development Path

Workflow from Single-Site to Massive Parallelism

Scale Capacity & Functionality as Needed

Courtesy Advantest Test Solutions, Inc

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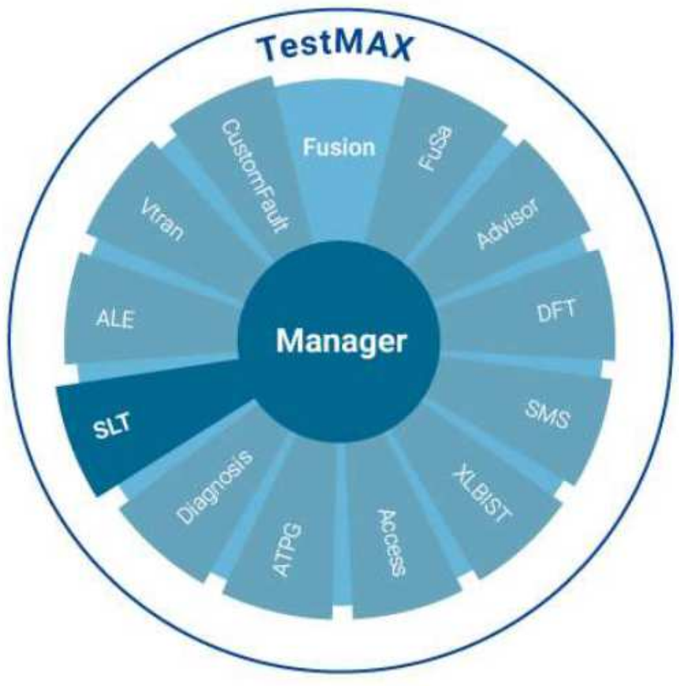
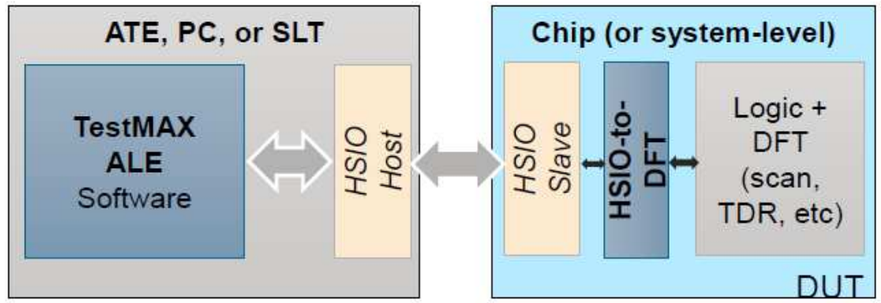
Augmented Design for Test

TestMAX ALE and TestMAX SLT

High-speed / system-level interface for test



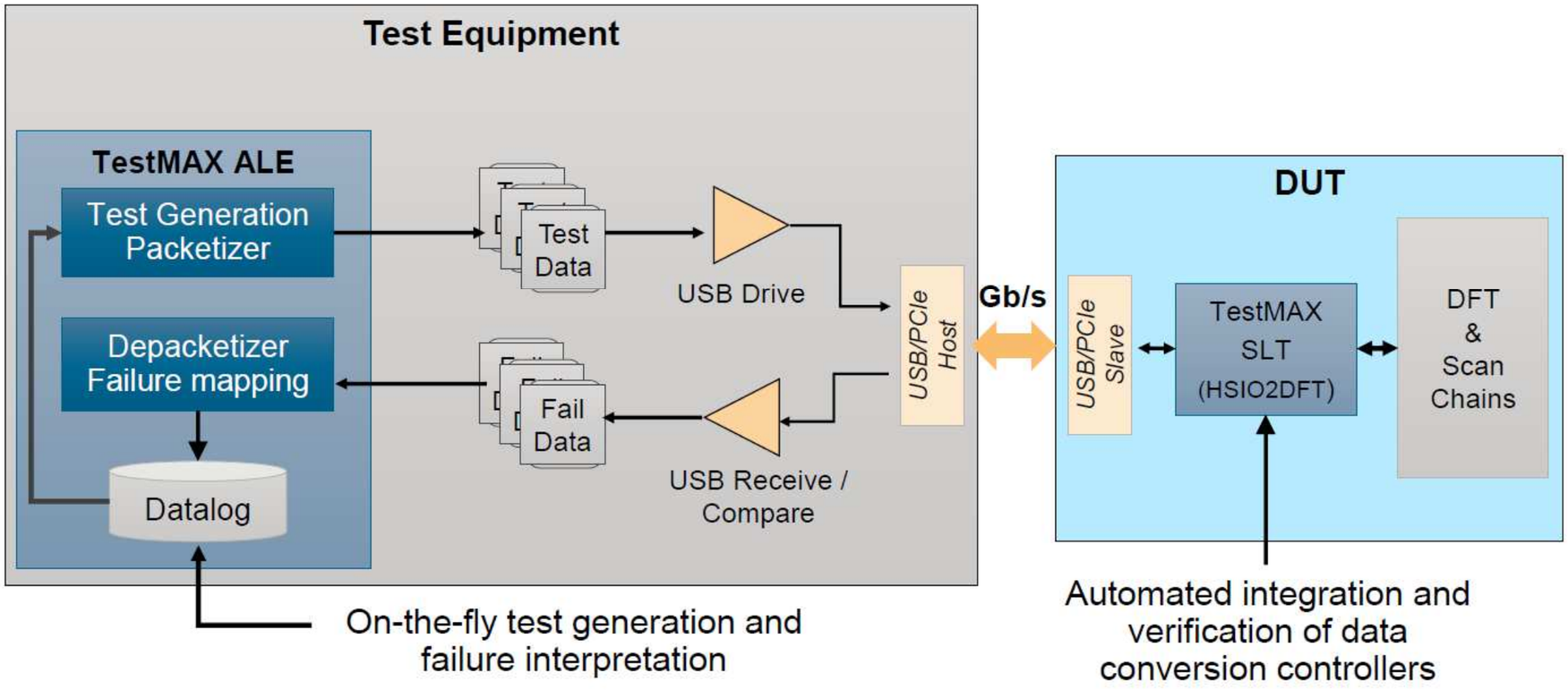


- Re-use existing high-bandwidth functional interfaces
  - USB, PCIe, etc with multi-gigabit data rates
- SLE inserts the HSIO2DFT controller for data format translation (de/packetizing); ALE provides software control
- Benefits:
  - High-bandwidth application helps reduce test time
  - Reduces or eliminates need for dedicated test I/O
  - Provides portability of tests through the product life-cycle

Source: Synopsys, Inc with permission

Accessing DFT through Existing Functional Links

Adaptive High-Bandwidth Test



Source: Synopsys, Inc with permission

Summary

Take out from the product roadmap:

- Automotive is progressively accessing advanced technologies, sometime beyond what the rest of market segments are doing
  - FinFet, SiC
- The roadmap of digital products includes few relevant factors to the test technology needed in the next years:
  - Large die size, wide temperature spectrum, ultra-high bump count and long test time, leading to high parallelism needs
  - High variability, high number of integrated IP's makes traditional structural test less effective on corners of boundary conditions (P, V. T)
  - Package and back-end technologies in general increased their complexity introducing several defect mechanisms, whose detection might not happen only as a side result of testing the silicon
  - Increased silicon content in the car puts pressure on ASP
  - Increased silicon content in the car ALSO increases quality challenges

Summary

Factors relevant to the test technology roadmap:

- Silicon technologies
  - No evidences of defects which can be activated in unique temperature conditions
  - Accurate review of BC/WC screening conditions
- Structural test is weakening progressively its efficiency across PVT:
  - Applicative-oriented test considered to complement existing
  - Data analytic necessary to minimize coverage overlaps
  - Test time duration puts challenges on equipment (performances vs cost)
- Package assembly
  - New defects lead by complexity, BOM and manufacturing process
  - Possibly needed ad-hoc DFT for an effective screening
- Cost
  - Adding stages can be prohibitive, merging appears possible

Thank You!

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