POSTER #

Electrical Performance of Advanced Interconnect Technologies for 5G Applications

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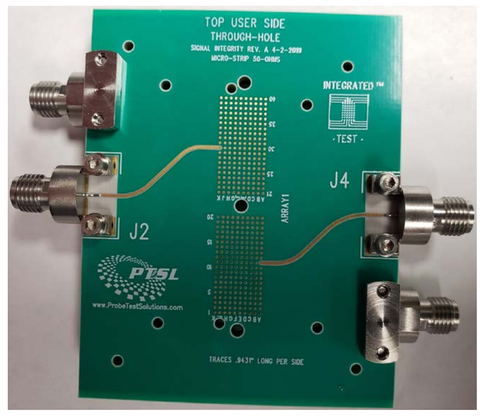
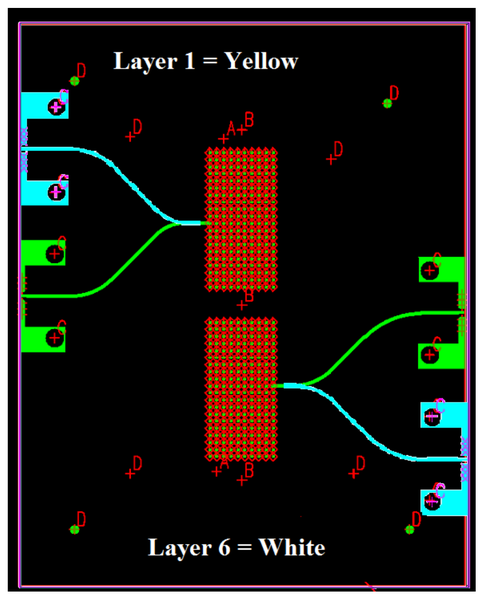
Introduction and Background

- Purpose: As PCB's become more complex with increasing aspect ratios and decreasing device pitch it has become necessary to evaluate different methods for creating the interconnects in the PCB. The purpose of this poster session is to evaluate the electrical characteristics of 3 different PCB interconnect technologies.
- Interconnects evaluated: High aspect ratio through hole via, sintered vias and vias connected through a micro pitch PCB to PCB connector.



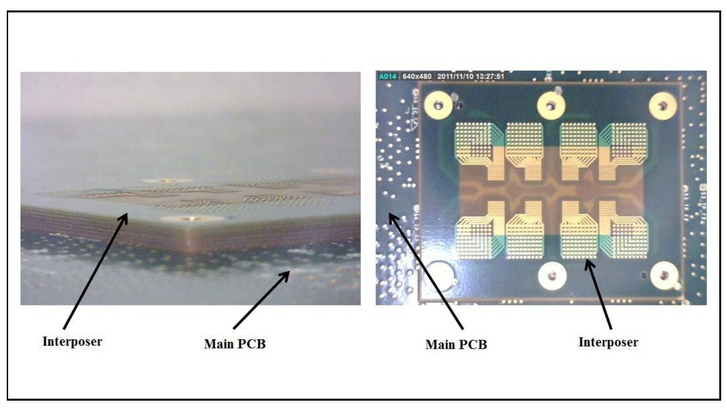


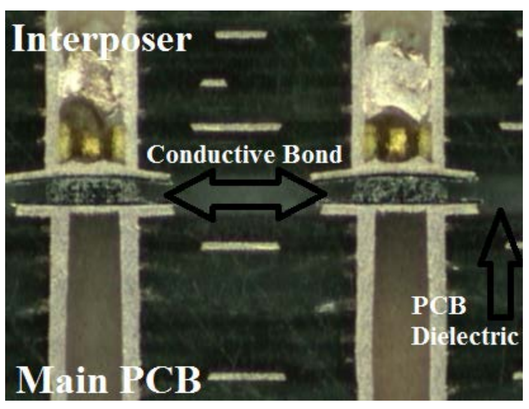
Test Vehicle and Electrical Properties

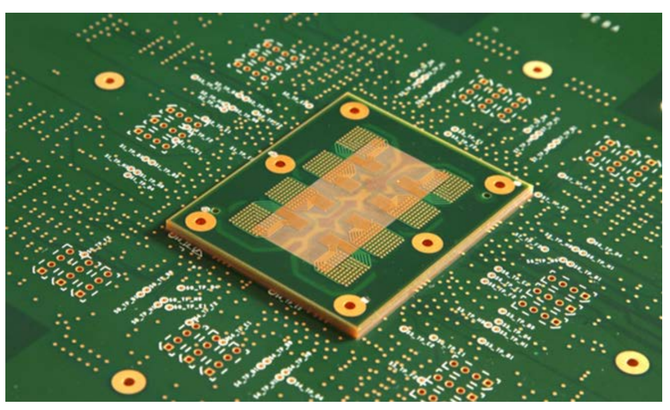
- Test vehicle was designed at 0.160" thickness with 0.006" via (27:1 aspect ratio) with a 50 ohm impedance controlled surface trace on top and bottom surface each connected to an RF connector.
- Test vehicles for sintered via, reflowed via and micro pitch PCB to PCB connector via were processed as two 0.080" thick PCB's which were then connected with each interconnect method.
- Electrical characterization is completed through VNA testing. Electrical properties evaluated: return loss, insertion loss, impedance and rise time degradation.
- 4 samples of each were processed.

Sintered Via Process

- Process consists of completing two independent PCBs through etch and final electrical test. Once completed PCBs are joined with standard PCB dielectric material and conductive paste between the vias. This process results in a permanent bond.

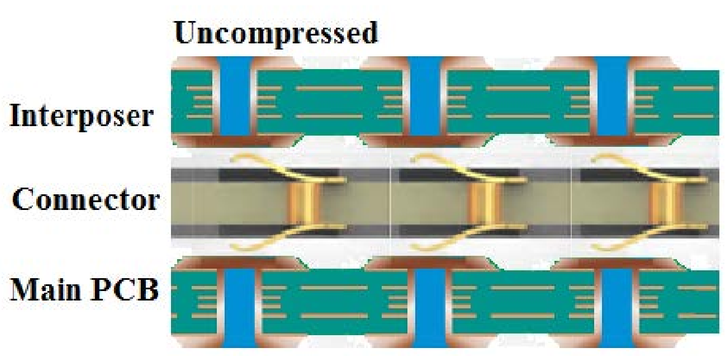


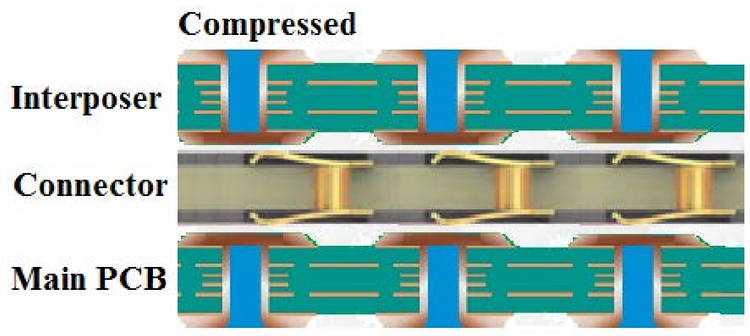




Micro Pitch PCB to PCB Connector Process

- Similar to the sintered via this process consists of completing two independent PCBs through etch and final electrical test. However unlike that process these two PCBs are joined with a micro pitch connector which is not a permanent process.





Process Benefits

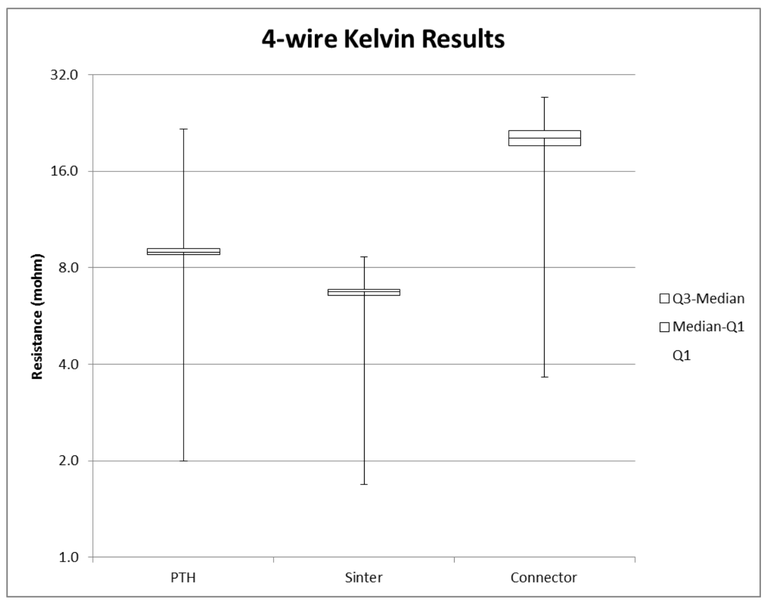
- Reduced aspect ratios increase manufacturing yields and reduce cost.
- Eliminates the need for MLO or MLC to make interconnect between the probe head and main PCB.
- Generic main PCB can be designed for use with multiple interposer configurations. In case where micro pitch connector is used interposers can be switched out as the need arises.

Results

- Vias were not optimized to 50ohm impedance which affected the results.
- Within each group of similar samples there was minimal variation in the test results.
- Sintered via had similar impedance and performed comparably to the through hole via through 20GHz.
- Micro pitch PCB to PCB connector had marginally better performance at low frequencies (less than 10GHz).

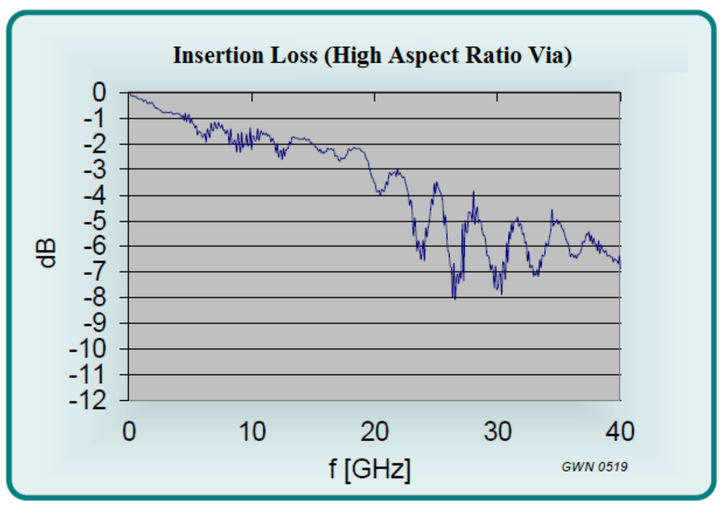
4-wire Kelvin Resistance Measurements

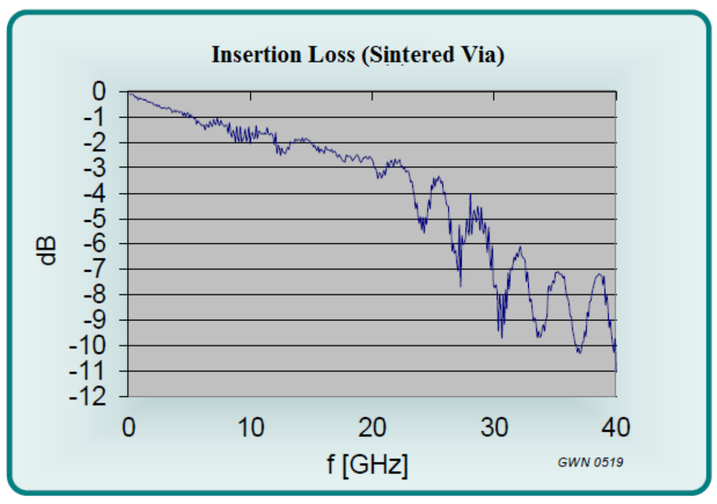
- 4-wire kelvin is a high resolution measuring method where finite changes in via resistance can be evaluated. It is highly accurate because it utilizes a four wire system which negates all current sources, lead and contact resistances.
- On average the sinter paste structure was 2 mΩ lower in resistance than the high aspect ratio PTH Via. This is an indication of the improved manufacturability of lower aspect ratio vias.
- On average the micro pitch PCB to PCB connector was 11 mΩ higher in resistance than the PTH Via.

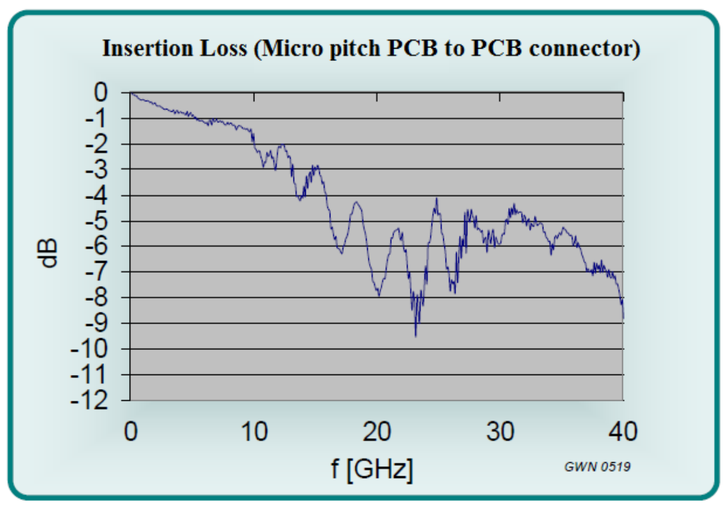


Insertion Loss

- Insertion loss is the loss of signal power when traveling from input through to output.
- The sintered via performed similarly to the high aspect ratio via through 20GHz (~-3dB). Both of these structures were stable through this range (0 - 20GHz).
- The micro pitch PCB to PCB connector was very stable and performed slightly better than the sintered via or high aspect ratio through via at lower frequencies (0 - 10GHz) showing -1.5dB (compared to ~-2dB for the other two samples). However beyond this frequency the loss is not stable and increases in magnitude.

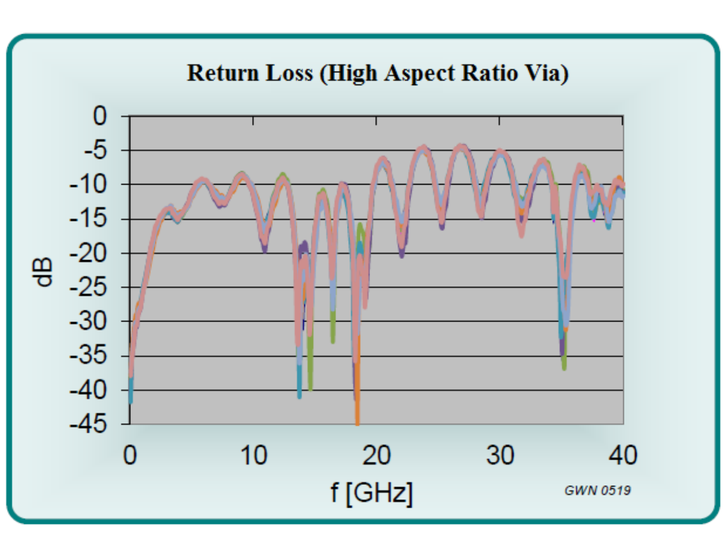


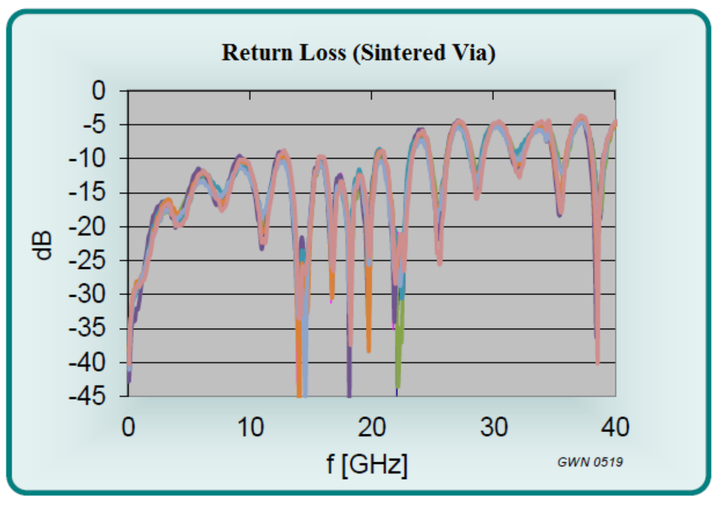


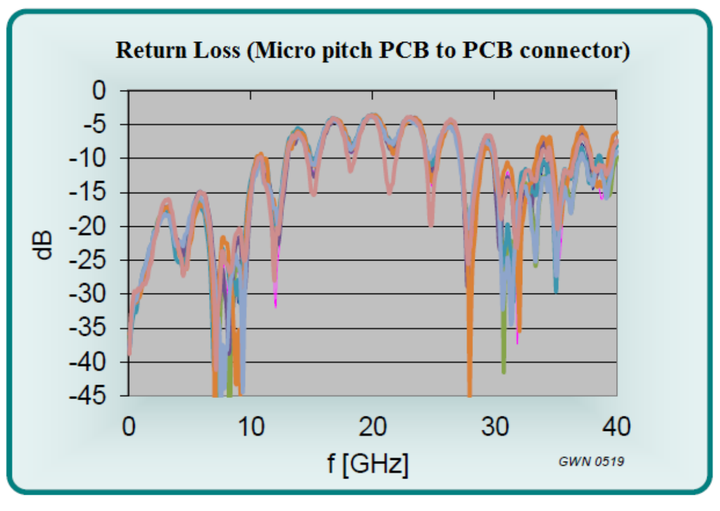


Return Loss

- Return loss is the proportion of signal power that is reflected as a result of an impedance mismatch.
- Return loss showed similar results to the insertion loss in that the sintered via performed similarly to the high aspect ratio through via up to 20GHz. Again the micro pitch PCB to PCB connector performed marginally better through 10GHZ.



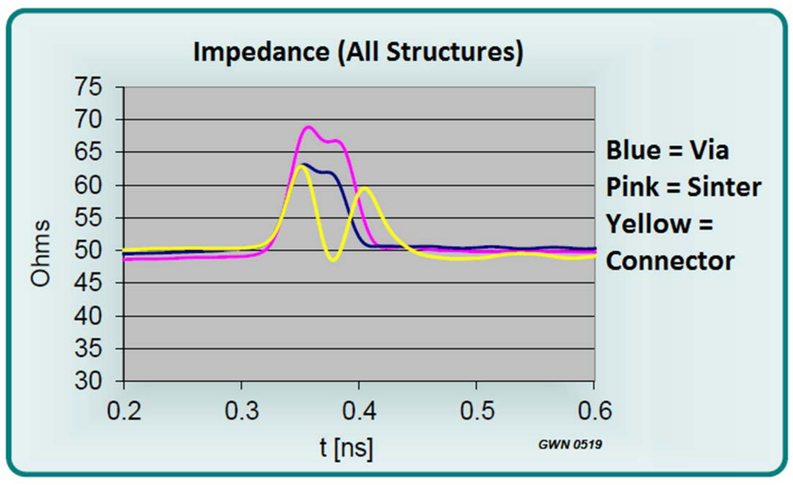




Impedance

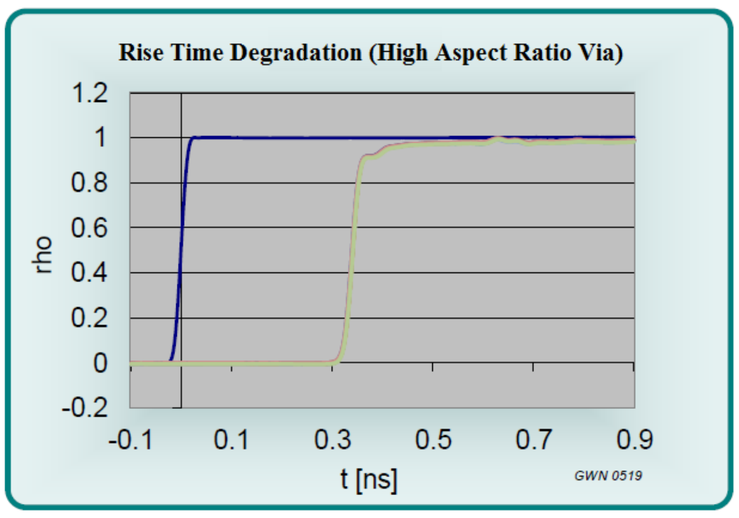
- Impedance is the amount of opposition faced by direct or alternating current when it passes through a circuit.
- Vias were not optimized to 50ohm impedance which affected the results. For future work this will need to be optimized to really show the difference in connection methods.
- Sintered via had similar impedance to the high aspect ratio through via.

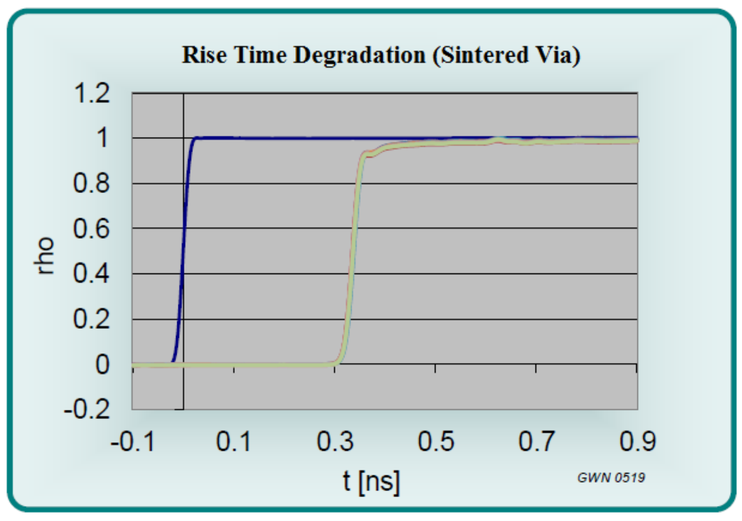
- Micro pitch PCB to PCB connector showed a double peak in impedance which would have adverse effects at higher frequencies. This double peak is a direct result of the composition of the connector (pin + FR4 + pin).

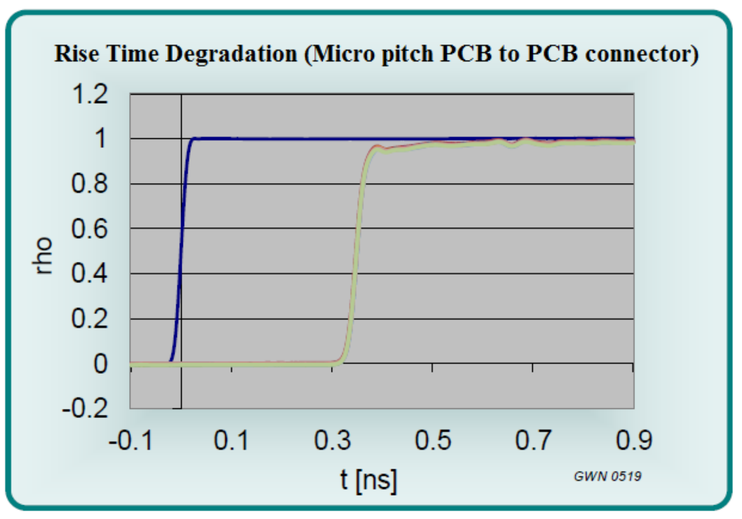


Rise Time Degradation

- Rise time degradation is the increase in the rise time of a pulse as it travels through a circuit.
- All structures showed acceptable values in the 20 – 80% range.
- The sintered via had the lowest delay (AVG = 335.7 ps, Via = 339.4 ps & Connector = 348.6 ps)
- The connector showed some variation due to the impedance mis-match in the connector.







Conclusions

- Sintered Via
  - Based upon the insertion loss and return loss the sintered via performs similarly to a standard high aspect ratio through via s up to 20GHz frequencies.
  - The sintered via sample showed the lowest delay and similar impedance to the high aspect ratio through via which would indicate acceptance for high frequency applications.
  - The kelvin results were lower than the through via which shows the decrease in difficulty in the plating manufacturing processes.

- Micro Pitch PCB to PCB Connector
  - Based upon the insertion loss and return loss the connector is a viable option for low frequency applications (less than 10GHz).
  - Due to Impedance mis-matches in the connector due to its construction its use would be prohibited at higher frequencies,
  - Based upon kelvin results this connector should not be used in applications where there is a sensitivity to resistance.

Further Work

- Two more interconnect methods will be evaluated using this same test vehicle. These are solder ball reflowed and conductive elastomer.
- Temperature testing will be performed on all samples.
- Via impedance will be modeled to 50 ohms and some of the samples will be regenerated.

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