POSTER #02_04

Design and Analysis of Test Interposer for ASIC Package Test with 3D MEMS Co-axial Probe

***TAE-KYUN KIM,** YONG-HO CHO, MICROFRIEND INC.
SANG-KYU YOO, SAMSUNG ELECTRONICS / JONG-GWAN YOOK, YONSEI UNIVERSITY
JONATHAN LEE, NTECHNOLOGY

Introduction

- As better performance devices with higher memory bandwidth emerge in the automotive and the mobile industries, the demands for higher test speeds increase as well.
- Due to the increasing data rate of the devices, the companies who provide the testing technology face more difficult challenges to meet all the requirement.
- Signal/Power integrity issues increase
  : Crosstalk, Jitter, Skew, Inter-symbol Interference (ISI)
  PDN (power delivery network), Eye-diagram
- The needs for testing and analyzing for IC Packages without soldering on mainboard increase.

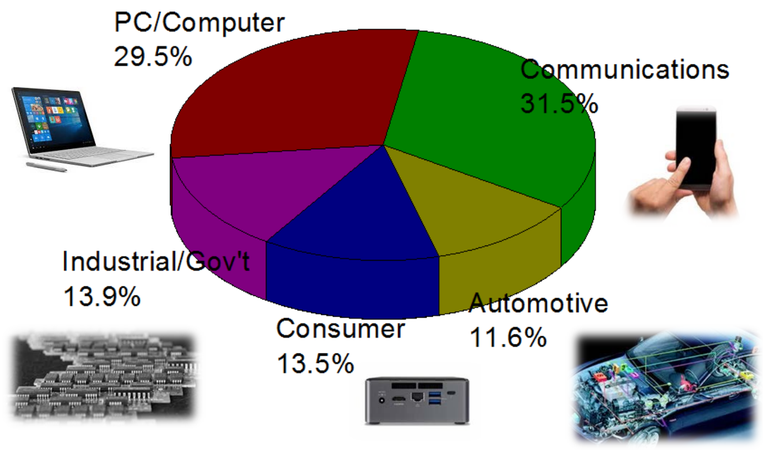


Fig.1. Global Semiconductor Market, Sourced by World Semiconductor Trade Statistics (WSTS), Google

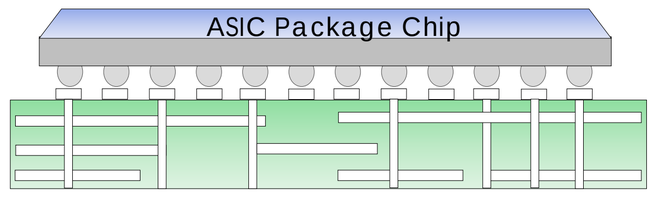


Fig.2. Mainboard

Proposal of Test Interposer with 3D MEMS Co-axial Probe

- Finding a new testing method for packages to monitor data signal without any physical damage.
- Proposing reusable test interposer and data access with less set up time.
- The test interposer uses 3D MEMS co-axial probe instead of soldering. It can provide vertical interconnections among the ASIC package chip, test interposer, and main PCB.

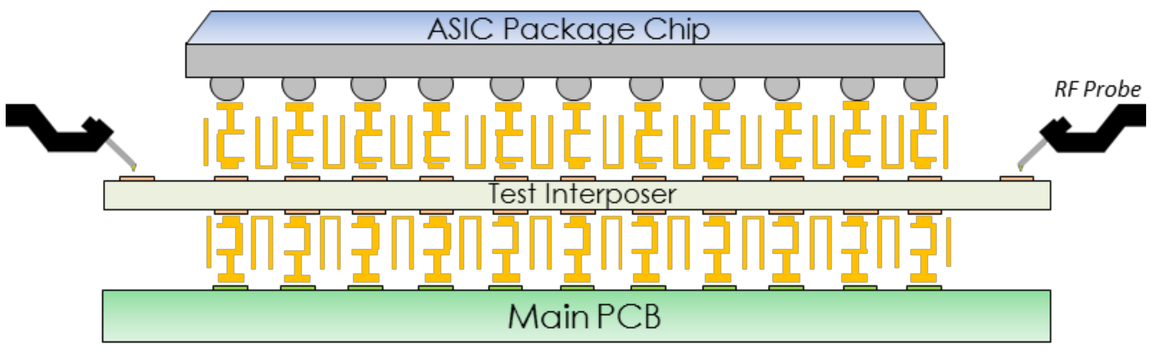


Fig.3. Test Interposer System for ASIC Package Test

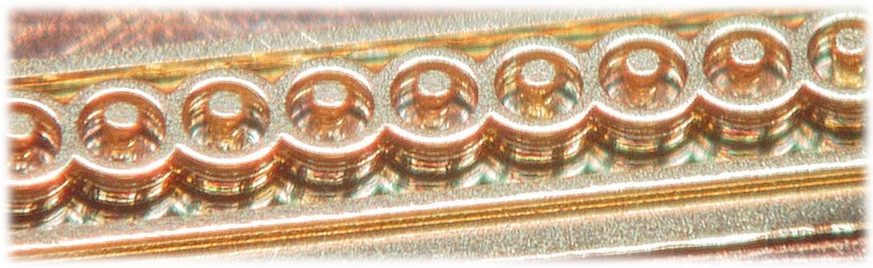
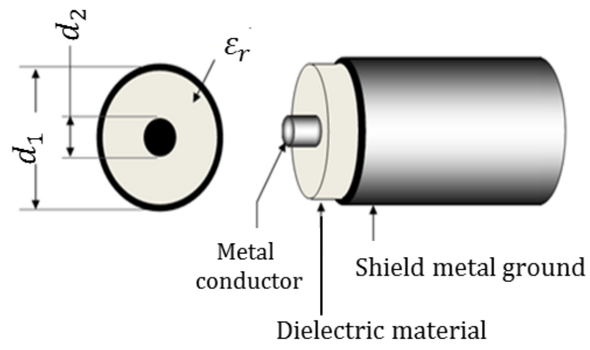


Fig.4. 3D MEMS Co-axial Structure

- For testing high-frequency with a small signal loss, 3D MEMS co-axial socket is the best choice for matching impedance using a ground shield.
- The 3D MEMS co-axial probe socket can be fabricated into different kinds of shapes to satisfy what customer demands for the device : Fine pitch, high reliability, and better mechanical performance.



$$Z_O = \frac{138}{\sqrt{\varepsilon_r}} \log_{10} \frac{d_1}{d_2}$$

Where,
Z_O = Characteristic impedance of line
d_1 = Inside Diameter of Outer Conductor
d_2 = Outside Diameter of Inner Conductor
ε_r = Relative Dielectric Constant

Fig.5. Co-axial Impedance Theory

Design of Test Interposer & 3D MEMS Co-axial Probe

▪ Design Consideration of Test Interposer

- Multi-layer polyimide thin film (Dielectric Constant : 3.2)
- Signal trace Impedance matching
  Single ended : 50 Ohm / Differential : 100 Ohm
  (* Main factors : dielectric thickness, trace width/height)
- Ground & Power Plane / Mesh Plane
- Require flexibility (bend near 45 degree)
  due to many components on PCB
- Circuit design on polyimide thin film is fabricated by MEMS process (Etching, Electroplating, Lithography, Chemical mechanical polishing)

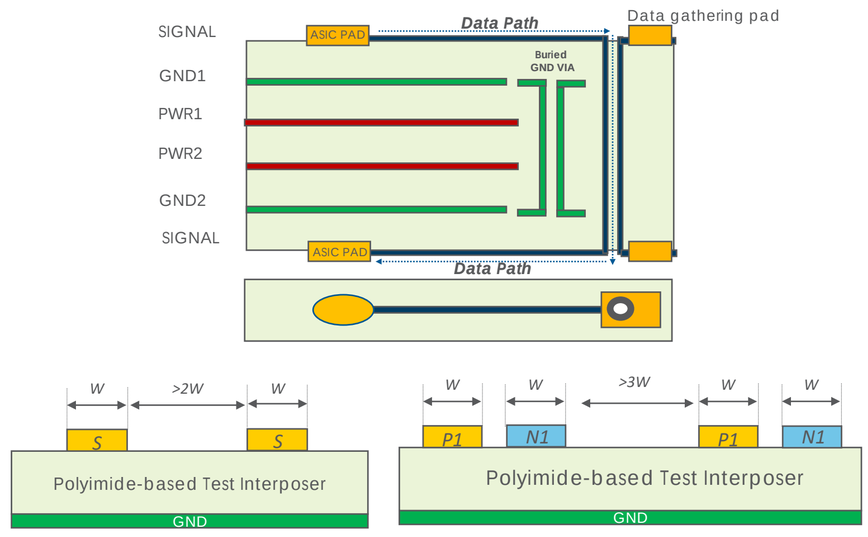


Fig.6. Test Interposer signal design concept

▪ Concept of Co-axial Probe

- Coaxial transmission geometry (outer ground shield) conductor forms a shield preventing external magnetic-field from crosstalk.
- The probe is composed of a core signal, an outer ground shield, and a dielectric material - polydimethylsiloxane ($\varepsilon_r = 2.63$)
- High quality signal for high frequency due to the well-defined signal impedance.
- The shielding and specific dielectric keep the core signal separated to promote good impedance matching that results in the high signal quality.

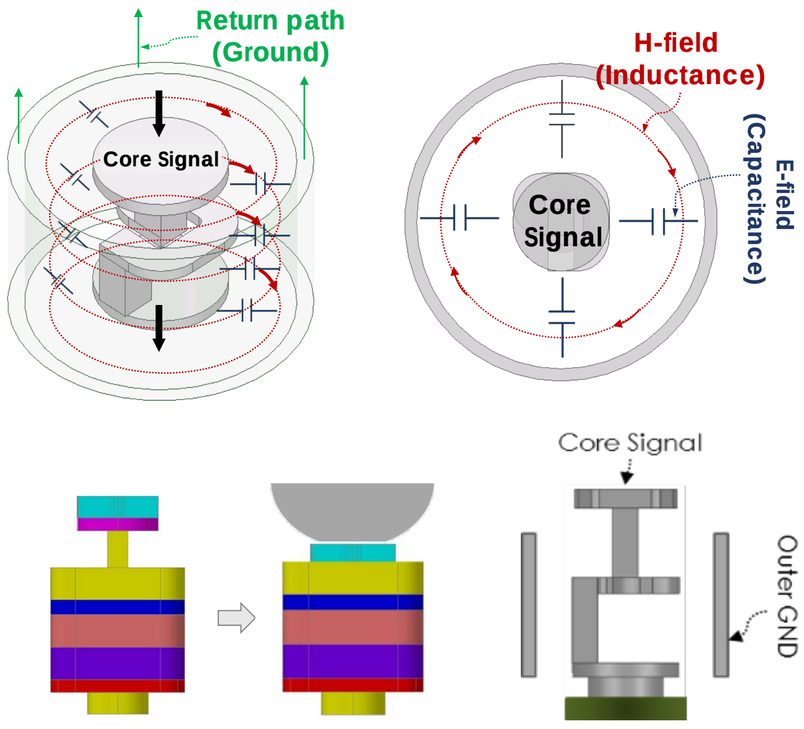


Fig.7. 3D MEMS Co-axial Probe Structure

Verification of 3D MEMS Co-axial Probe

▪ 3D MEMS Co-axial Socket Products

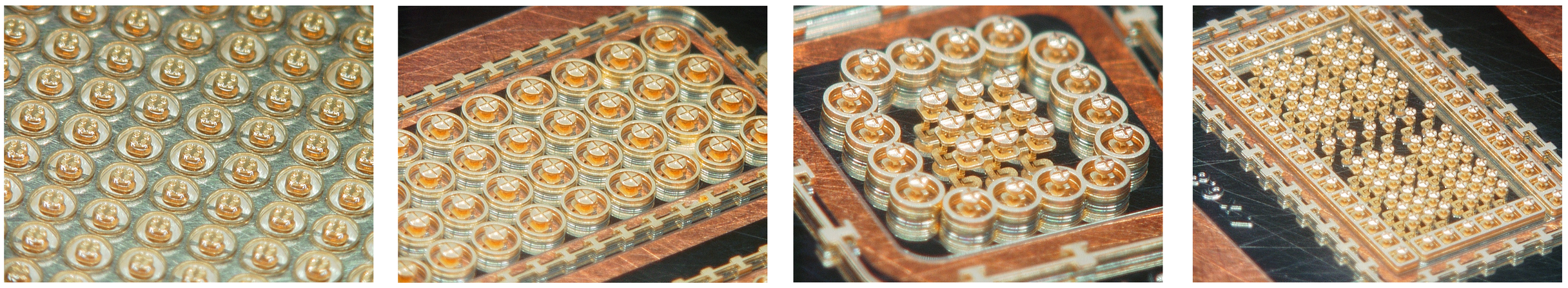


Fig.8. 3D MEMS Co-axial Socket (1.0pitch / 0.8pitch / 0.6pitch / 0.3pitch)

▪ Measurement System (Electrical Characteristics & Mechanical Characteristics)

Fig.9. Co-axial Measurement with 1mm Connector (110GHz)

Fig.10. Mechanical Test

▪ Analysis of Measurement (Electrical & Mechanical)

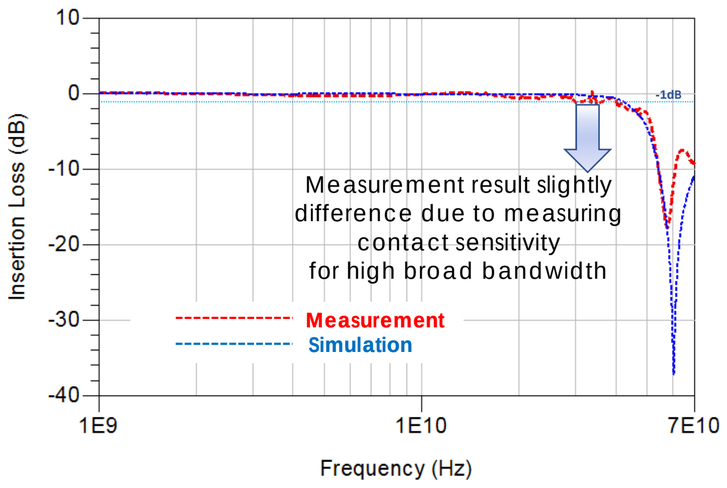


Fig.11. Co-axial Insertion Loss

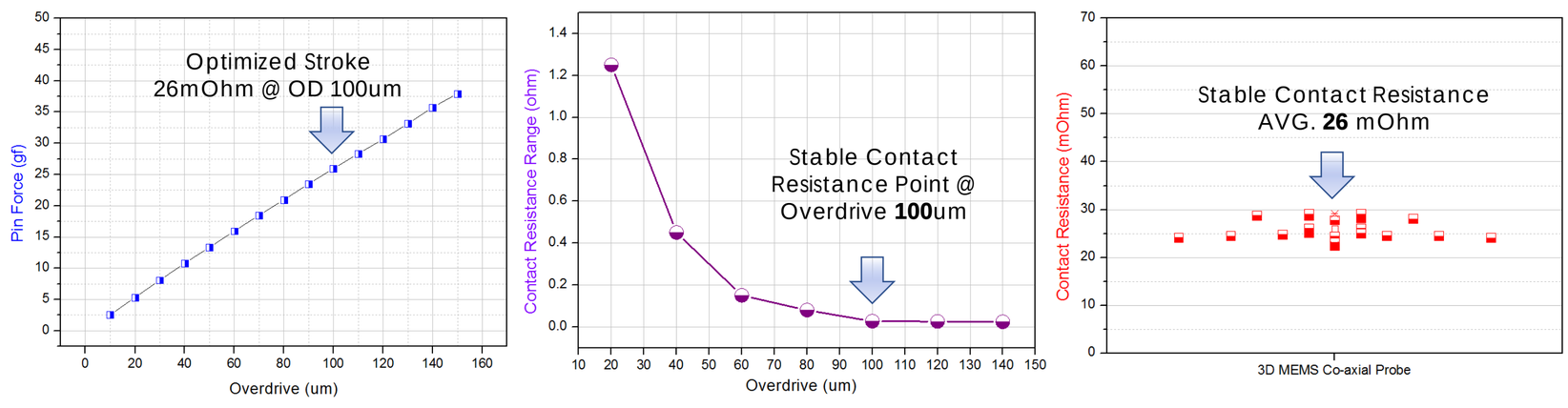


Fig.12. Mechanical Characteristics of Co-axial Probes

Verification of Test Interposer

▪ Design of Test Interposer

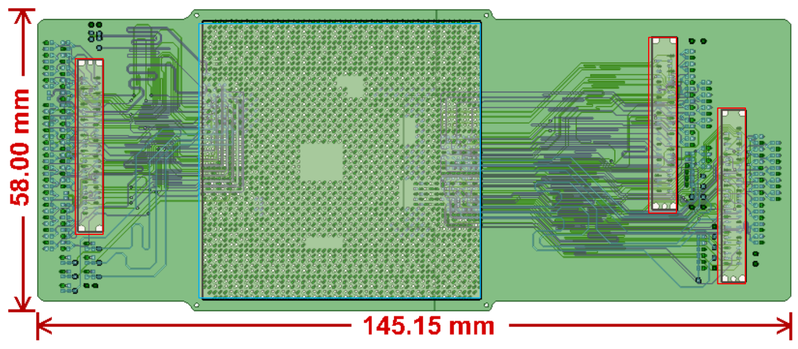


Fig.13. Dimension of Test Interposer

[Interposer Information]

- 6 layers of test interposer
- Polyimide based ($\varepsilon_r = 3.2$)
- Total thickness 0.4T
- Pad pitch 1.0mm
- Trace Length : 70mm /matching
- Signal Trace Re-distribution by MEMS Fabrication
- Total # of ASIC Pins : 2778 pins (Signal, Power, GND)

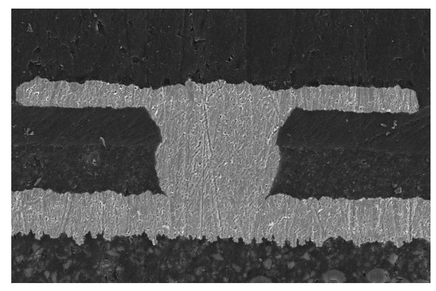
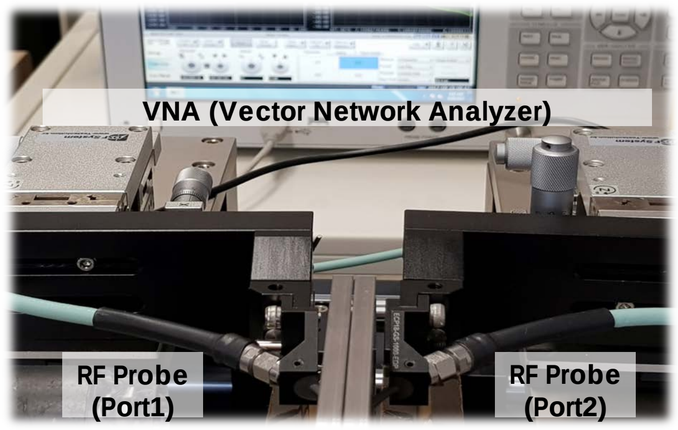


Fig.14. VIA Hole Fabricated by 3D MEMS Process

▪ Measurement System (Electrical Characteristics & Mechanical Characteristics)



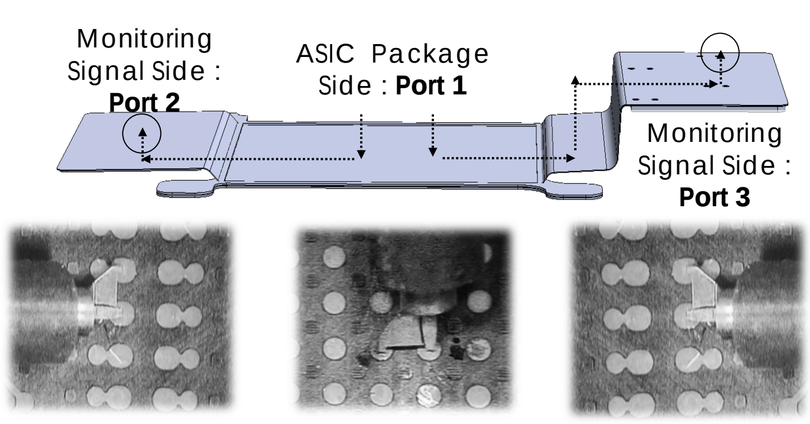


Fig.15. Measurement Setup to analyze Test Interposer

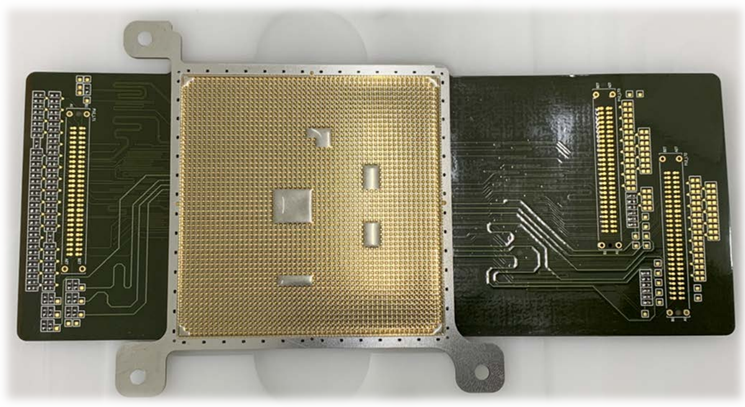


Fig.16. Product of Test Interposer

▪ Experimental Verification of Test Interposer

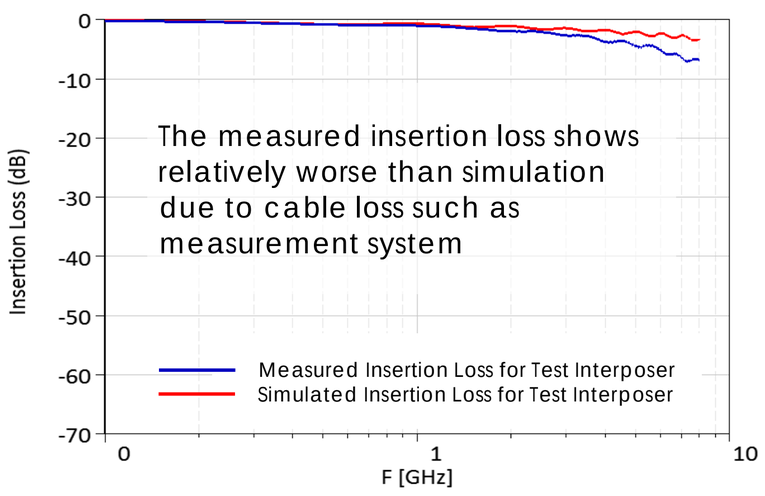


Fig.17. Frequency-Domain Measurement and Simulation for Test Interposer

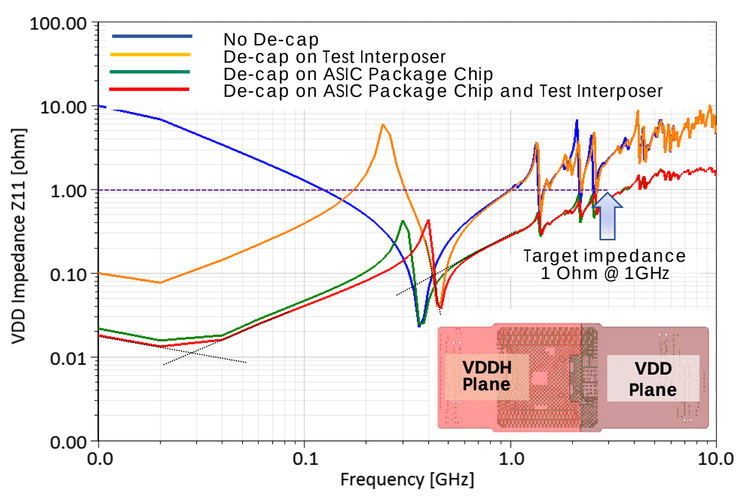


Fig.18. Decoupling Capacitor Effect on the Test Interposer and ASIC chip

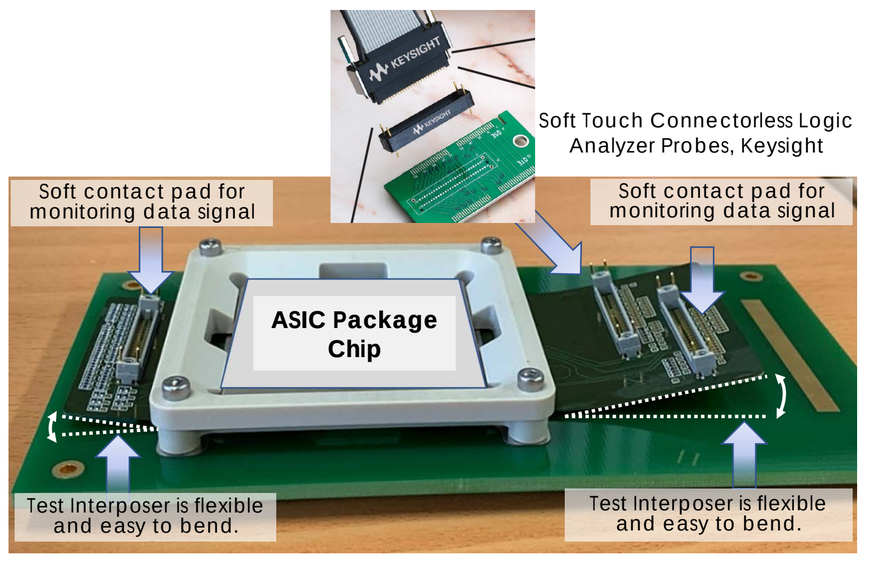
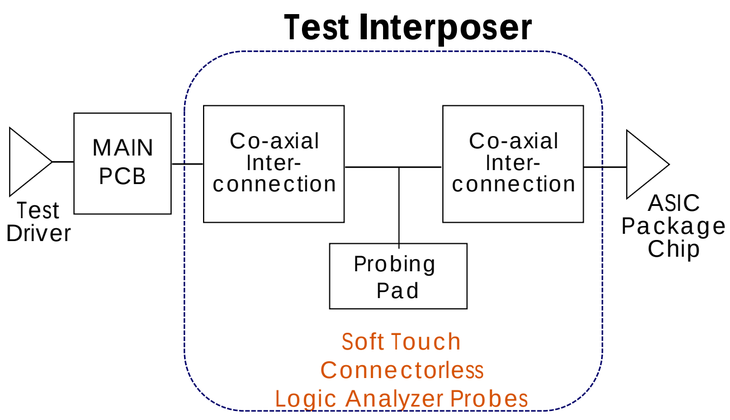


Fig.19. Assembly of Test interposer

▪ Simulation-based Verification of Test Interposer with 3D MEMS Co-axial Probe



- Time Domain Simulation
- Input Data : PRBS input
- Voltage Amplitude : 0 ~ 1.1V
- Data Rate : 1.0GHz(2.0Gbps)~2.0GHz(4.0Gbps)
- Simulation Tool : ANSYS Electronics

Fig.20. Simulation Conditions for Test Interposer System

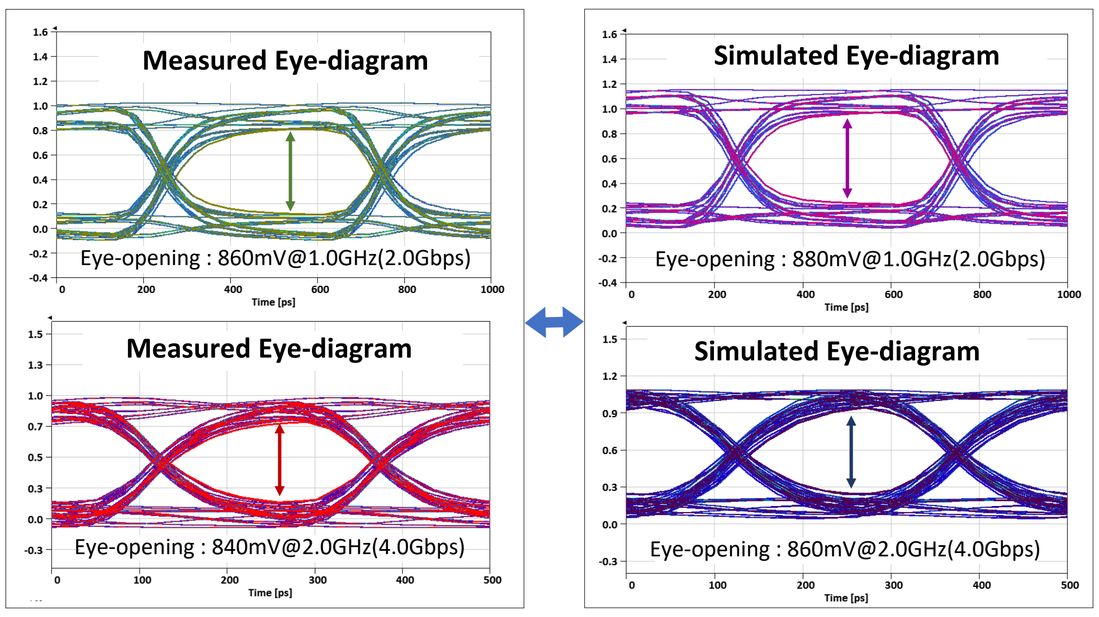


Fig.21. Comparison of Eye-diagram at Test Interposer with Co-axial Probe

Conclusion

- Proposed test interposer with 3D MEMS co-axial probe for testing ASIC package.
- Adopted 3D MEMS coaxial probes for contacting Interposer and main PCB.
- Verified the reliability of simulation and measurement on the performance of 3D MEMS co-axial socket and test interposer.
- Analyzed the test interposer system accessible to monitor data signal of the ASIC package chip without any damage.

Contact Information

- kinggerm@microfriend.co.kr (South Korea)
- jonathanlee@ntechnologyinc.com (USA)

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