SWTEST

PROBE TODAY, FOR TOMORROW

Practical Method For Detecting Hot-Stepping, Micro-Arcing Or Hot-Switching During Wafer Probe

Texas Instruments

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Overview

- Introduction/Background
- Definitions
- Causes and Effects
- Methods and Challenges
- Results/Improvements
- Summary

Introduction/Background

Maintaining probe card tip integrity and life during wafer probing becomes a challenge as the device under test (DUT) increases in complexity and testing requirements.

- Some factors contributing to this challenge include:
  - Full temperature range test coverage
  - Prolonged test times
  - Yield requirements
  - Bond pad damage specification requirements

Introduction/Background

Two aspects of this challenge that can be controlled:

- Physical:
  - Probe Mark Inspection (PMI) improvements
  - Overdrive (OD) optimizations
  - Probe tip cleaning optimizations
  - Probe tip technology improvements
- Electrical:
  - Program yield improvements
  - Program test time reduction
  - Electrical Over-Stress reduction
  - Hot-switching, Hot-stepping and Micro-arcing

This presentation will focus on one of the most prevalent electrical factors (Micro-arcing) and highlight a way to help detect and mitigate it.

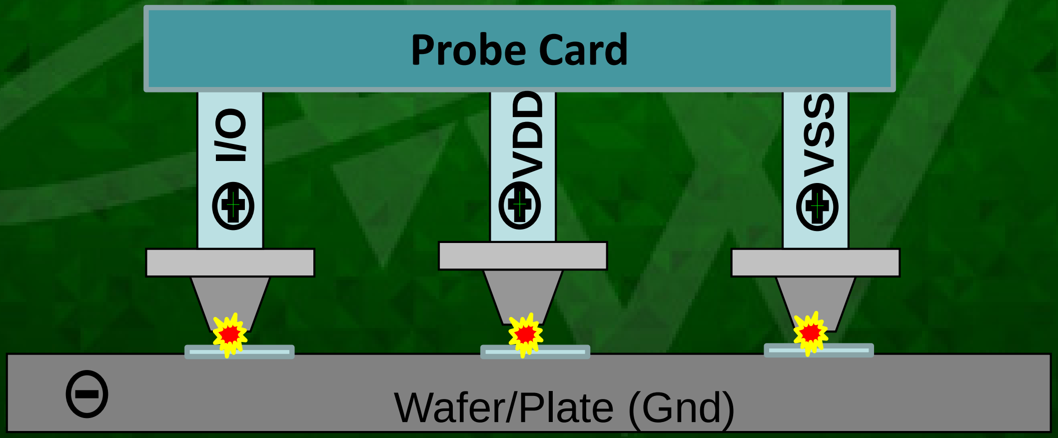
Definitions

Hot-switching:

Voltage potential shock event that exist between two contacts while connecting or closing a circuit.

Hot-stepping:

Process that takes place when a probe card indexes (steps) from die to die on a wafer (or surface plane) while an electrical charge or potential difference exist between the surface and the probe tips.



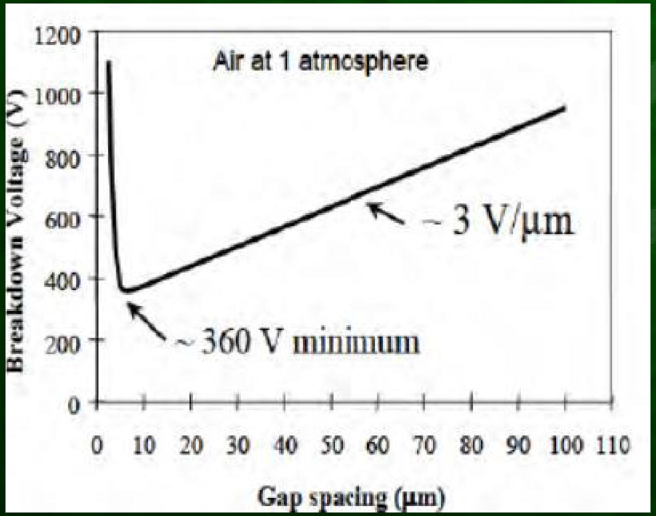
Definitions

Micro-arcing:

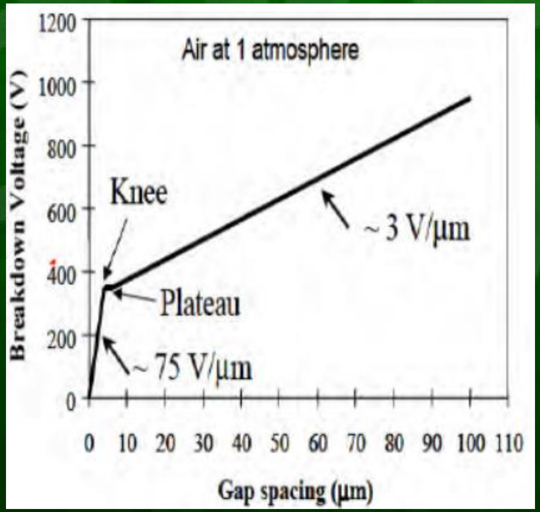
Effect produced at the contact point(s) such as probe tips during a Hot-stepping or Hot-switching event.

It's arcing at a micron level with varying degrees of severity.

Per Studnicki et al, "arcing caused by the electric field will melt the surface of the tip and will create miniature craters"…"is an electrical breakdown of gas which produces an ongoing plasma discharge and results in a current flow". For gaps <5-7um, the breakdown is caused by "field emission and electrons tunneling" rather than gas and this "will happen at voltage differences below 1V at nm gaps" [Studnicki et al].



Paschen Law per Studnicki et al, "for gaps >5um")



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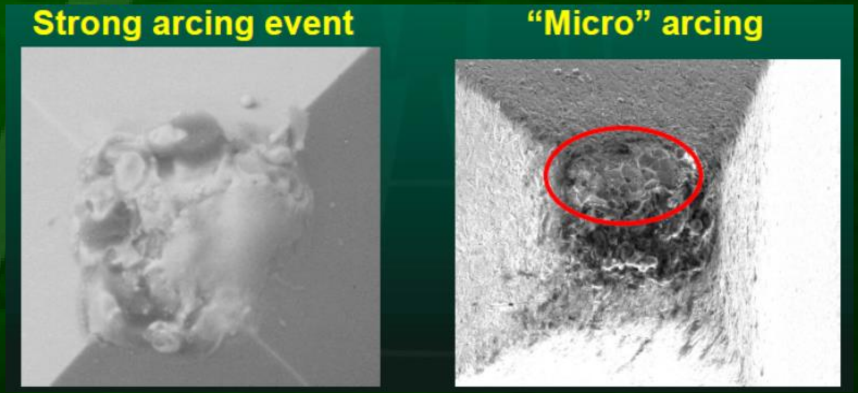


Probe Tip SEM pictures from Huebner et al, FFI

Cause and Effects of Micro-arcing

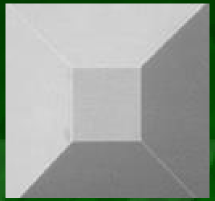
Stages of micro-arcing during a hot-stepping event:

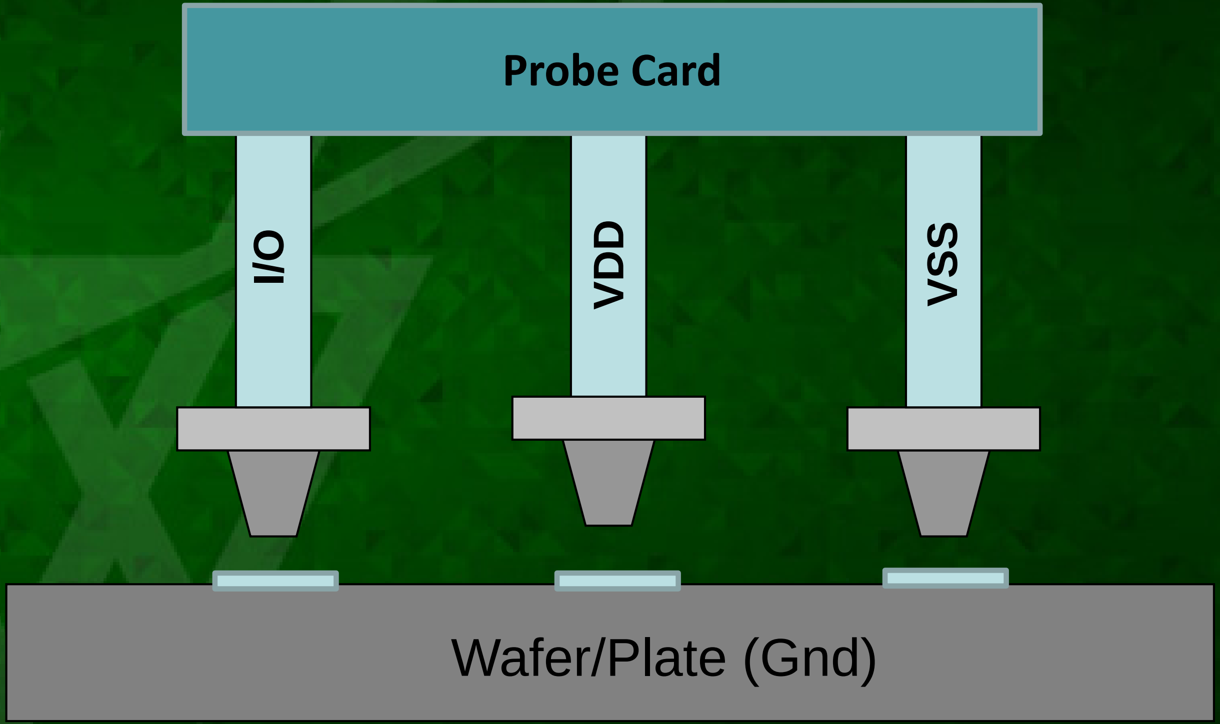
Index: Probes with Charge positioned above new X/Y.

Z-up: First contact at micro-gap and arcing starts to form.

Melting occurs and plasma generated and expelled.

Tip left with droplets or molten material.





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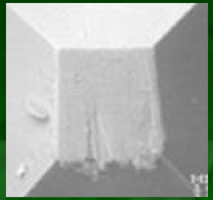

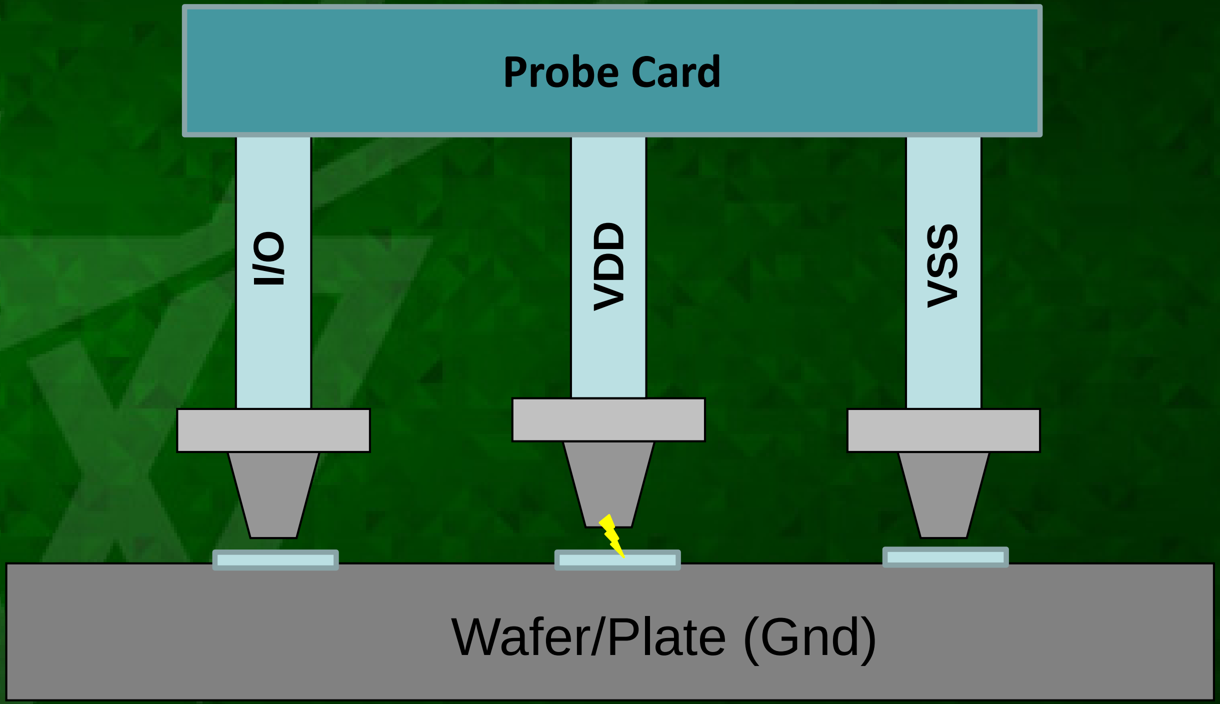

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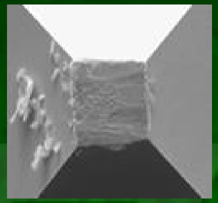

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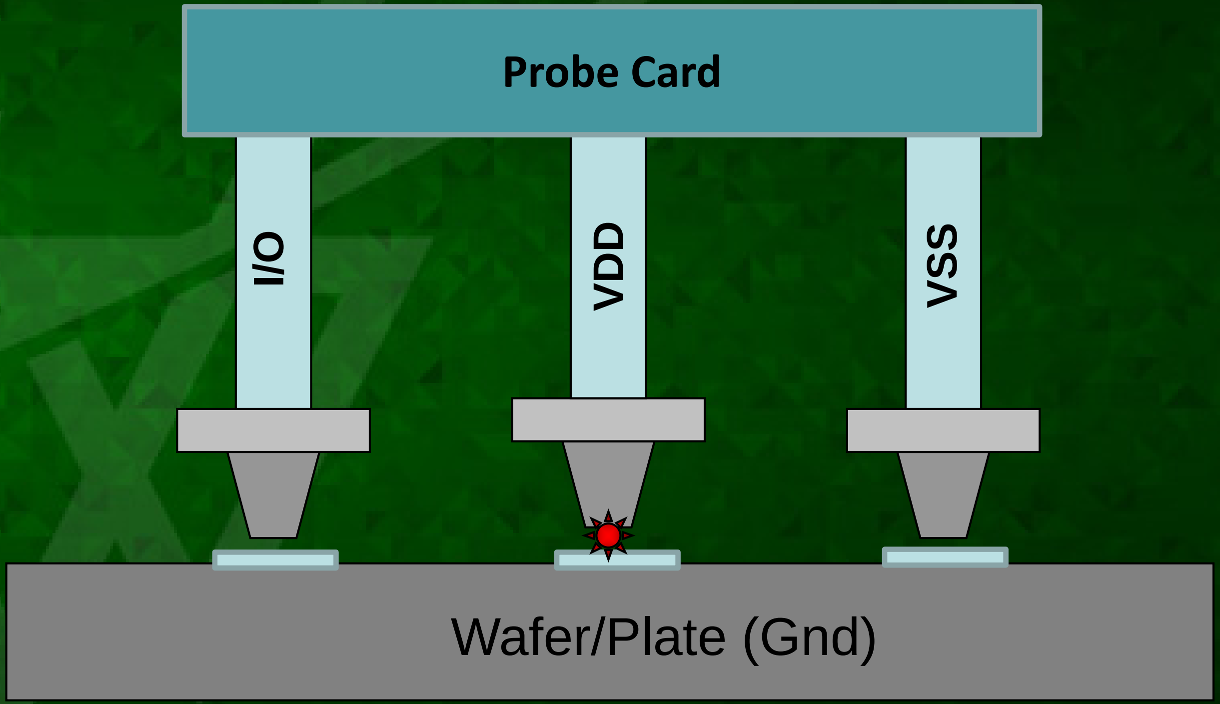

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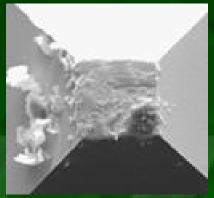

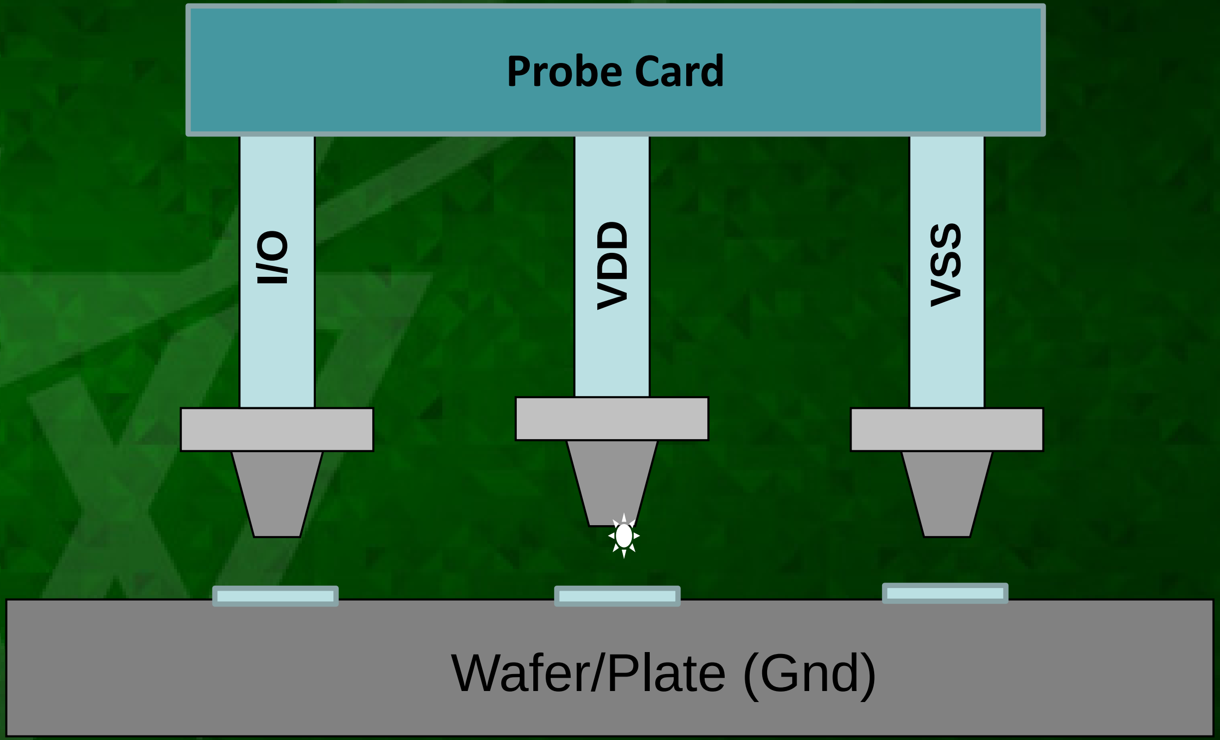

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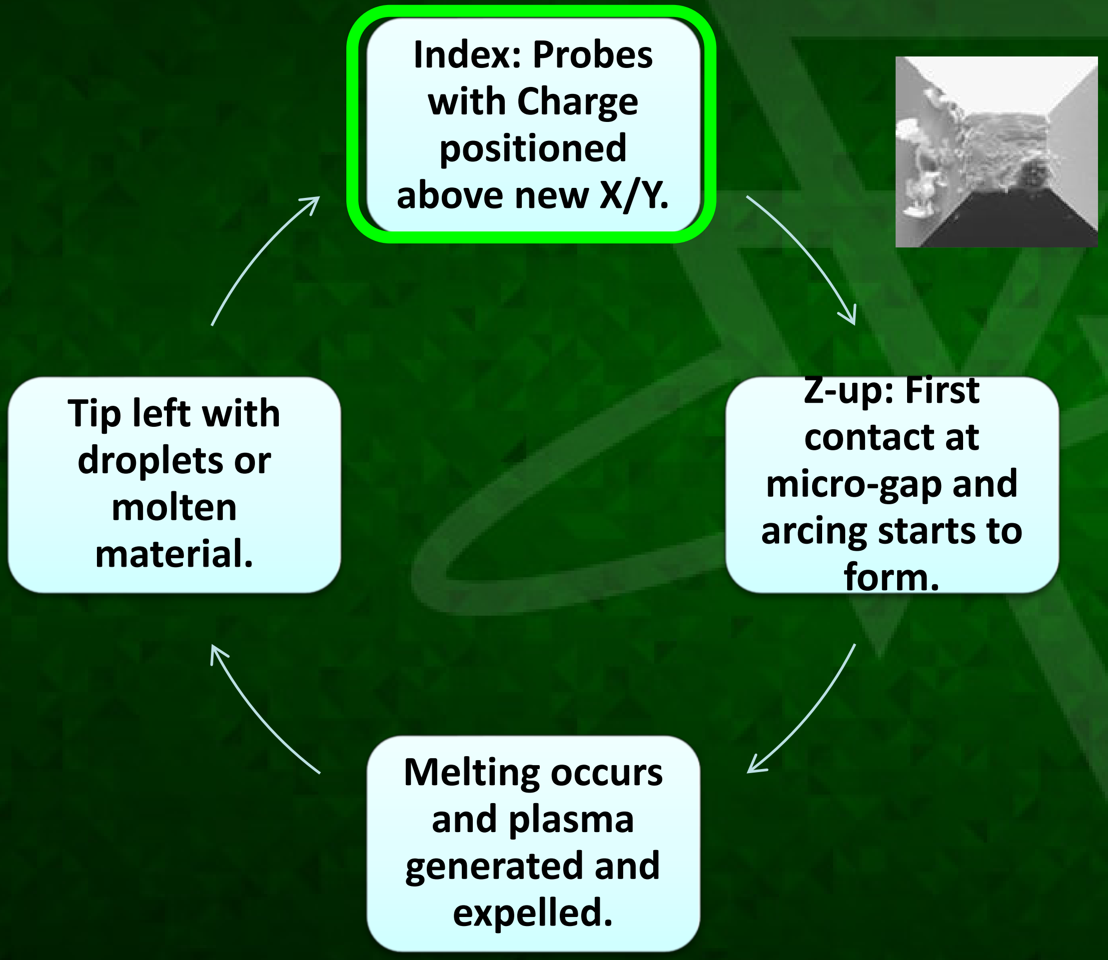

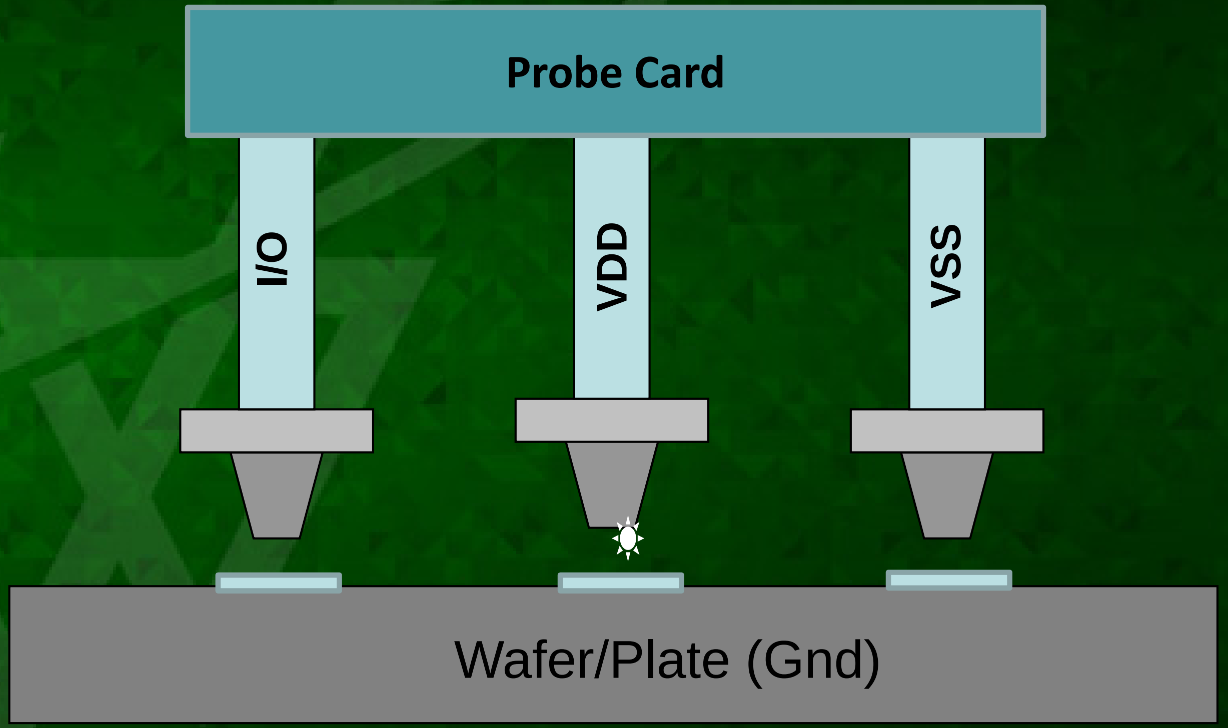

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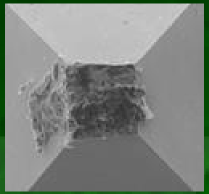

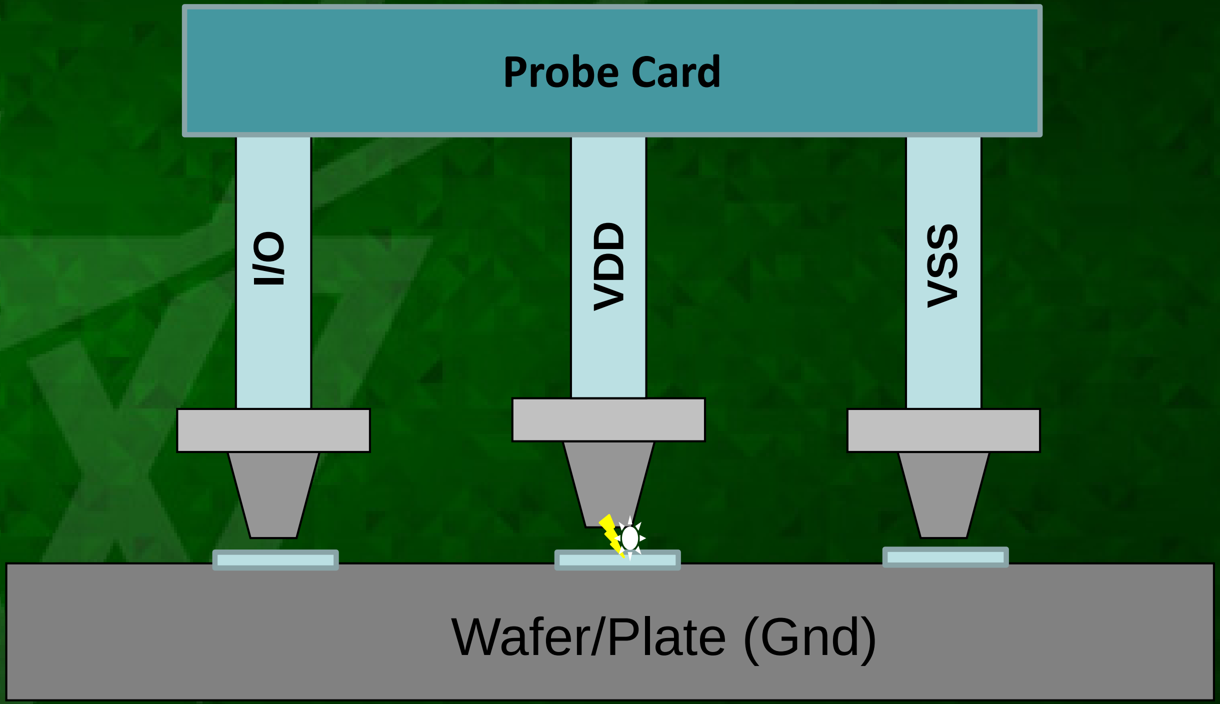

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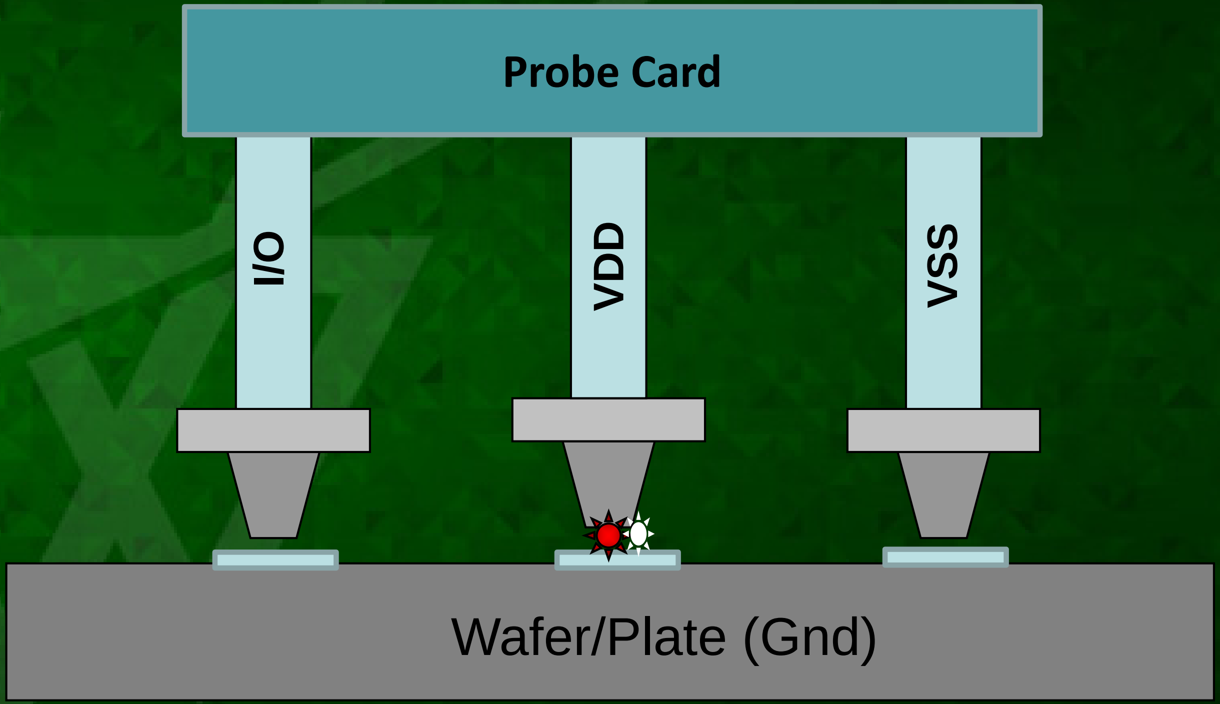


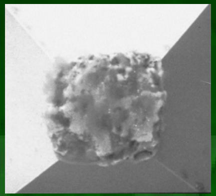
SEM pictures and drawings from FFI et al.

Cause and Effects of Micro-arcing

Stages of micro-arcing during a hot-stepping event:

* This process will continue and intensify with each touch down until next cleaning cycle or failure.

Index: Probes with Charge positioned above new X/Y.



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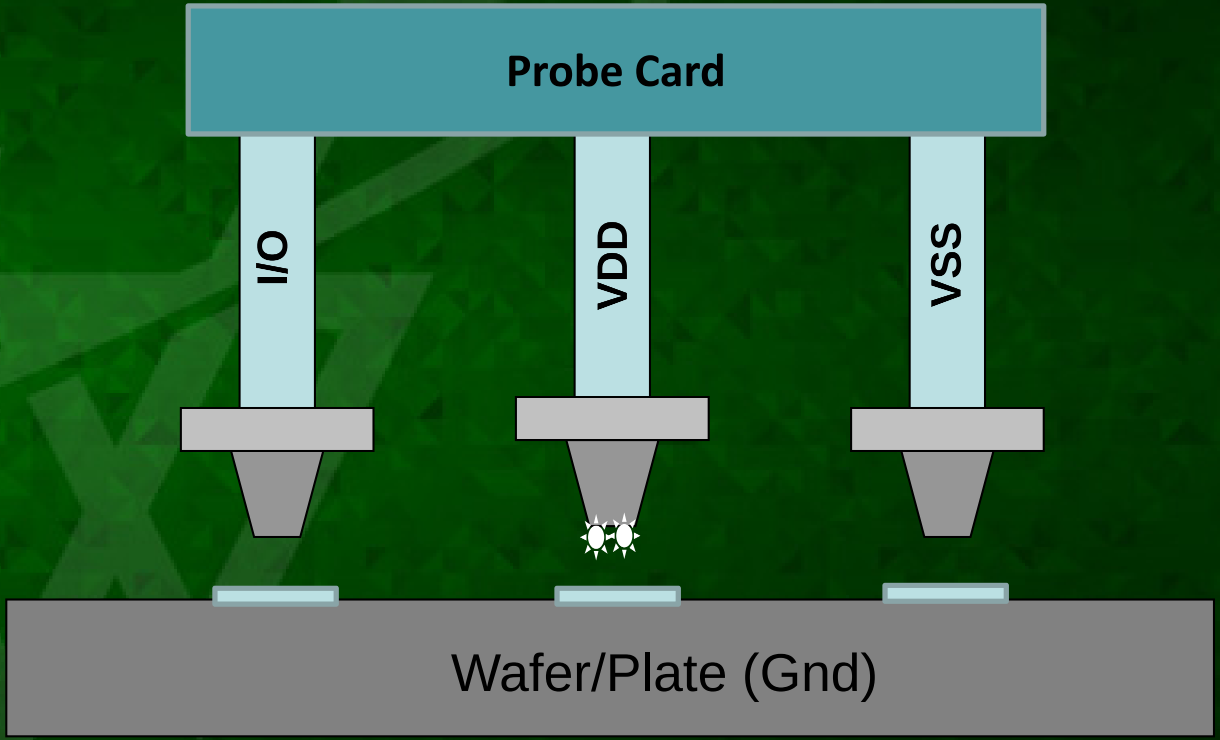
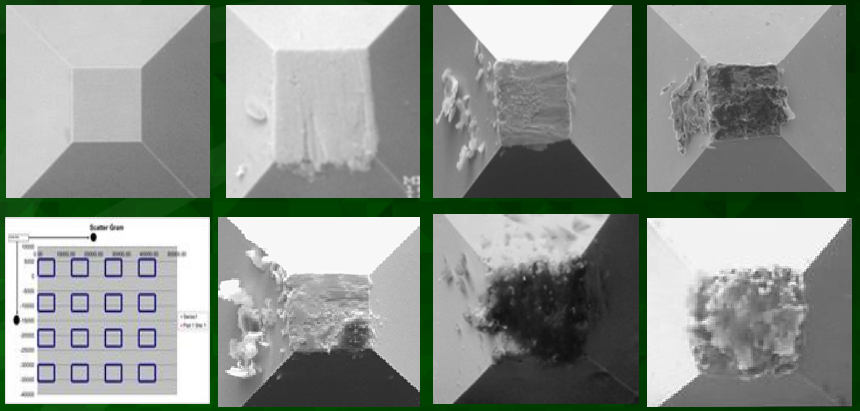


SEM pictures and drawings from FFI et al.

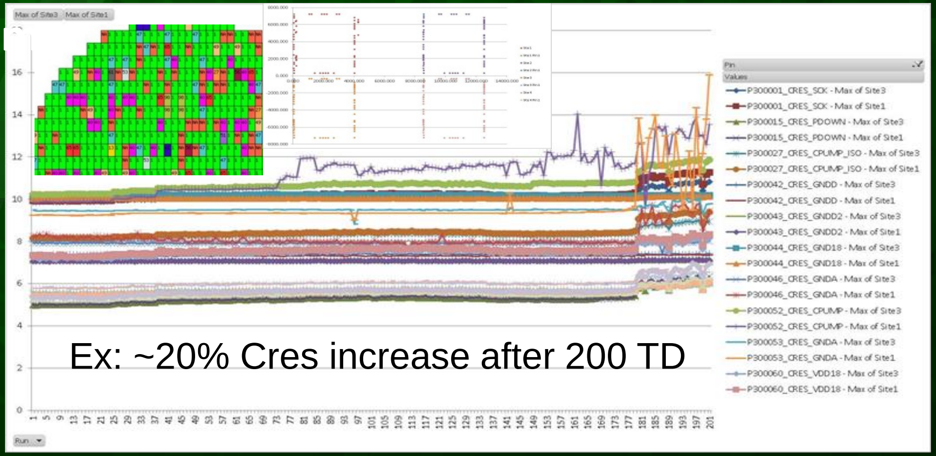
Cause and Effect of Micro-arcing

- **Micro-arcing/hot-stepping symptoms in production testing:**
  - Initially, yield loss and damage may not be apparent or easy to detect specially on high pin count probe card designs.
  - Damage is accumulative and depending on frequency and severity noticeable effects may require a considerable amount of events.
  - First noticeable effects will typically correlate with functional and/or Cres sensitive failures.
  - After many repeated events and damage, gross Cres and/or continuity failures will start to appear.
  - Ultimate accumulative damage will likely require probe tip replacement or probe card rebuild.

SEM pictures from FFI et al.



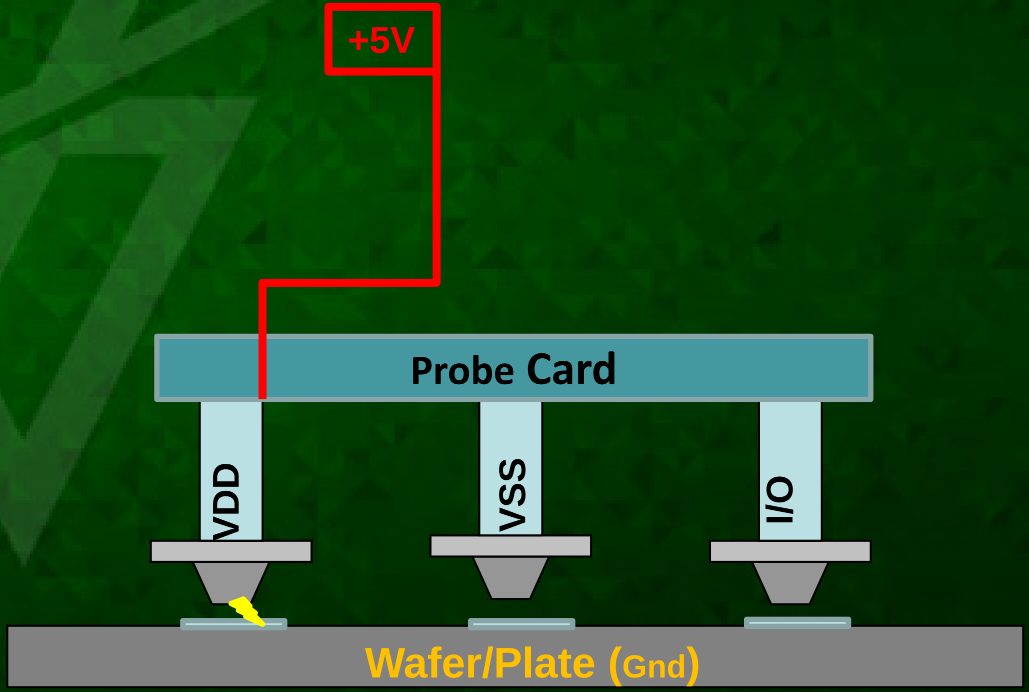
Accumulation of debris and non-conductive



Cres increase over time with hot-stepping

Cause and Effect of Micro-arcing

- **Possible Sources and Conditions for Micro-arcing:**
  - Probe card stepping with active voltage or power on.
    - No power down at End of Flow (EOF) or after a specific failure condition, such as continuity, functional or stress.



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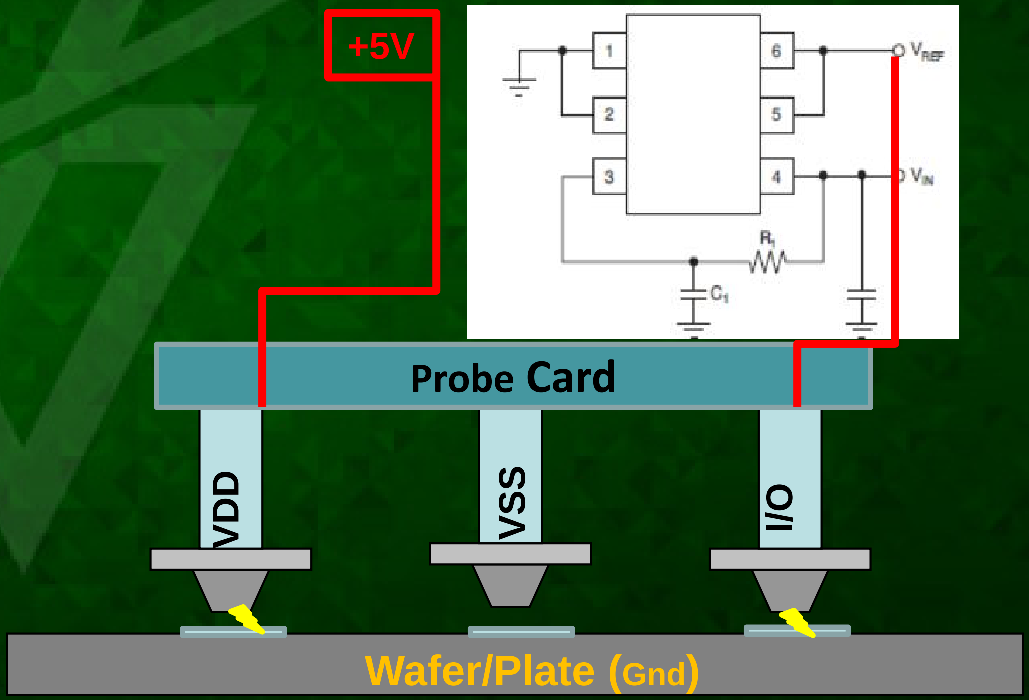
  - Probe card tips connected to a tester resource(s) or component in unknown state at EOF.
    - Power supply pin disconnected or resource disabled before powered down.
    - Pin connected to IC output with inputs left in a floating/unknown or 'on' state.



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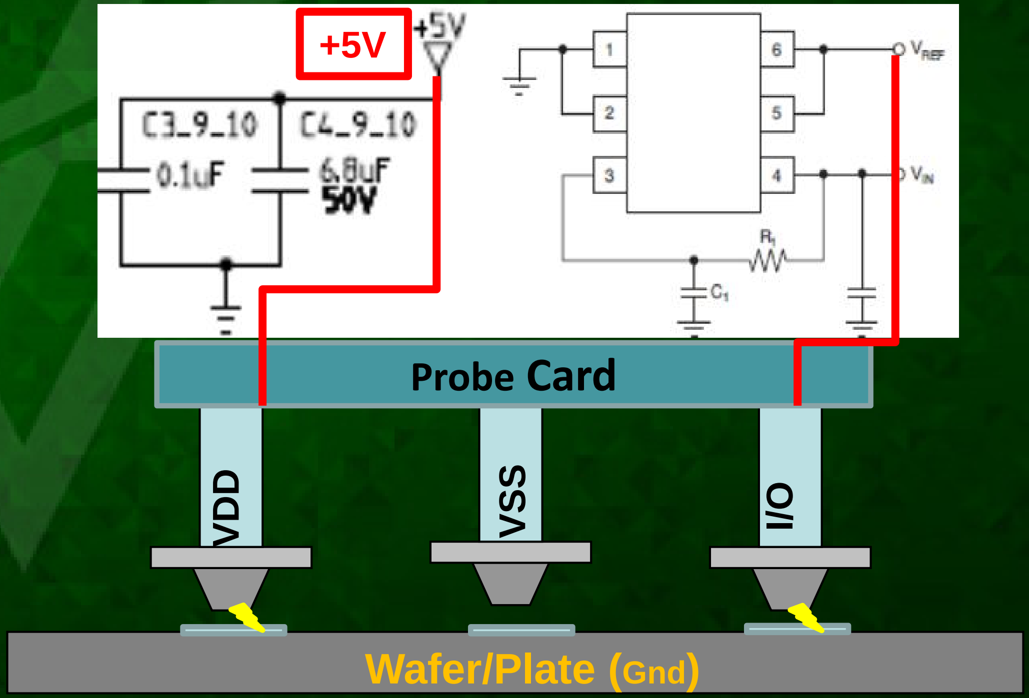

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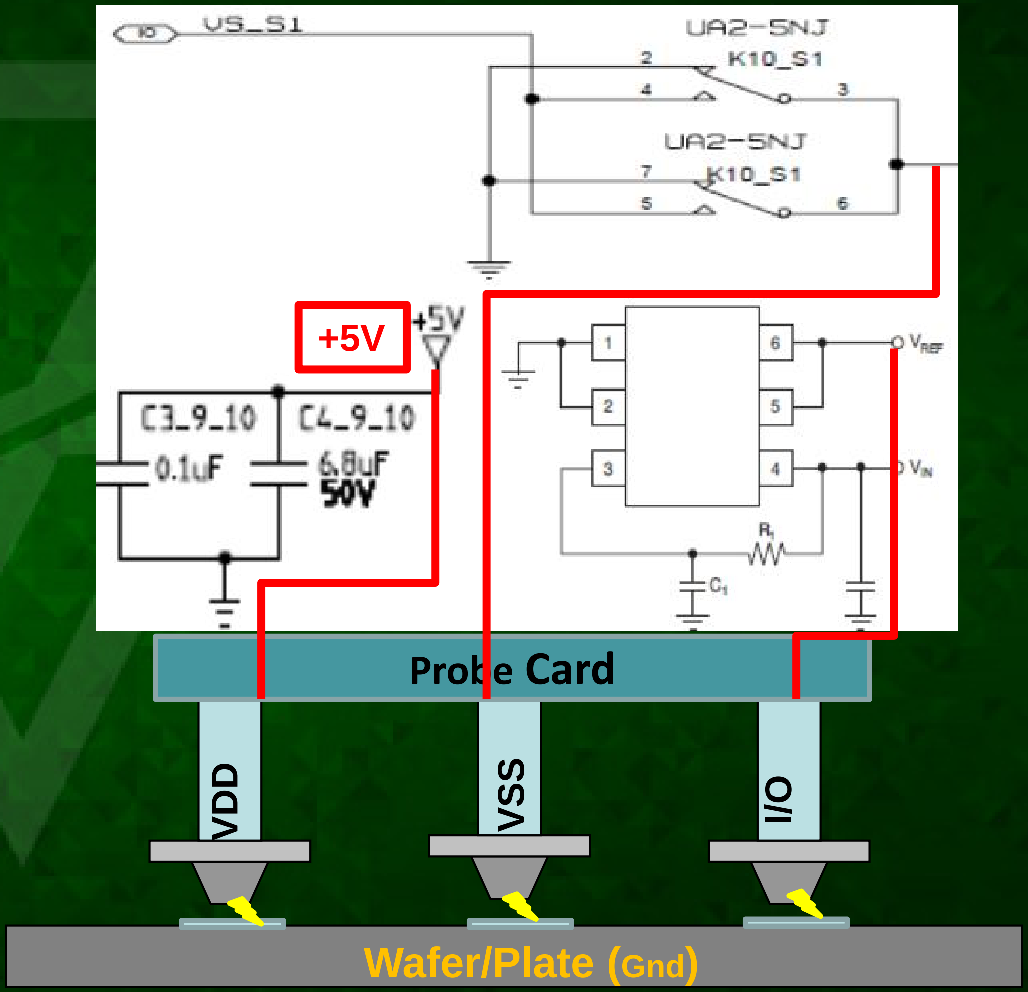
  - Incorrect activation/deactivation sequence for active components such as relays or buffers.



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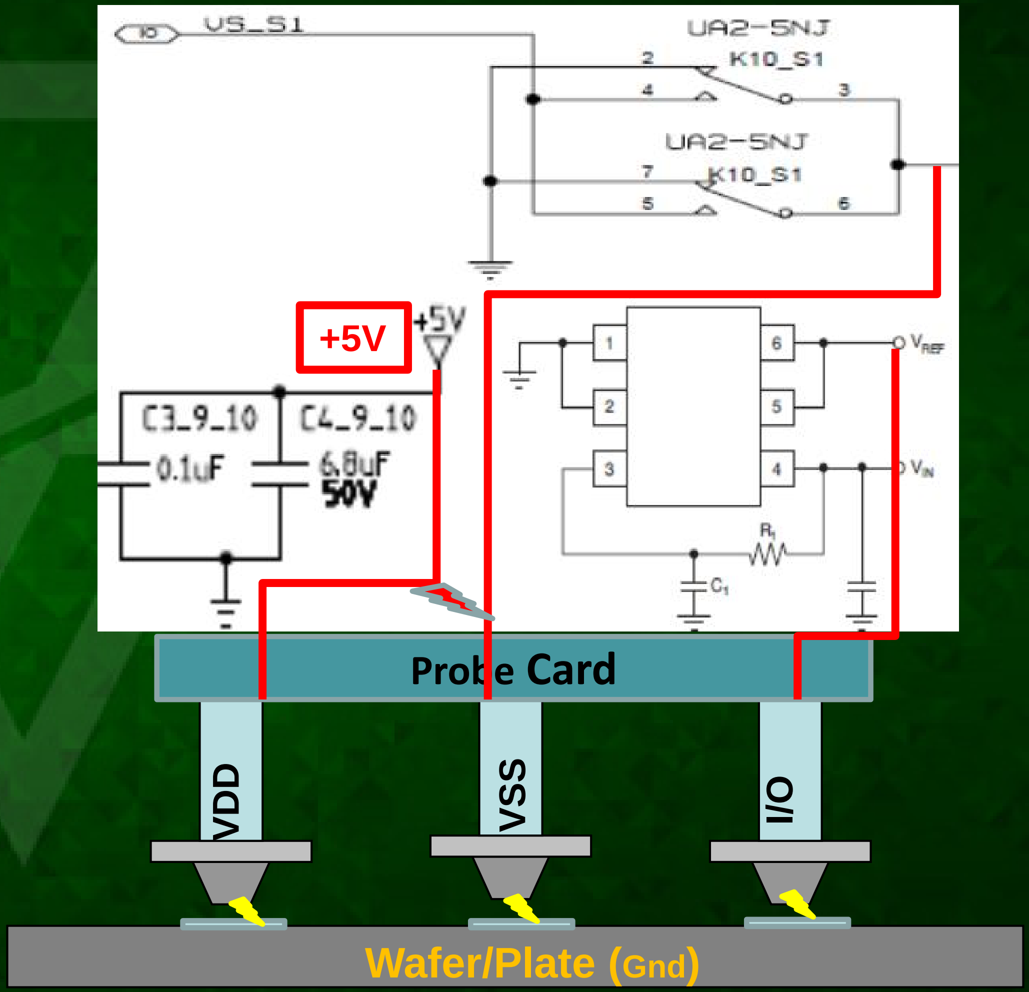
  - Probe card tips connected to a charged capacitor component(s) at EOF.
  - Incorrect activation/deactivation sequence for active components such as relays or buffers.
  - Faulty trace(s) or active/passive component(s) causing a short to a voltage source.



Prevention Methods

- **Micro-arc/Hot-stepping Prevention Steps Summary:**
  - Ensure tester resources are powered down at EOF.
    - Applies to both passing and failing conditions (Good Bins & Fail Bins)
    - Applies to enabled and disabled sites.
  - Ensure active component(s) are powered down and in known state at EOF.
  - Ensure capacitors involved are completely discharged at EOF.
  - Ensure correct activation/deactivation sequence for active components such as relays/buffers.
    - Relays may need to remain closed before discharging capacitors.
  - Ensure correct activation/deactivation for sites to ensure a valid discharge and power down sequence.
  - Ensure proper physical probe tip contact (CRES) and cleaning process.
    - Per Keithley et al “Improper contact or contamination on the probe tips can cause arcing and turn a probe tip into a mini arc welder”

Detection Methods

- Once prevention methods are in place it may still be difficult to verify the source and implement a fix.
- Often times it will require more than one program iteration to ensure symptoms are eliminated or improved.
- One good way to ensure preventions are in place is to implement a real time measurement monitor routine for probe tips throughout one full cycle of a normal test operation.

Level Detection Method

Level Monitoring Routines:

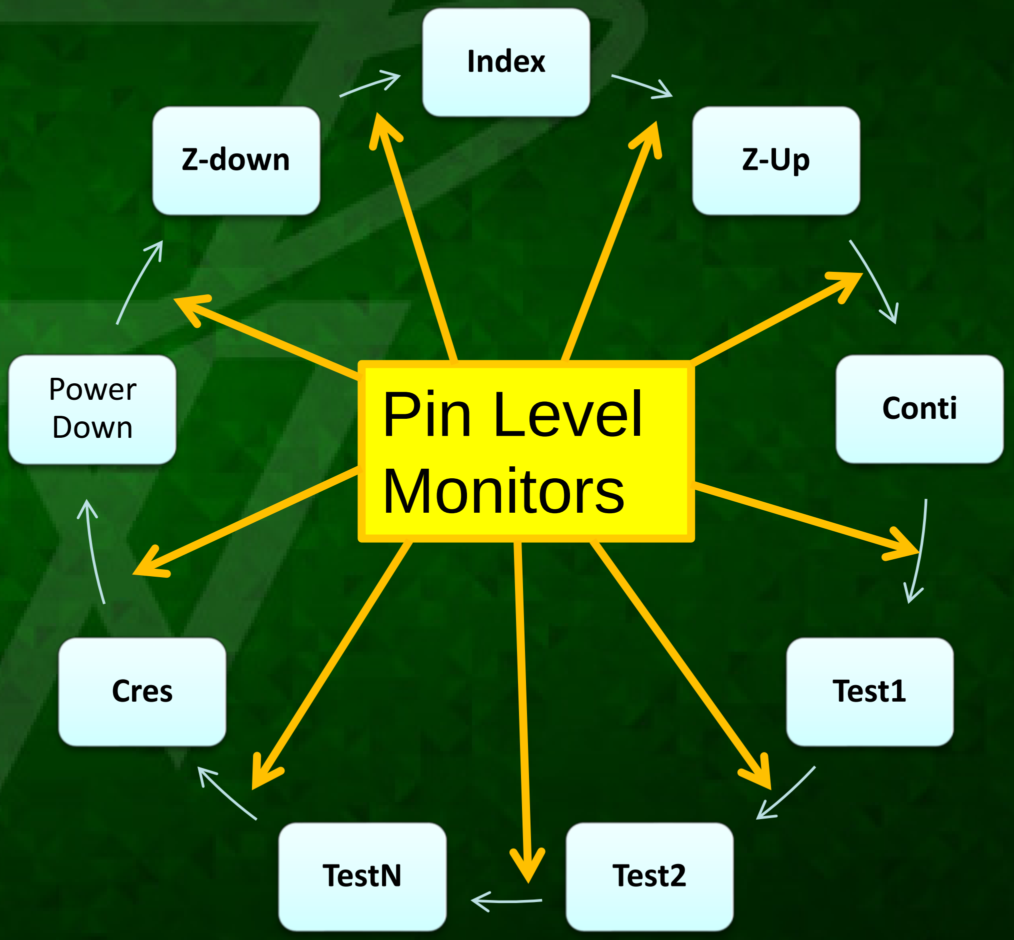
Measure voltage levels at Digital/Analog channels and Power Supplies at following points within program flow:

- After Index before Z-up
- After Z-Up touchdown
- After Continuity
- After each subsequent test.
- After End Of Flow (EOF)
- After Z-down

Things to look for:

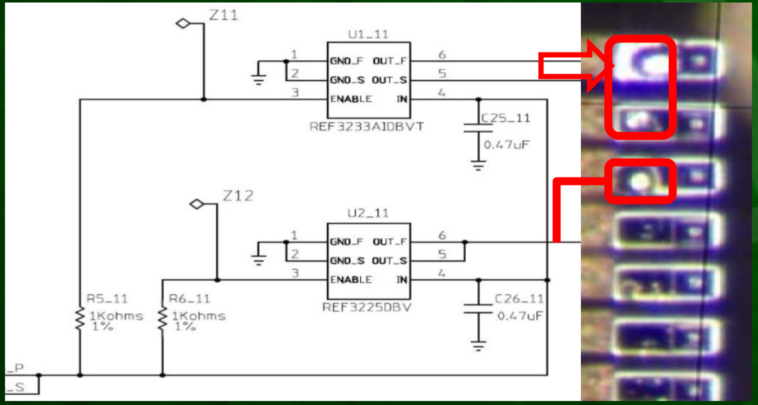
- I/O, Analog, MS, Power Supplies >0.2V at all these locations.
- Tester I/O States to known level before touchdown (TD).
- Auxiliary IC Buffer I/O States to Known level before TD.

Full Die Probe Cycle

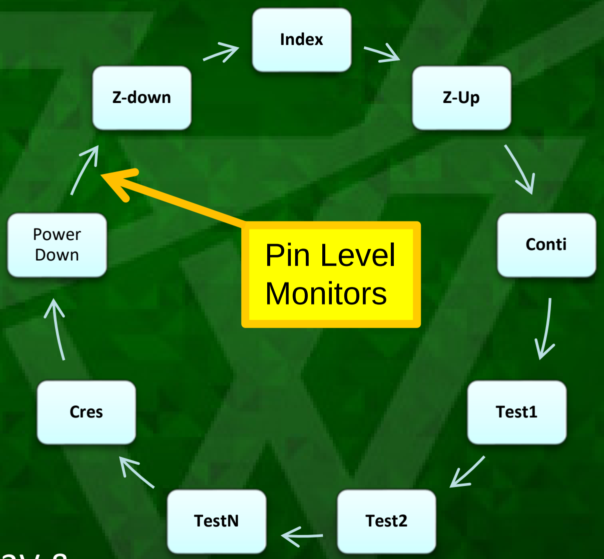


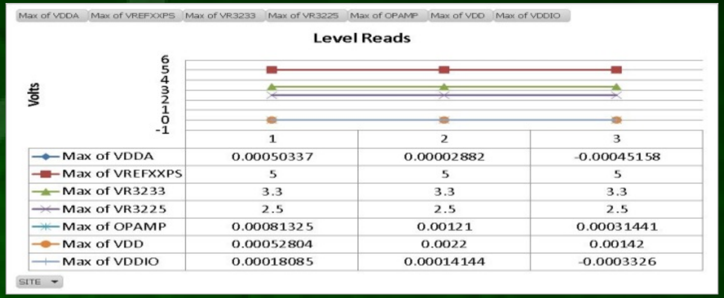
Results

- **Test Case #1:**
- **Device suffered from yield stability problems including Cres/Continuity failures & Prober misalignment failures**
  - Upon probe card visual inspection found blobs build-up on side of probe tips.
  - Probe tips affected were connected to voltage reference active components.



  - Added Monitor Routine at EOF and found some pins keeping ~3.3V & 2.5V due to PS on Volt Reference IC left on and not mapped to a site
  - Fixed by mapping Ref32xx PS (or Enable pin) to each site allowing power down by site.

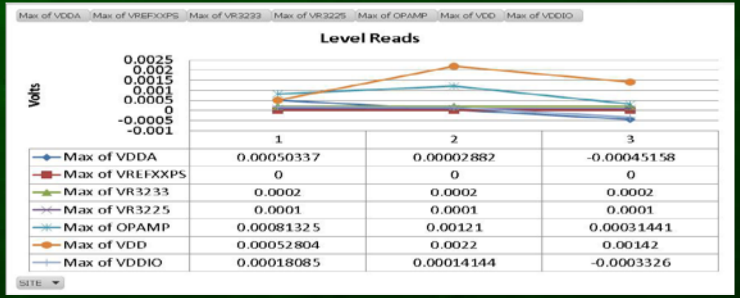




	1	2	3
Max of VDDA	0.00050337	0.00002882	-0.00045158
Max of VREFXXPS	5	5	5
Max of VR3233	3.3	3.3	3.3
Max of VR3225	2.5	2.5	2.5
Max of OPAMP	0.00081325	0.00121	0.00031441
Max of VDD	0.00052804	0.0022	0.00142
Max of VDDIO	0.00018085	0.00014144	-0.0003326

Monitor Levels Before Fix:

VREFXXPS~5V, VR3233~3.3V & VR3225~2.5V @ EOF



	1	2	3
Max of VDDA	0.00050337	0.00002882	-0.00045158
Max of VREFXXPS	0	0	0
Max of VR3233	0.0002	0.0002	0.0002
Max of VR3225	0.0001	0.0001	0.0001
Max of OPAMP	0.00081325	0.00121	0.00031441
Max of VDD	0.00052804	0.0022	0.00142
Max of VDDIO	0.00018085	0.00014144	-0.0003326

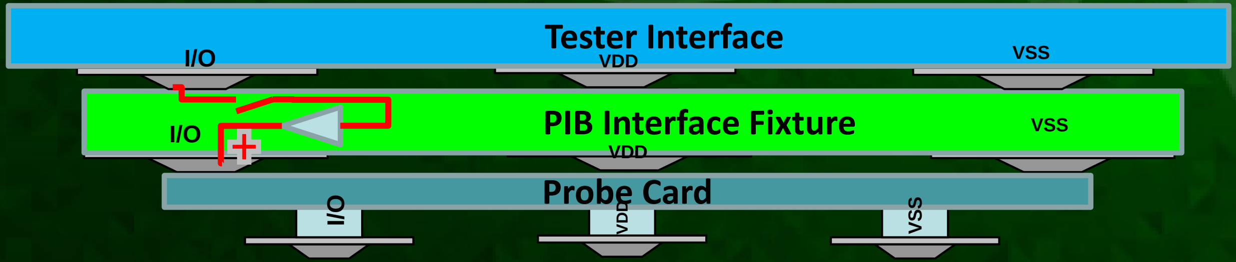
Monitor Levels After Fix:

VREFXXPS~0V, VR3233~0V & VR3225~0V @ EOF

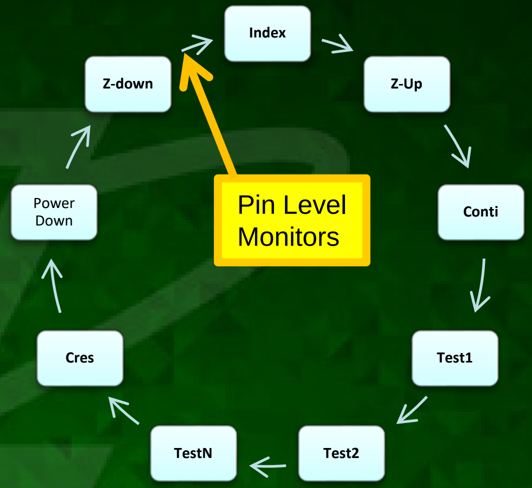
Results

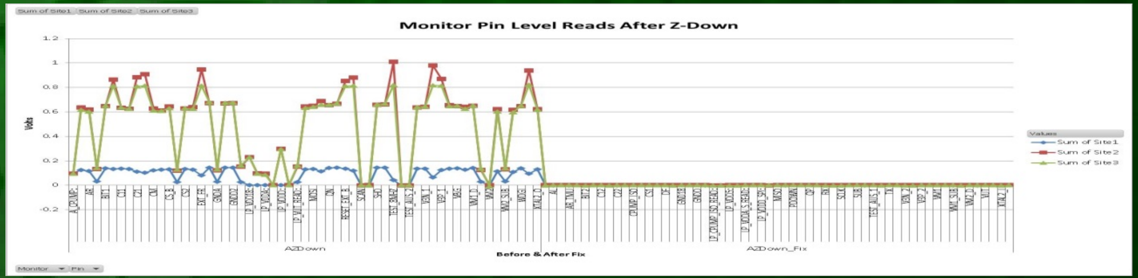
- **Test Case #2:**
- **Device suffered from yield stability problems including premature contact sensitive failures.**
  - Upon probe card visual inspection found debris build-up on needles causing functional and Cres failures requiring frequent offline cleaning.

  - Probe tips involved were connected to tester digital channel resources.
  - Added Monitor Routine for all pins including I/O's at the end of every test case and found several digital pins measuring up to ~1V after Z-down event.
  - Found interface fixture with active IC inputs left in a floating/un-known state.

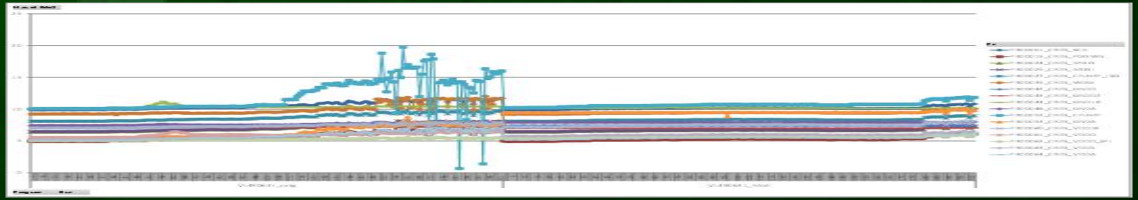


  - Added a provision to keep these levels low until next touch down and that resolved this problem.





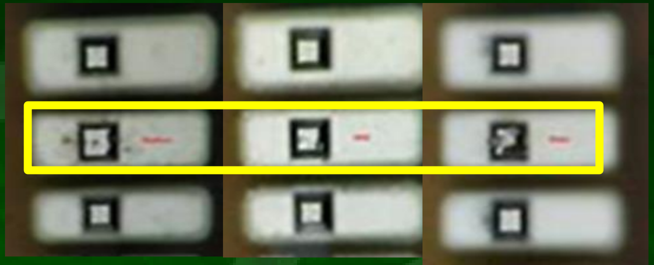
Monitor Levels Before and After Fix



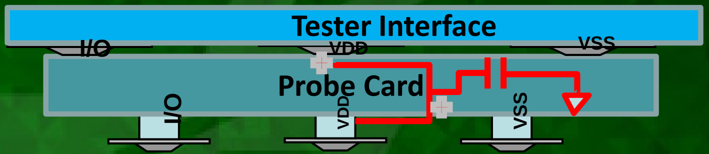
Cres Reads Before and After Fix

Results

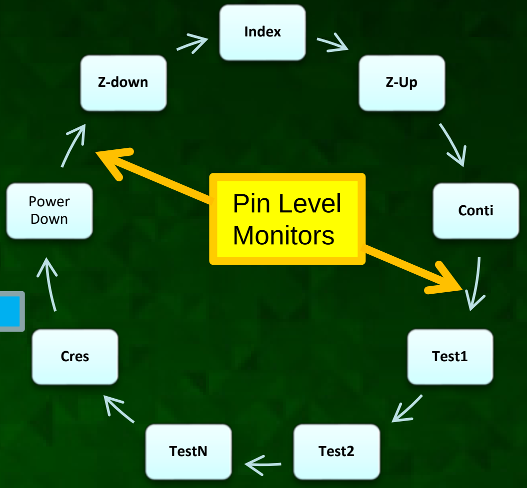
- **Test Case #3:**
- **Device Premature Continuity failures & Card Required Probe Tip Replacement after regular prolonged use.**
  - Upon visual inspection found one PS pin being damaged by Micro-arcing with evidence of craters and pin alloy missing causing premature continuity failures after a prolonged continuous use (Ex: One Month).
  - Main Probe tips involved was single pin Power Supply connected to a 4uF decoupling capacitor.
  - Added Monitor Routine for all PS pins at end of every test and found PS involved measuring ~1V at EOF when failing continuity.
  - Found power down routine not having enough current and discharge times for this power supply after a continuity failure, thus, leaving ~1V charge on this pin after an Open failure.
  - Added correct amount of discharge time and current.
  - After fix, reads for all PS pins on a production run sample did not show voltage spikes at EOF for any bin conditions and levels below <6mV.

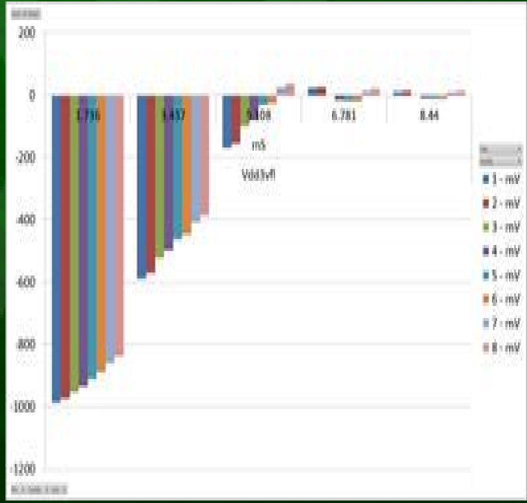


Progressive Damage Show on Single Pin PS

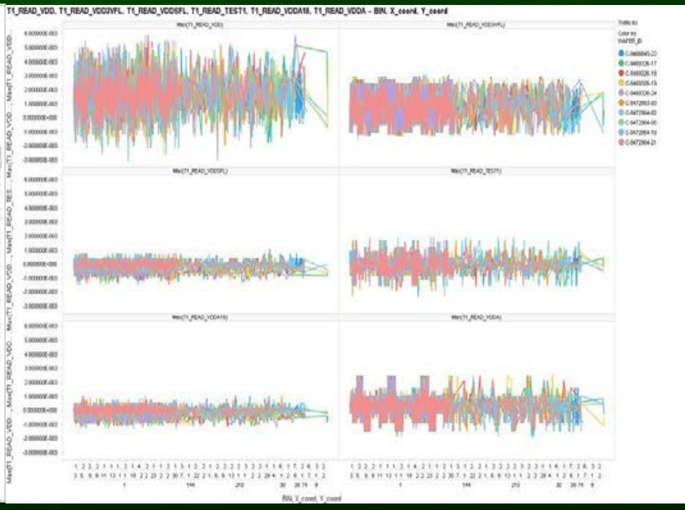


4uF Cap on PS showing damage (@~1V)





PS Level Reads Before Fix (~1V)



PS Level Reads After Fix (All <6mV)

Summary

- Eliminating Micro-arcing from the probe process can be challenging, however, following best programing practices, applying good logic to the problem the effects can be mitigated.
- The use of a monitoring routine for the detection is an effective tool to pinpoint the source of the problem and help find a resolution.
- Seeing real time measurements tabulated on a chart helps visualize the location of the problem and search for the right solution even under a complex test flow process.

Acknowledgements

- Imran Ahmed (EE)
- Sid Gibson, Gary Grayson (Apps)
- Dan Stillman, Connie Smith, Doug Shuey (Probe Cards)
- Brennan Tran, Vincent Ellis (Probe Cards)

References

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Discussion/Questions

Thank you!