SWTEST

PROBE TODAY, FOR TOMORROW

A Technique of Embedding Protection Resistors inside LTCC Substrate using Space TransFormer

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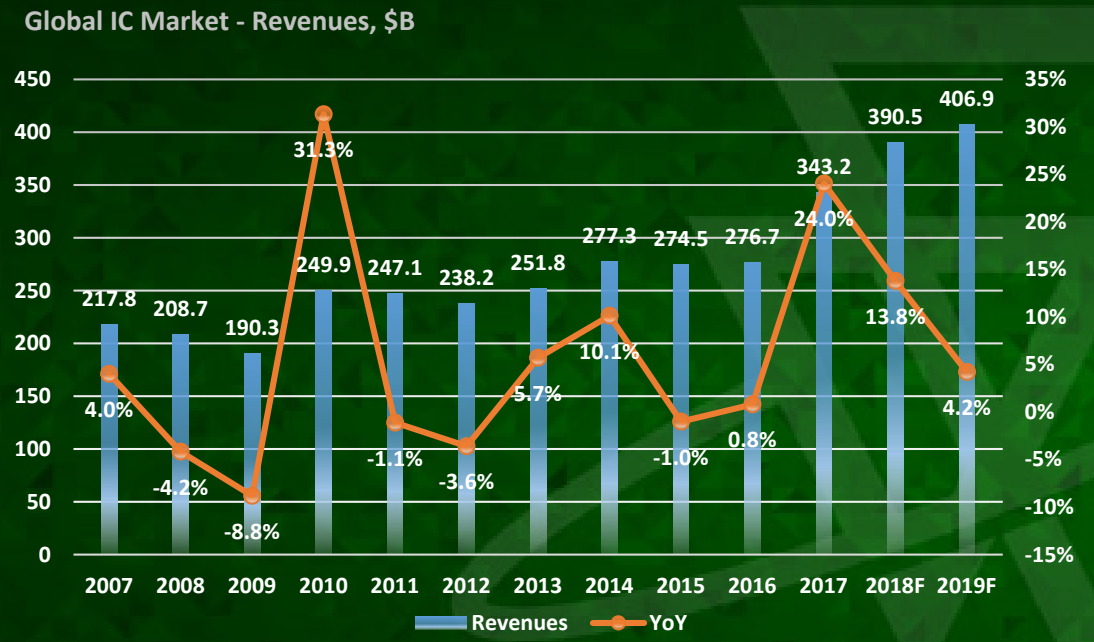
Overview

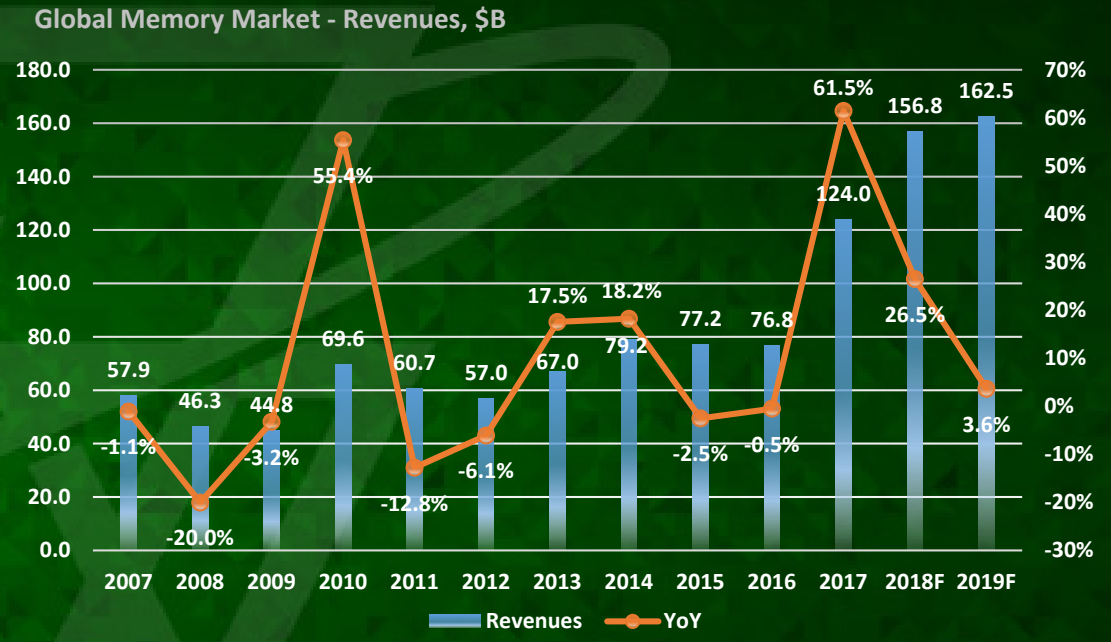
- Trends of Probe Card
- High Parallelism for Probe Card
- Introduction of Protection Resistor
- Research and Evaluation of Protection Resistor
- Measurement and Analysis for Protection Resistor
- Summary
- Future Works

Trends of Probe Card

- **Global Semiconductor Market**



Source : Shared Research based on WSTS data(2018)



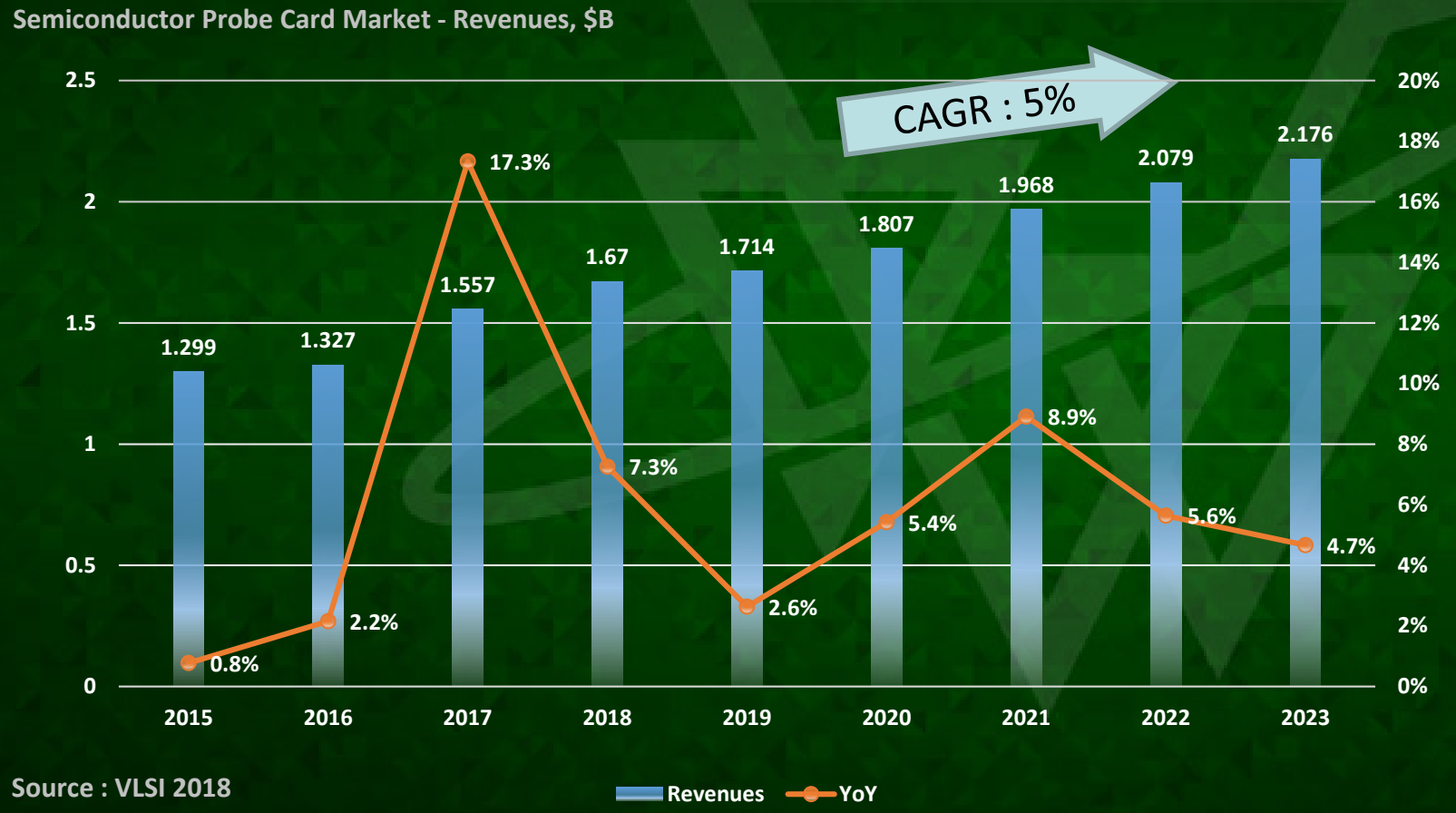
Source : Shared Research based on WSTS data(2018)

- IC market flat in 2015–2016
- Upturn 24% YoY to 343.2B$ in 2017
  - Economic recovery & expansion in automotive market
- Weakening growth until 2019

- Memory market Stagnation in 2015-2016
- Market Changed 61.5% YoY to 124.0B$ in 2017
  - Smartphone, server/data center equipment and SSDs

Trends of Probe Card

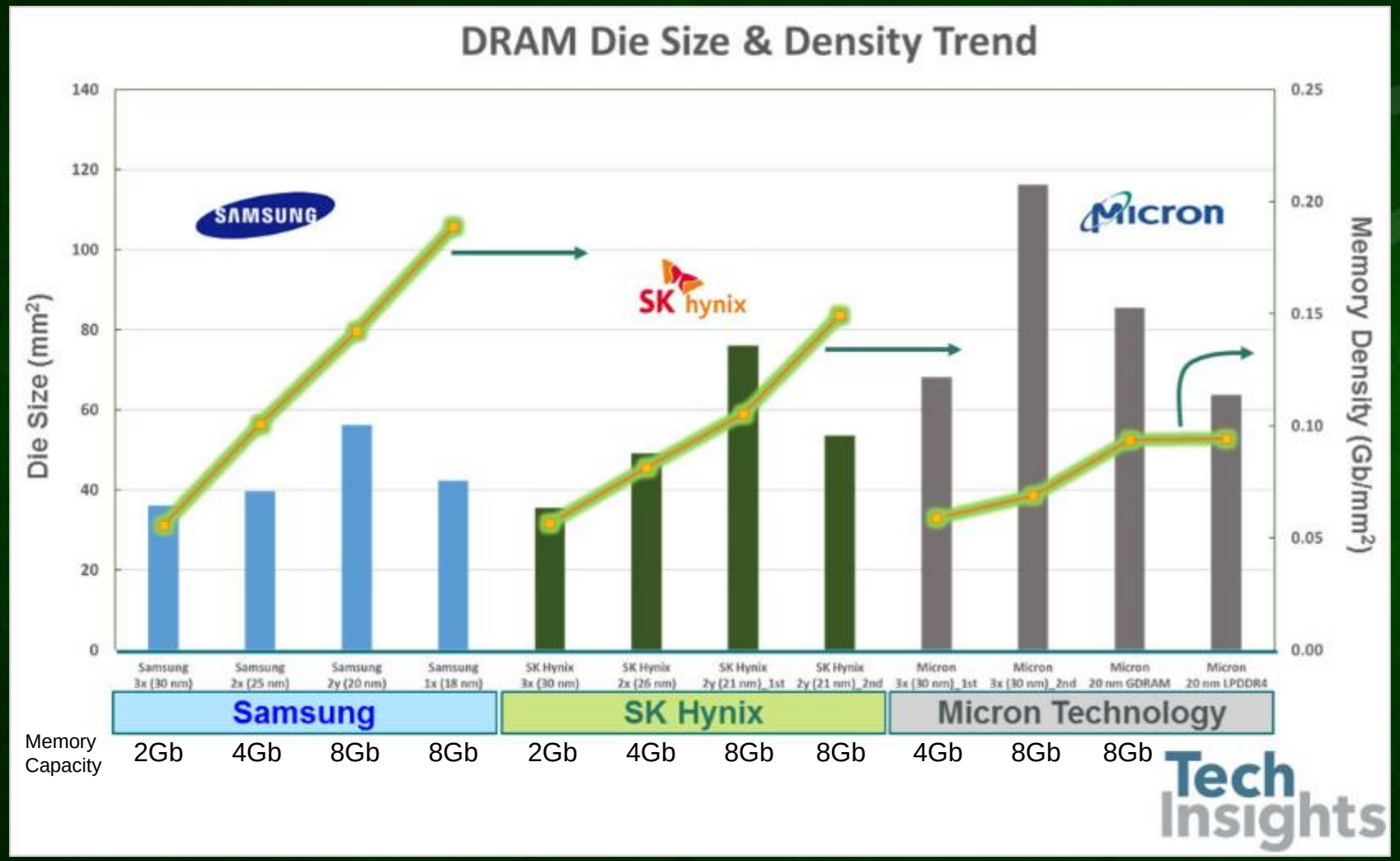
- **Global Probe Card Market**



Source : VLSI 2018

- Increased P/card Revenues In 2017
  ➔ IC & Memory Sales ▲
- Steady increase trend of CAGR 5% since 2017
- Need to Check Growth after 2019

Trends of Probe Card



Fab node ▼

Memory Density ▲

Die Size (@ Same Capacity) ▼

Chip Count per wafer ▲

Parallelism of P/Card ▲

High Parallelism for Probe Card

- **DRAM Probe Card Features**
  - Over 1,000 DUTs
  - Over 100,000 Probes
  - Over x10 Shared
  - Fine Pitch Pad Probing (under 60um)

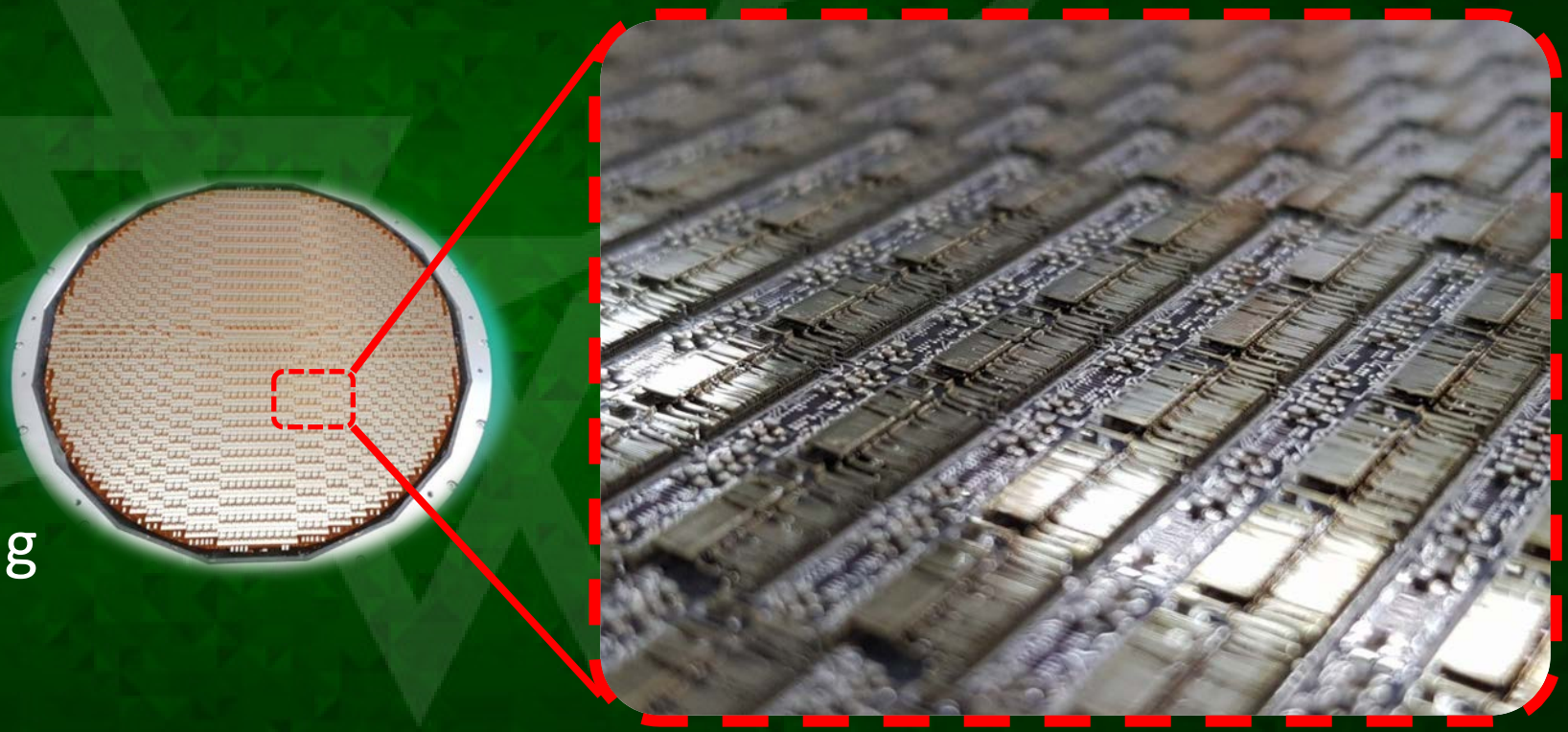


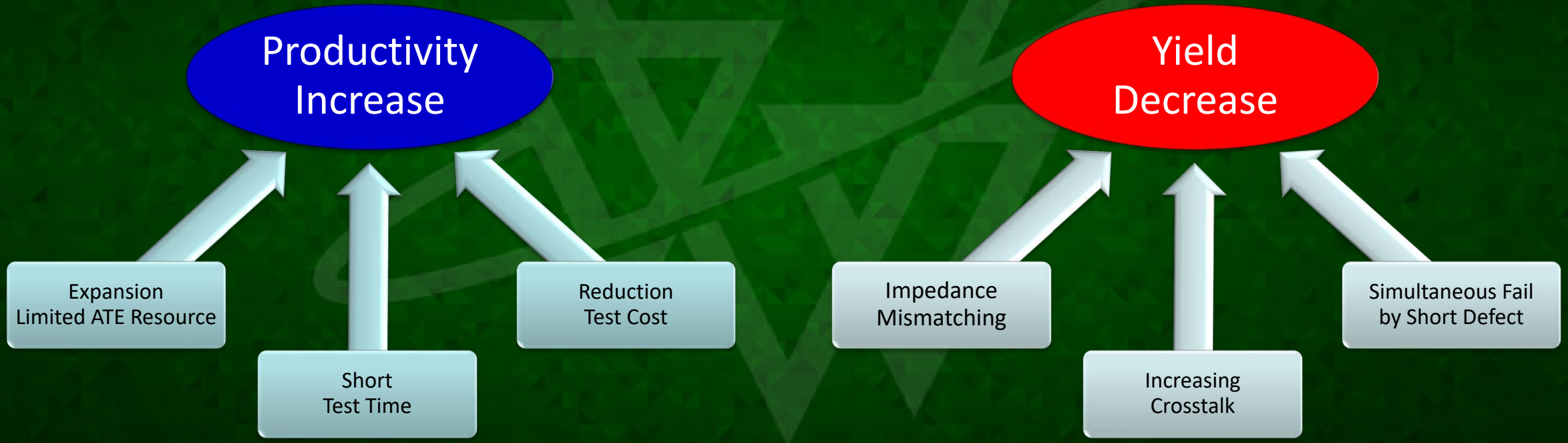
Fig. Probe Card for DRAM

High Parallelism for Probe Card

- **Customer Requirement**
  - Electrical Performance
    - Signal Integrity
      - Impedance Control
      - Time of Propagation Delay Matching
      - Differential Pair Trace Matching
      - Multi Shared Channels Routing
    - Power Integrity
      - Low Power Impedance Control
      - DC Trace Resistance
      - Current Carrying Capacity
      - Leakage Current Control
  - Mechanical Performance
    - Probe Contact
      - Force Uniformity
      - Position Accuracy
      - Planarity
      - Scrub Mark in Hot/Cold Temp.
      - Wearing Robustness
      - Depress / Broken
      - Tip Shape Uniformity
    - Stiffener Structure
      - Thermal Deformation
      - Strong Stiffness

High Parallelism for Probe Card

- **Multi Shared Channel Test**
  - Pros and Cons



Introduction of Protection Resistor

- **Role of Protection Resistor**
  - Short Defect Isolation by Protection Resistors at shared Channel

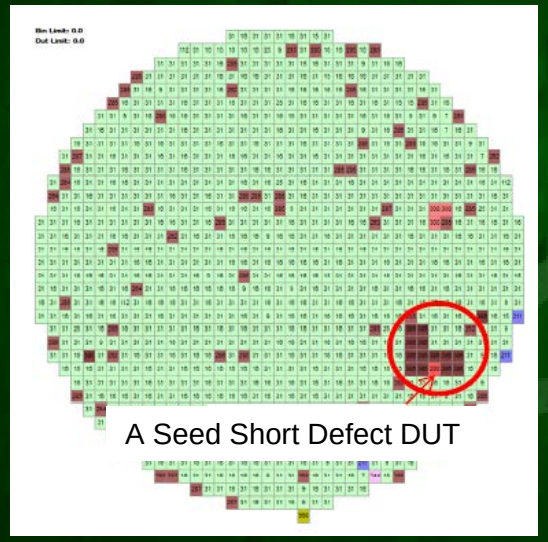


Fig. Wafer Test Result

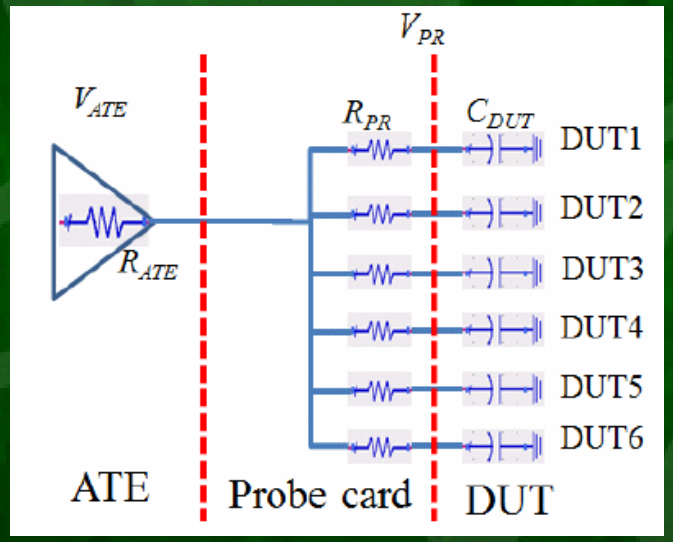


Fig. Circuit of Shared Channel

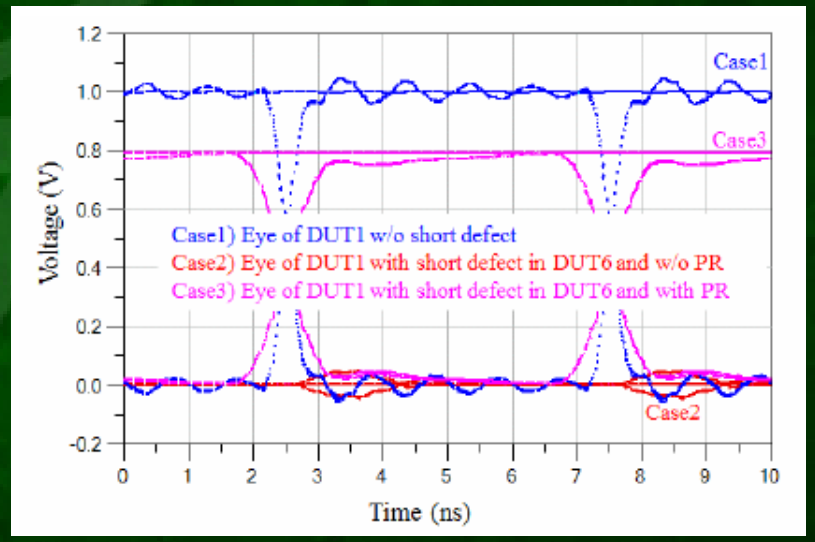
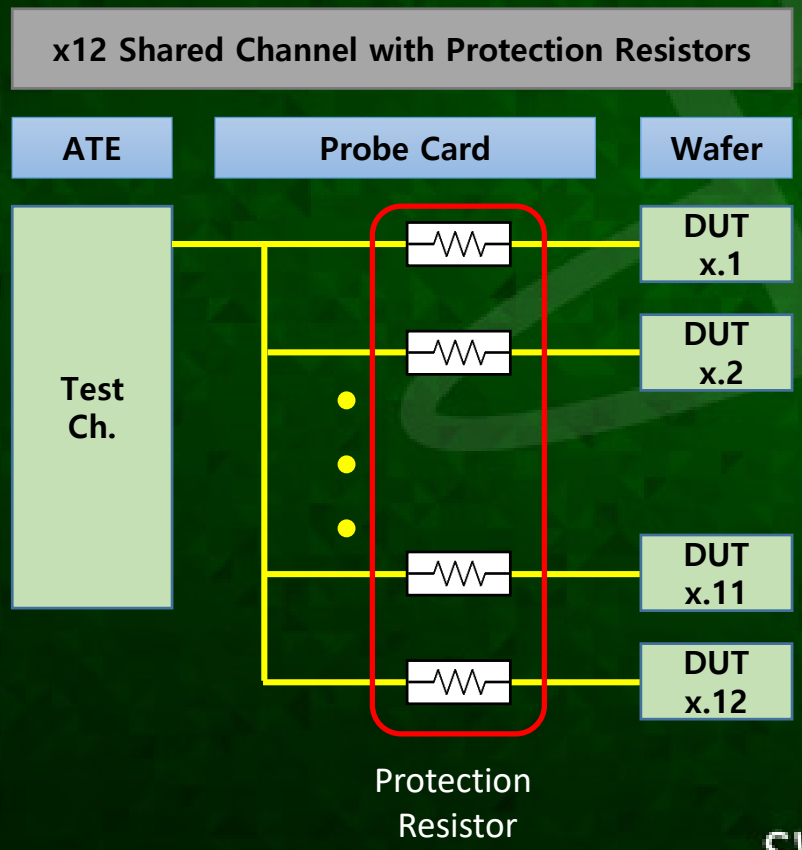


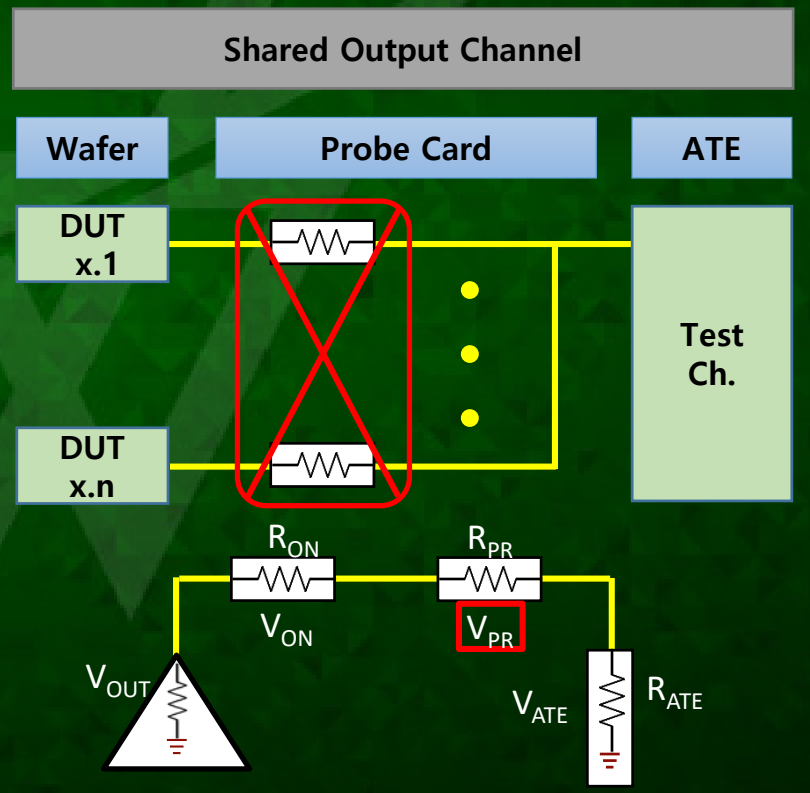
Fig. Output Simulation Result

Source : G. Kim and W. Nah, "NAC Measurement Technique on High Parallelism Probe Card with Protection Resistors", Journal of Semiconductor Technology and Science , VOL.16, NO.5,

Introduction of Protection Resistor

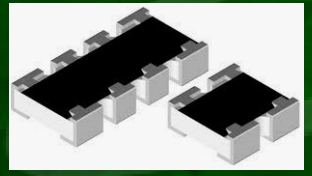
- **Recommended Channel to Use Protection Resistor**
  - Recommended Channel
    - Only Input Shared Channel
  - Restriction Channel
    - Output Channel include I/O



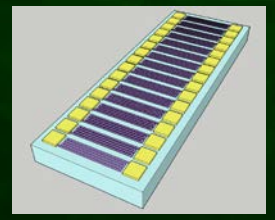


Research and Evaluation of Protection Resistor

- **Types of Appropriate Protection Resistor**
  - Surface Mount Resistor on Substrate
    - Need to Packaging Area, Time and Cost
    - Highly Resistance Accuracy and Various Value
  - Types
    - Lumped Resistor

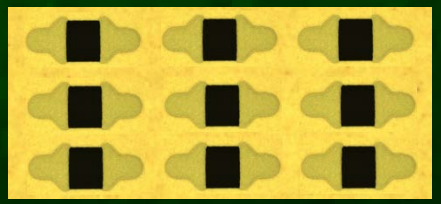



    - Thin Film Array Resistor Module



  - Embedded Resistor in Substrate
    - No Packaging Area on the Substrate with over 100K pins
    - Inaccurate Resistance and Low Resistance
  - Types
    - Thin Film Resistor on Polyimide


    - Thick Film Resistor on Inner Ceramic

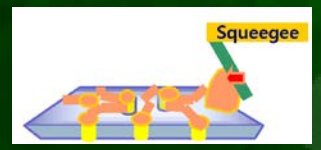


Research and Evaluation of Protection Resistor

Embedded Thick Film Resistor

- **Feature**
  - Similar Processing like a Lumped Resistor
  - Using LTCC(Low Temperature Co-fired Ceramic) Process for Making Embedded Resistor

Printing Resistor paste



Collating

Sintering

LTCC STF with Resistors

Source : SEMCNS

- **Advantage**
  - Free Space on the Substrate Surface
  - No Degradation during Post-Processing
    - Machining, Thin Film Process, MEMS, etc.
  - Reduce Cost
    - Post-Processing Fail Cost, Soldering, etc.
- **Disadvantage**
  - Rough Resistance Tolerance between Resistors
  - Un-tunable Resistance

Research and Evaluation of Protection Resistor

- **LTCC Introduction**
  - Low Temperature Co-fired Ceramic
    - Material : Alumina + Glass
    - Firing Temperature : 850 ℃
    - Conductor Metal : Ag, Au, Cu
  - Feature
    - High Conductivity Metal Electrode
    - Low Dielectric Loss
    - Embedded Passive Devices

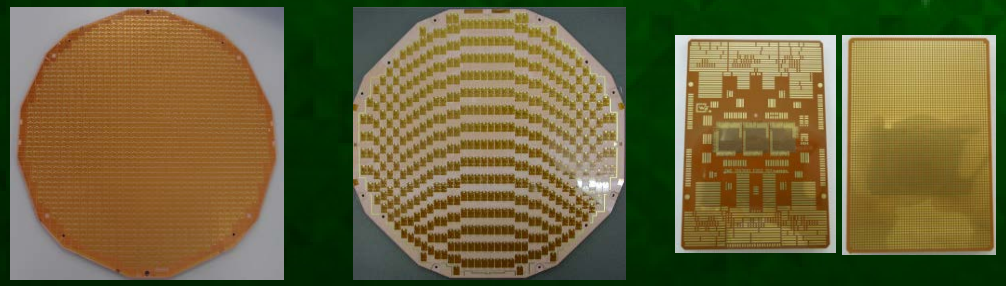


Fig. Space Transformer for Probe Card

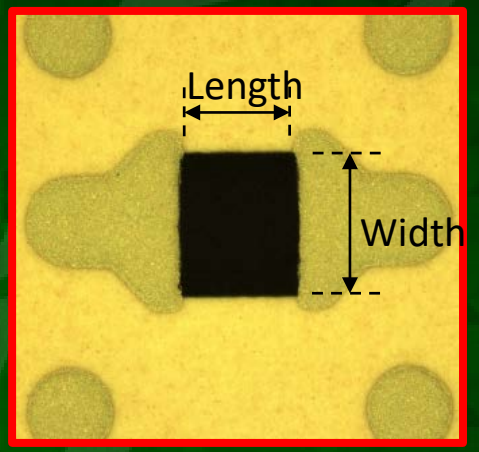
- **LTCC Application**

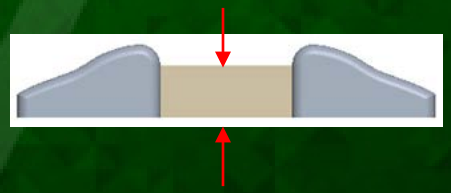
Source : SEMCNS

Research and Evaluation of Protection Resistor

Variable Experiment to Overcome Resistance Tolerance

- **Design Parameter**
  - ① Width & Length
  - ② Width & Length Aspect Ratio
  - ③ Termination Pad Size
- **Process Parameter**
  - ① Paste Printing Thickness
  - ② Printing Direction
  - ③ Lamination Structure

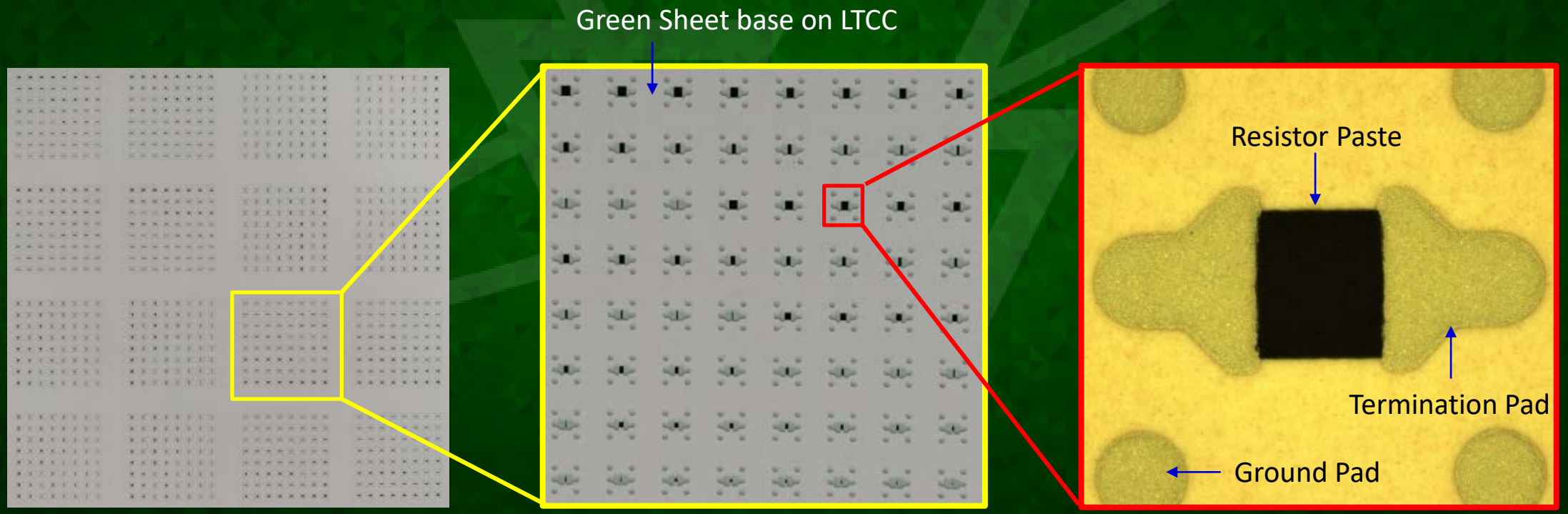




Research and Evaluation of Protection Resistor

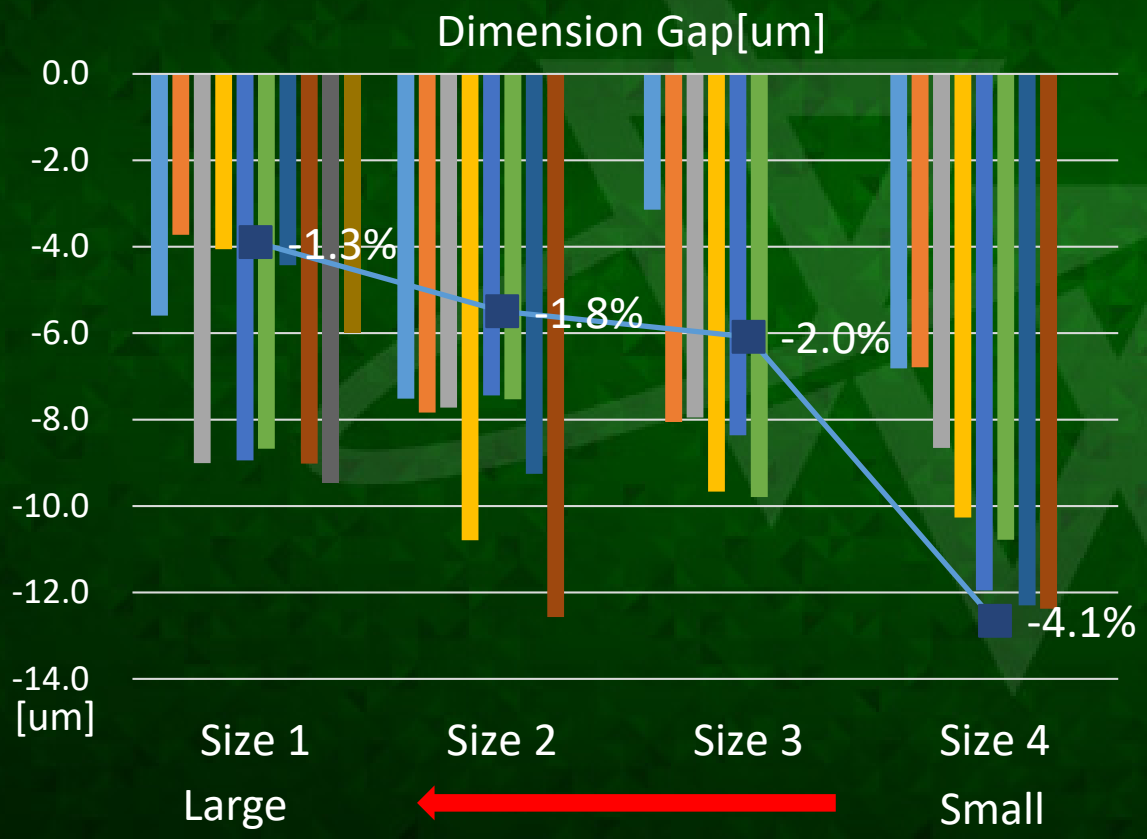
Prototype Test Experiment

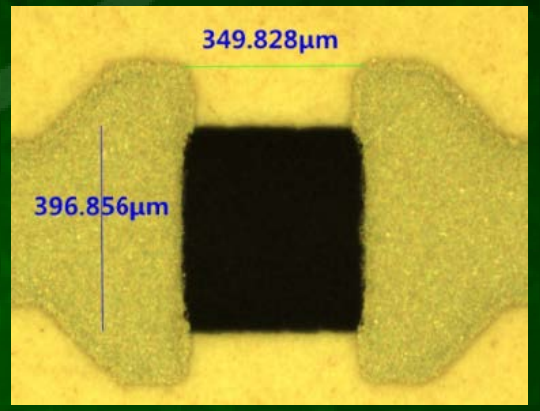
- **Test Vehicle for Fixing the Parameter and Setup the Library**



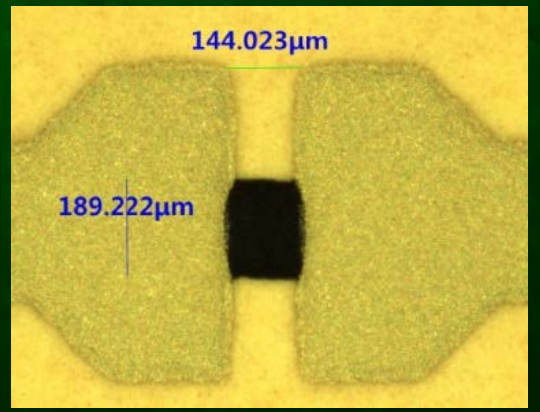
Measurement and Analysis for Protection Resistor

- **Dimension Gap Compared to Design after Printing Process**
  - Process Gap is Similar from above Small Size





350x400um^2 Resistor



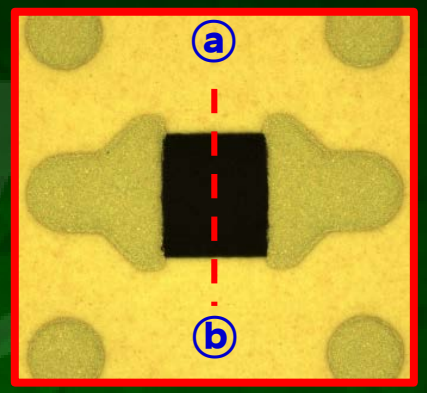
150x200um^2 Resistor

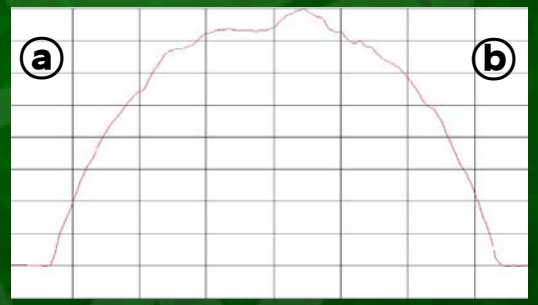
Measurement and Analysis for Protection Resistor

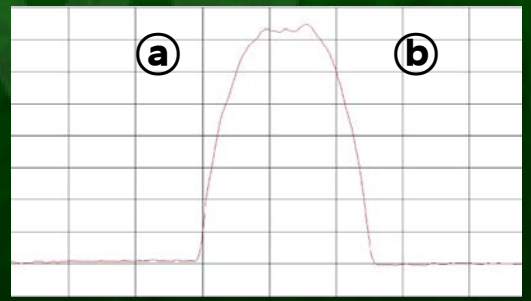
- **Thickness Profile Measurement**
  - Overall Thickness : Constant
  - Side Slope : Depends on Paste Length
    - Vertical Direction

    ➔ Need to Process Control
    - Horizontal Direction

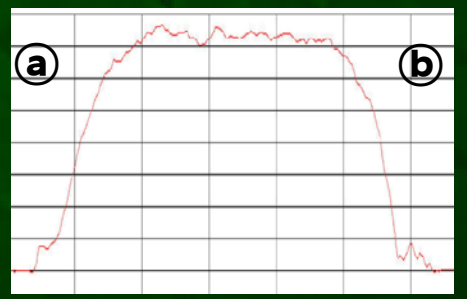
    ➔ Overlap Control of Termination Pad and Resistor Pattern
- **Process Variable Optimization**
  - Control factor
    - Thickness + Flatness
    - Side Slope





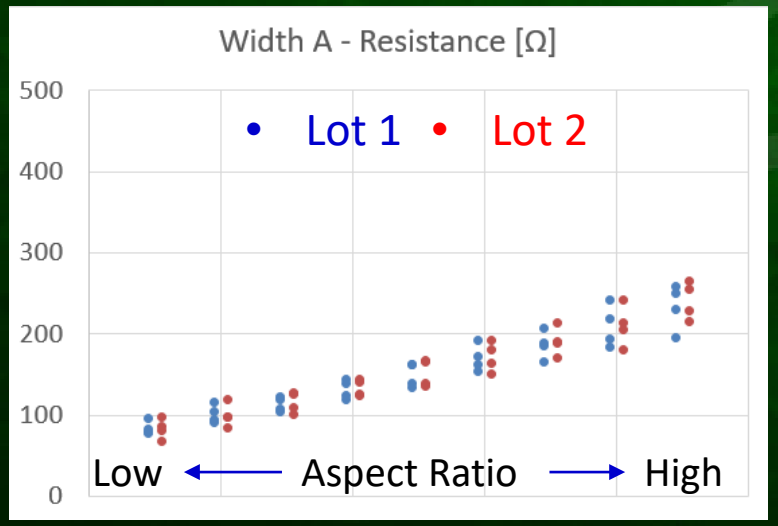


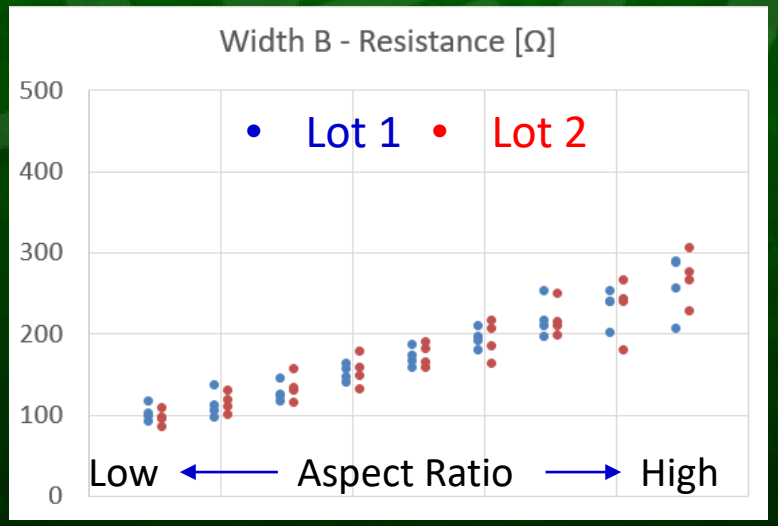
After Optimization

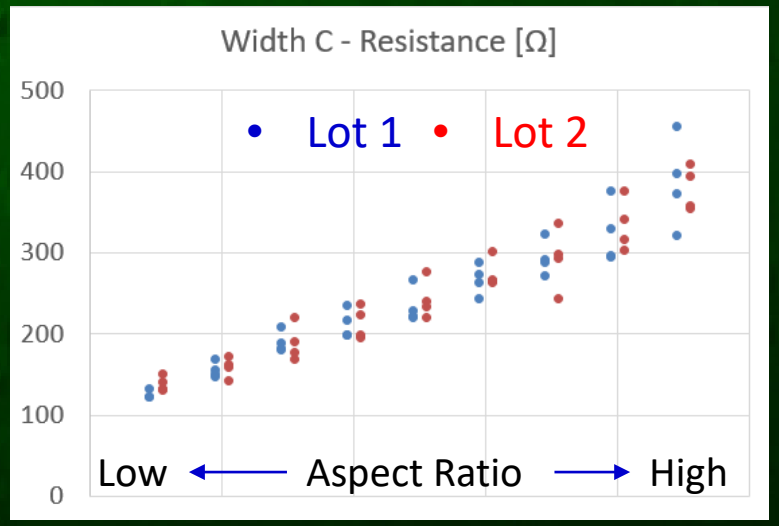


Measurement and Analysis for Protection Resistor

- **Result of Resistance Measurement**
  - Predictable Resistor Value by Aspect Ratio
  - Under ± 20% Resistance tolerance
    - Under ± 15% on Low Aspect Ratio
  - Low Tolerance Level between Lots on Low Aspect Ratio







Measurement and Analysis for Protection Resistor

- **Measurement Setup of Resistor**
  - Network Analyzer : Agilent E5071C
  - Probe Station : DSF System BTE300
  - Probe Tip : Picoprobe ECP18-SG-600
  - Test Sample : 8 Inch LTCC Test Substrate

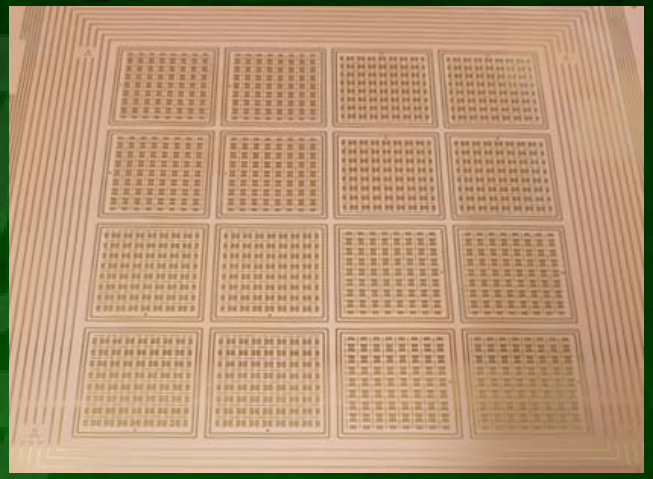


Fig. 8inch LTCC Test Sample

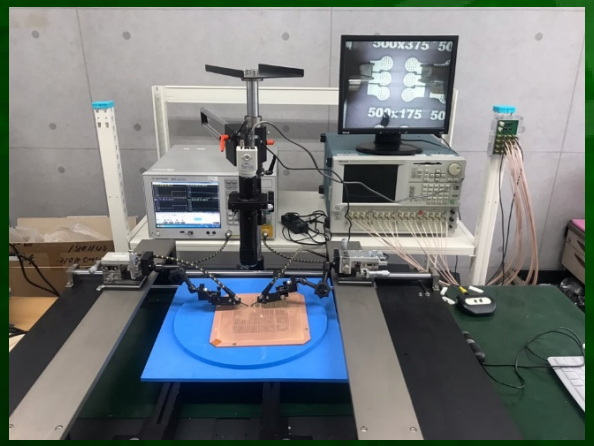


Fig. Measurement System

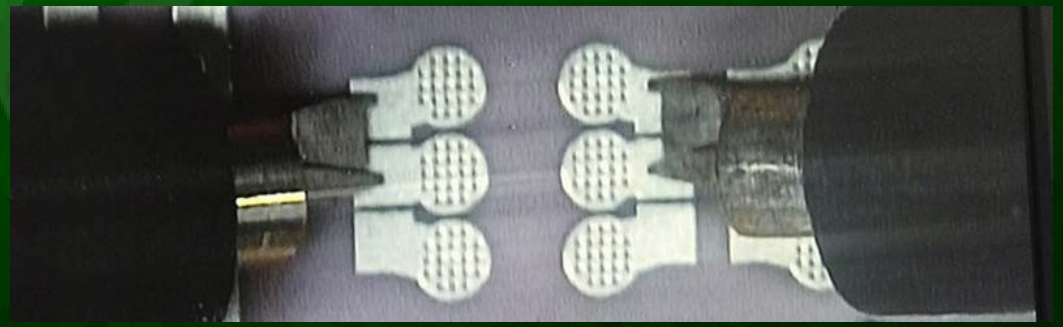
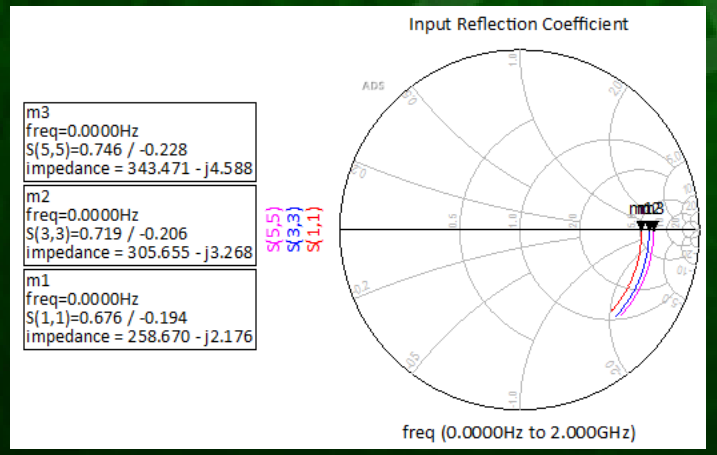


Fig. Probing embedded Resistor

Measurement and Analysis for Protection Resistor

- **Result of S-parameter Measurement**
  - Result of 3 Embedded Resistors
    - Resistance : 208Ω, 255Ω, 293Ω
      - Measurement R = Embedded R + 50Ω (50 Ω Termination)
      - The Larger the Resistance, the Greater the Insertion Loss
    - Capacitive Reactance
      - Ground Plane for Measurement Under the Resistor Pattern



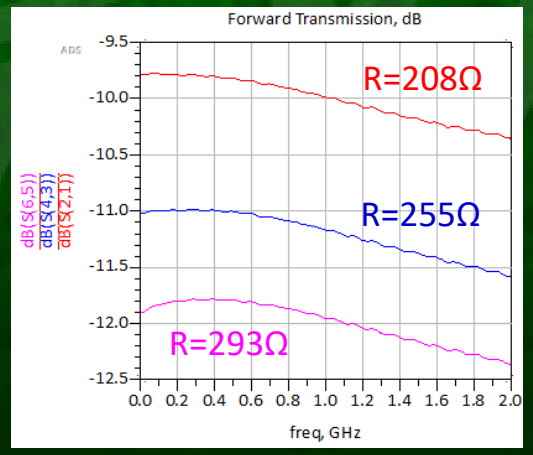


Fig. Result of Resistor Measurement

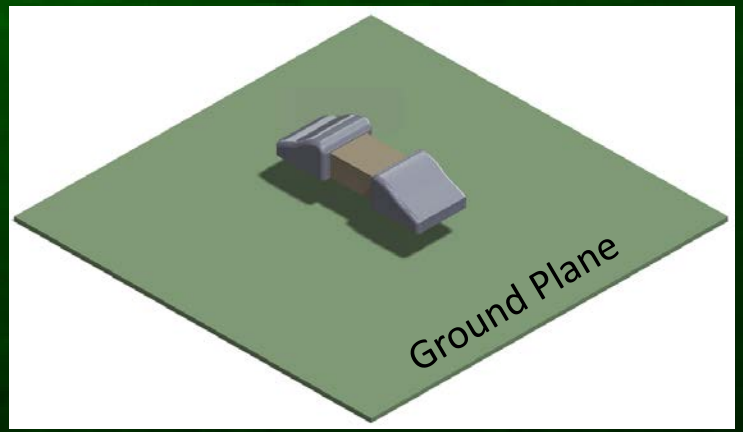


Fig. Embedded Resister Structure

Measurement and Analysis for Protection Resistor

- **X12 Shared Channel Circuit Simulation**
  - Compared with the Lumped Resistor and the Embedded Resistor
  - X12 Circuit Eye Pattern (200Mbps) Simulation
    - Lumped Resistor : Vishay's Resistor S-parameter Database
    - Embedded Resistor : Measured S-parameter Data

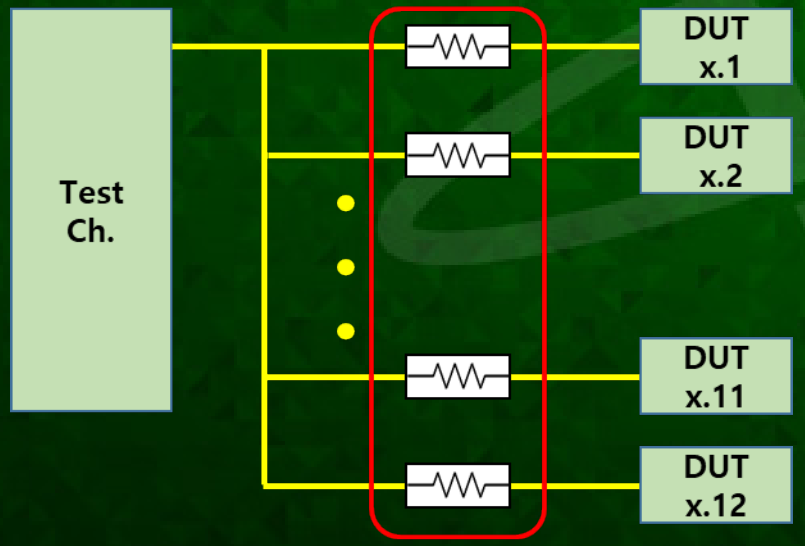
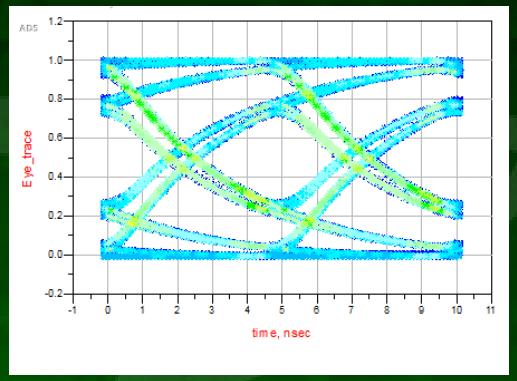
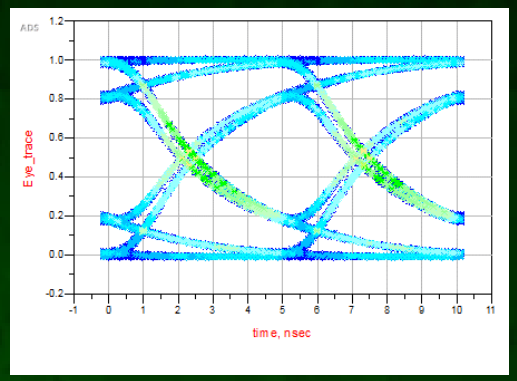


Fig. Block Diagram of x12 Shared Channel



E.R. 208Ω



L.R. 200Ω

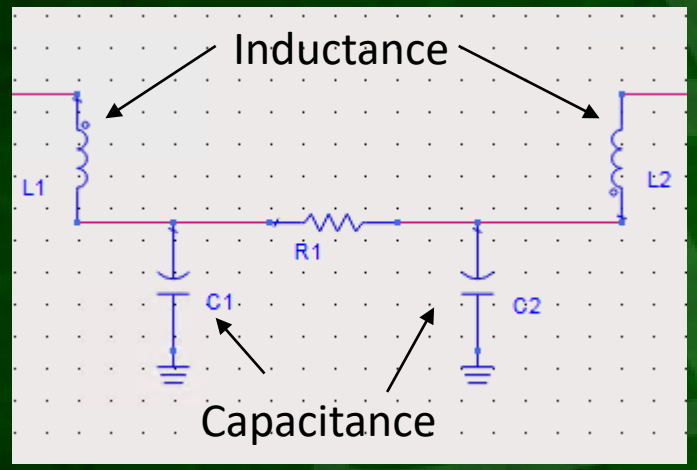
Data rate	2.000E8	2.000E8
Start measurement time	5.507E-8	5.507E-8
Stop measurement time	9.864E-7	9.862E-7
Eye level zero	0.161	0.126
Eye level mean	0.510	0.510
Eye level one	0.860	0.893
Eye amplitude	0.699	0.767
Eye height	0.369	0.484
Eye height (db)	-4.325	-3.155
Eye width	4.079E-9	4.523E-9
Eye opening factor	0.675	0.744
Eye signal to noise	3.081	3.901
Eye duty cycle dist.	4.907E-12	1.410E-10
Eye duty cycle dist. (%)	0.098	2.820
Eye crossing 1 time	2.135E-9	2.313E-9
Eye crossing 1 amplitude	0.500	0.498
Eye crossing 2 time	7.148E-9	7.316E-9
Eye crossing 2 amplitude	0.500	0.498
Average eye rise time	3.118E-9	2.658E-9
Average eye fall time	3.308E-9	2.758E-9
Eye jitter (rms)	3.688E-10	1.984E-10
Eye jitter (pp)	9.570E-10	5.254E-10

➔ **Degradation Eye Diagram Measurement By Capacitive Reactance of Embedded Resistor**

Measurement and Analysis for Protection Resistor

- **Lumped Device Modeling of Embedded Resistor**

(Induced by the Via for Measurement)



(Induced by the Ground Plane)

Fig. Lumped Model of the Embedded Resistor

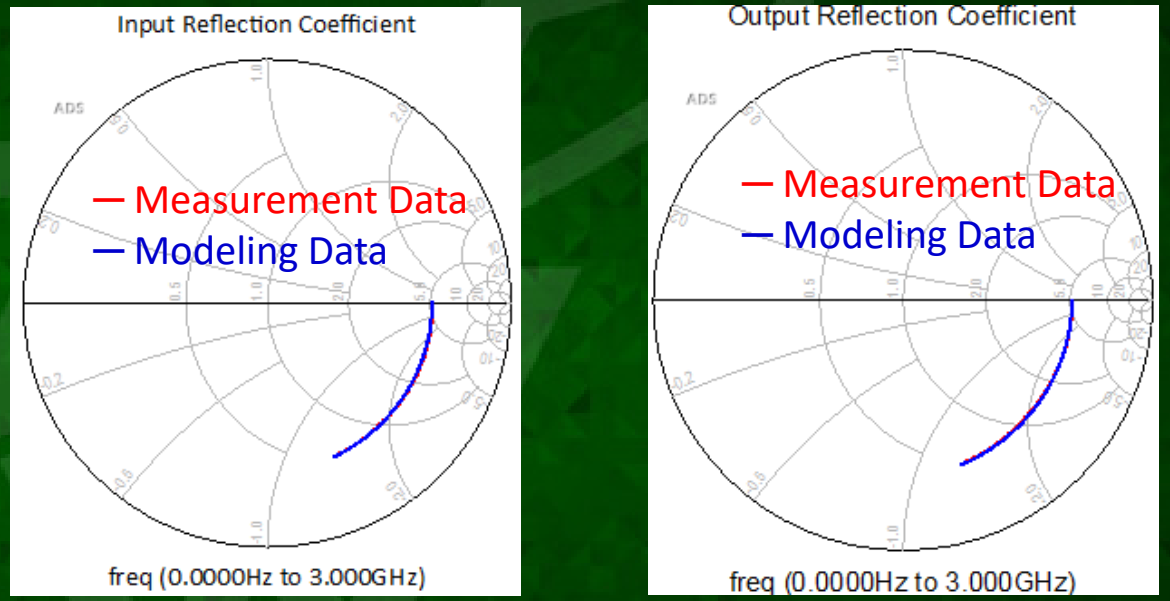


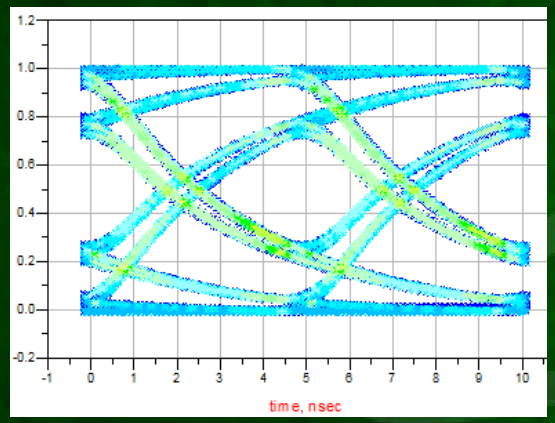
Fig. In/output Reflection Data on the Smith Chart between Measurement and modeling

- Reduction Parasitic Elements
  - Removing the Ground Plane under Embedded Resistor ➔ Decreasing the Capacitance
  - De-embedding the Measurement Data ➔ Removing the Inductance

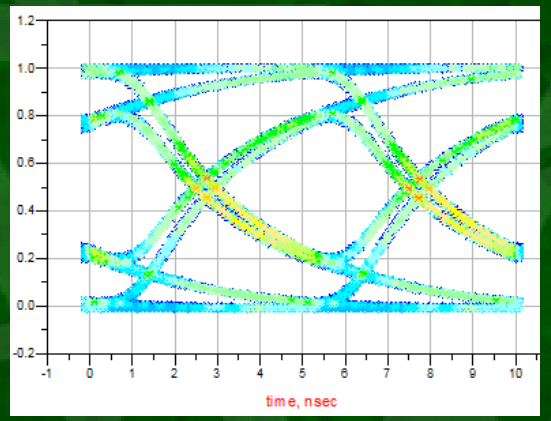
Measurement and Analysis for Protection Resistor

- **Comparative x12 Eye Simulation with Improved Embedded Resistor**
  - Virtual Simulation with Improved E.R. which is reduced Parasitic Reactance to 1/3

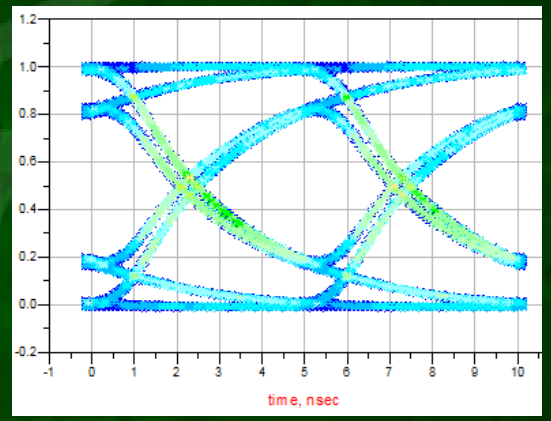
Initial E.R. 208Ω



Improved E.R. 208Ω



Discrete R 200Ω



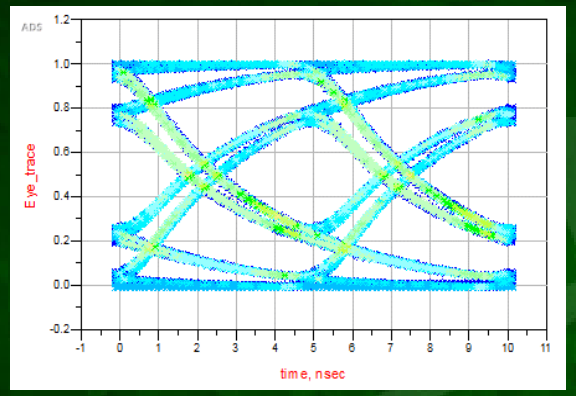
	Eye Level Zero	Eye Level One	Eye Amplitude	Eye Height	Eye Width	Eye Opening Factor	Average Eye Rise Time	Average Eye Fall Time	Eye Jitter (pp)
Initial E.R.	0.161	0.859	0.698	0.369	4.053.E-09	0.674	3.804.E-09	3.306.E-09	1.002.E-09
Improved E.R.	0.137	0.885	0.747	0.458	4.459.E-09	0.728	2.714.E-09	2.832.E-09	5.915.E-10
Discrete R	0.125	0.894	0.770	0.490	4.550.E-09	0.746	2.623.E-09	2.732.E-09	5.259.E-10

➔ Verifying the improvement of Eye Performance close to Discrete R

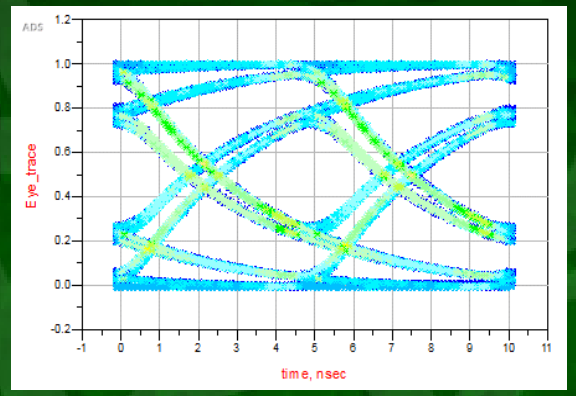
Measurement and Analysis for Protection Resistor

- **Test Simulation about 20% Resistance Tolerance**

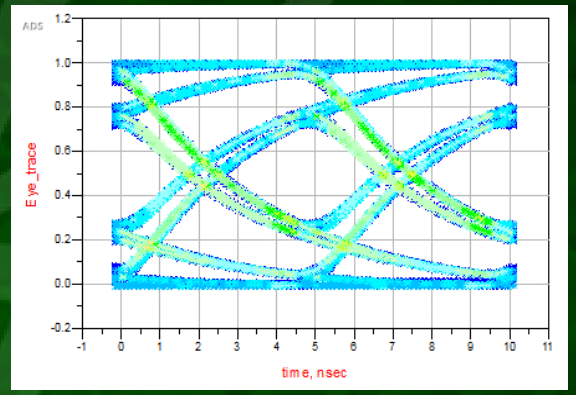
E.R. 208Ω



E.R. 255Ω



E.R. 293Ω



	Eye Level Zero	Eye Level One	Eye Amplitude	Eye Height	Eye Width	Eye Opening Factor	Average Eye Rise Time	Average Eye Fall Time	Eye Jitter (pp)
E.R. 208Ω	0.159	0.862	0.703	0.376	4.099E-09	0.679	3.132E-09	3.274E-09	9.564E-10
E.R. 255Ω	0.161	0.860	0.699	0.369	4.079E-09	0.675	3.118E-09	3.308E-09	9.570E-10
E.R. 293Ω	0.163	0.858	0.695	0.363	4.034E-09	0.673	3.058E-09	3.347E-09	1.003E-09

➔ **No Significant Performance Change even at 20% Resistance Tolerance**

Summary

- **Embedded Protection Resistor**
  - There is a disadvantage that the resistor value can not be tuned when the resistors are embedded in STF
  - Parameter optimization can manage the resistance and tolerance.
  - Protection resistor can be embedded with the target resistance value by adjusting the appropriate width and aspect ratio
- **Probe Card with Embedded Protection Resistor**
  - Signal degradation due to parasitic capacitance from ground structure
  - Available of similar performance like discrete Resistor when improving the embedded resistor structure
  - Even if the protection resistor value of the shared channel in the probe card has tolerance ±20%, it does not affect the transmission performance of the probe card

Future Work

- Simulation Test after Modifying the Resistor Design for Reducing Capacitive Reactance
- Optimization Test of Design Parameter for Stable Resistance
- Additional Resistance Library Setup Experiment
- Applying a Embedded Protection Resistor Test inside 12inch STF
- Increase Yield by Engineering and Manufacturing Valuation Test

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Thanks for Your Attention !