A Technique of Embedding Protection Resistors inside LTCC Substrate using Space TransFormer

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Overview

• Trends of Probe Card
• High Parallelism for Probe Card
• Introduction of Protection Resistor
• Research and Evaluation of Protection Resistor
• Measurement and Analysis for Protection Resistor
• Summary
• Future Works
Trends of Probe Card

- **Global Semiconductor Market**
  - IC market flat in 2015–2016
  - Upturn 24% YoY to 343.2B$ in 2017
    - Economic recovery & expansion in automotive market
  - Weakening growth until 2019

- Memory market Stagnation in 2015-2016
  - Market Changed 61.5% YoY to 124.0B$ in 2017
    - Smartphone, server/data center equipment and SSDs
Trends of Probe Card

- **Global Probe Card Market**

  - **Increased P/card Revenues**
    - In 2017
    - IC & Memory Sales
  - **Steady increase trend of CAGR 5% since 2017**
  - **Need to Check Growth after 2019**

Source: VLSI 2018
Trends of Probe Card

DRAM Die Size & Density Trend

- Fab node ▼
- Memory Density ▲
- Die Size (@ Same Capacity) ▼
- Chip Count per wafer ▲
- Parallelism of P/Card ▲
High Parallelism for Probe Card

• DRAM Probe Card Features

– Over 1,000 DUTs
– Over 100,000 Probes
– Over x10 Shared
– Fine Pitch Pad Probing
  (under 60um)
High Parallelism for Probe Card

• Customer Requirement
  – Electrical Performance
    • Signal Integrity
      – Impedance Control
      – Time of Propagation Delay Matching
      – Differential Pair Trace Matching
      – Multi Shared Channels Routing
    • Power Integrity
      – Low Power Impedance Control
      – DC Trace Resistance
      – Current Carrying Capacity
      – Leakage Current Control
  – Mechanical Performance
    • Probe Contact
      – Force Uniformity
      – Position Accuracy
      – Planarity
      – Scrub Mark in Hot/Cold Temp.
      – Wearing Robustness
      – Depress / Broken
      – Tip Shape Uniformity
    • Stiffener Structure
      – Thermal Deformation
      – Strong Stiffness
High Parallelism for Probe Card

- **Multi Shared Channel Test**
  - Pros and Cons

- **Productivity Increase**
  - Expansion Limited ATE Resource
  - Short Test Time

- **Yield Decrease**
  - Reduction Test Cost
  - Impedance Mismatching
  - Simultaneous Fail by Short Defect

- **Test Time Reduction**
- **Test Cost Reduction**
- **Yield Decrease**
- **Impedance Mismatching**
- **Crosstalk Increasing**
- **Short Defect**
Introduction of Protection Resistor

• **Role of Protection Resistor**
  
  – Short Defect Isolation by Protection Resistors at shared Channel

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**Source:** G. Kim and W. Nah, “NAC Measurement Technique on High Parallelism Probe Card with Protection Resistors”, Journal of Semiconductor Technology and Science, VOL.16, NO.5,
Introduction of Protection Resistor

- **Recommended Channel to Use Protection Resistor**
  - **Recommended Channel**
    - Only Input Shared Channel
  - **Restriction Channel**
    - Output Channel include I/O

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**x12 Shared Channel with Protection Resistors**

<table>
<thead>
<tr>
<th>ATE</th>
<th>Probe Card</th>
<th>Wafer</th>
</tr>
</thead>
<tbody>
<tr>
<td></td>
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<table>
<thead>
<tr>
<th>Test Ch.</th>
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**Shared Output Channel**

<table>
<thead>
<tr>
<th>Wafer</th>
<th>Probe Card</th>
<th>ATE</th>
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</thead>
<tbody>
<tr>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Protection Resistor**

- $V_{ON}$
- $V_{PR}$
- $R_{ON}$
- $R_{PR}$

**ATE Test Ch.**

**V_{ATE}**

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Research and Evaluation of Protection Resistor

- **Types of Appropriate Protection Resistor**
  - Surface Mount Resistor on Substrate
    - Need to Packaging Area, Time and Cost
    - Highly Resistance Accuracy and Various Value
  - Embedded Resistor in Substrate
    - No Packaging Area on the Substrate with over 100K pins
    - Inaccurate Resistance and Low Resistance
  - Types
    - Lumped Resistor
    - Thin Film Array Resistor Module
      - Thick Film Resistor on Inner Ceramic
Embedded Thick Film Resistor

**Feature**
- Similar Processing like a Lumped Resistor
- Using LTCC (Low Temperature Co-fired Ceramic) Process for Making Embedded Resistor

**Advantage**
- Free Space on the Substrate Surface
- No Degradation during Post-Processing
  - Machining, Thin Film Process, MEMS, etc.
- Reduce Cost
  - Post-Processing Fail Cost, Soldering, etc.

**Disadvantage**
- Rough Resistance Tolerance between Resistors
- Un-tunable Resistance
Research and Evaluation of Protection Resistor

- **LTCC Introduction**
  - Low Temperature Co-fired Ceramic
    - Material: Alumina + Glass
    - Firing Temperature: 850 °C
    - Conductor Metal: Ag, Au, Cu
  - Feature
    - High Conductivity Metal Electrode
    - Low Dielectric Loss
    - Embedded Passive Devices

- **LTCC Application**
  - RF
  - Automotive
  - Semiconductor
  - Military
  - FEM
  - DMB-M
  - WLAN
  - 60GHz WPAN
  - Radar
  - EPS
  - MAP Sensor
  - Probe Card
  - ESC
  - Heater
  - Transceiver
  - Radar TRM

*Fig. Space Transformer for Probe Card*

Source: SEMCNS
Research and Evaluation of Protection Resistor

Variable Experiment to Overcome Resistance Tolerance

- **Design Parameter**
  ① Width & Length
  ② Width & Length Aspect Ratio
  ③ Termination Pad Size

- **Process Parameter**
  ① Paste Printing Thickness
  ② Printing Direction
  ③ Lamination Structure
Research and Evaluation of Protection Resistor

Prototype Test Experiment

• Test Vehicle for Fixing the Parameter and Setup the Library

Green Sheet base on LTCC

Resistor Paste
Termination Pad
Ground Pad

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Measurement and Analysis for Protection Resistor

- **Dimension Gap Compared to Design after Printing Process**
  - Process Gap is Similar from above Small Size

![Graph showing dimension gap comparison](image)

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Measurement and Analysis for Protection Resistor

• **Thickness Profile Measurement**
  – Overall Thickness: Constant
  – Side Slope: Depends on Paste Length
    • Vertical Direction
      ➔ Need to Process Control
    • Horizontal Direction
      ➔ Overlap Control of Termination Pad and Resistor Pattern

• **Process Variable Optimization**
  – Control factor
    • Thickness + Flatness
    • Side Slope
Measurement and Analysis for Protection Resistor

• **Result of Resistance Measurement**
  
  – Predictable Resistor Value by Aspect Ratio
  
  – Under ± 20% Resistance tolerance
    
    • Under ± 15% on Low Aspect Ratio
  
  – Low Tolerance Level between Lots on Low Aspect Ratio
Measurement and Analysis for Protection Resistor

- **Measurement Setup of Resistor**
  - Network Analyzer: Agilent E5071C
  - Probe Station: DSF System BTE300
  - Probe Tip: Picoprobe ECP18-SG-600
  - Test Sample: 8 Inch LTCC Test Substrate
Measurement and Analysis for Protection Resistor

• Result of S-parameter Measurement
  – Result of 3 Embedded Resistors
    • Resistance: 208Ω, 255Ω, 293Ω
      – Measurement $R = $ Embedded $R + 50Ω$ (50 Ω Termination)
      – The Larger the Resistance, the Greater the Insertion Loss
    • Capacitive Reactance
      – Ground Plane for Measurement Under the Resistor Pattern

Fig. Result of Resistor Measurement

Fig. Embedded Resistor Structure
Measurement and Analysis for Protection Resistor

- **X12 Shared Channel Circuit Simulation**
  - Compared with the Lumped Resistor and the Embedded Resistor
  - X12 Circuit Eye Pattern (200Mbps) Simulation
    - Lumped Resistor: Vishay’s Resistor S-parameter Database
    - Embedded Resistor: Measured S-parameter Data

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**Fig. Block Diagram of x12 Shared Channel**

- Degradation Eye Diagram Measurement By Capacitive Reactance of Embedded Resistor
Measurement and Analysis for Protection Resistor

• Lumped Device Modeling of Embedded Resistor

(Induced by the Via for Measurement)

Inductance

Capacitance

(Induced by the Ground Plane)

Fig. Lumped Model of the Embedded Resistor

Fig. In/output Reflection Data on the Smith Chart between Measurement and modeling

– Reduction Parasitic Elements
  • Removing the Ground Plane under Embedded Resistor ➞ Decreasing the Capacitance
  • De-embedding the Measurement Data ➞ Removing the Inductance
Comparative x12 Eye Simulation with Improved Embedded Resistor

- Virtual Simulation with Improved E.R. which is reduced Parasitic Reactance to 1/3

<table>
<thead>
<tr>
<th></th>
<th>Eye Level Zero</th>
<th>Eye Level One</th>
<th>Eye Amplitude</th>
<th>Eye Height</th>
<th>Eye Width</th>
<th>Eye Opening Factor</th>
<th>Average Eye Rise Time</th>
<th>Average Eye Fall Time</th>
<th>Eye Jitter (pp)</th>
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</thead>
<tbody>
<tr>
<td>Initial E.R.</td>
<td>0.161</td>
<td>0.859</td>
<td>0.698</td>
<td>0.369</td>
<td>4.053.E-09</td>
<td>0.674</td>
<td>3.804.E-09</td>
<td>3.306.E-09</td>
<td>1.002.E-09</td>
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<td>Improved E.R.</td>
<td>0.137</td>
<td>0.885</td>
<td>0.747</td>
<td>0.458</td>
<td>4.459.E-09</td>
<td>0.728</td>
<td>2.714.E-09</td>
<td>2.832.E-09</td>
<td>5.915.E-10</td>
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<tr>
<td>Discrete R</td>
<td>0.125</td>
<td>0.894</td>
<td>0.770</td>
<td>0.490</td>
<td>4.550.E-09</td>
<td>0.746</td>
<td>2.623.E-09</td>
<td>2.732.E-09</td>
<td>5.259.E-10</td>
</tr>
</tbody>
</table>

Verifying the improvement of Eye Performance close to Discrete R
Measurement and Analysis for Protection Resistor

- Test Simulation about 20% Resistance Tolerance

- No Significant Performance Change even at 20% Resistance Tolerance
Summary

• **Embedded Protection Resistor**
  – There is a disadvantage that the resistor value can not be tuned when the resistors are embedded in STF
  – Parameter optimization can manage the resistance and tolerance.
  – Protection resistor can be embedded with the target resistance value by adjusting the appropriate width and aspect ratio

• **Probe Card with Embedded Protection Resistor**
  – Signal degradation due to parasitic capacitance from ground structure
  – Available of similar performance like discrete Resistor when improving the embedded resistor structure
  – Even if the protection resistor value of the shared channel in the probe card has tolerance ±20%, it does not affect the transmission performance of the probe card
Future Work

• Simulation Test after Modifying the Resistor Design for Reducing Capacitive Reactance
• Optimization Test of Design Parameter for Stable Resistance
• Additional Resistance Library Setup Experiment
• Applying a Embedded Protection Resistor Test inside 12inch STF
• Increase Yield by Engineering and Manufacturing Valuation Test
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