



**SWTEST**

PROBE TODAY, FOR TOMORROW

# Stretching the Performance Envelope of ATE PCBs



**Tom Bleakley**  
Harbor Electronics

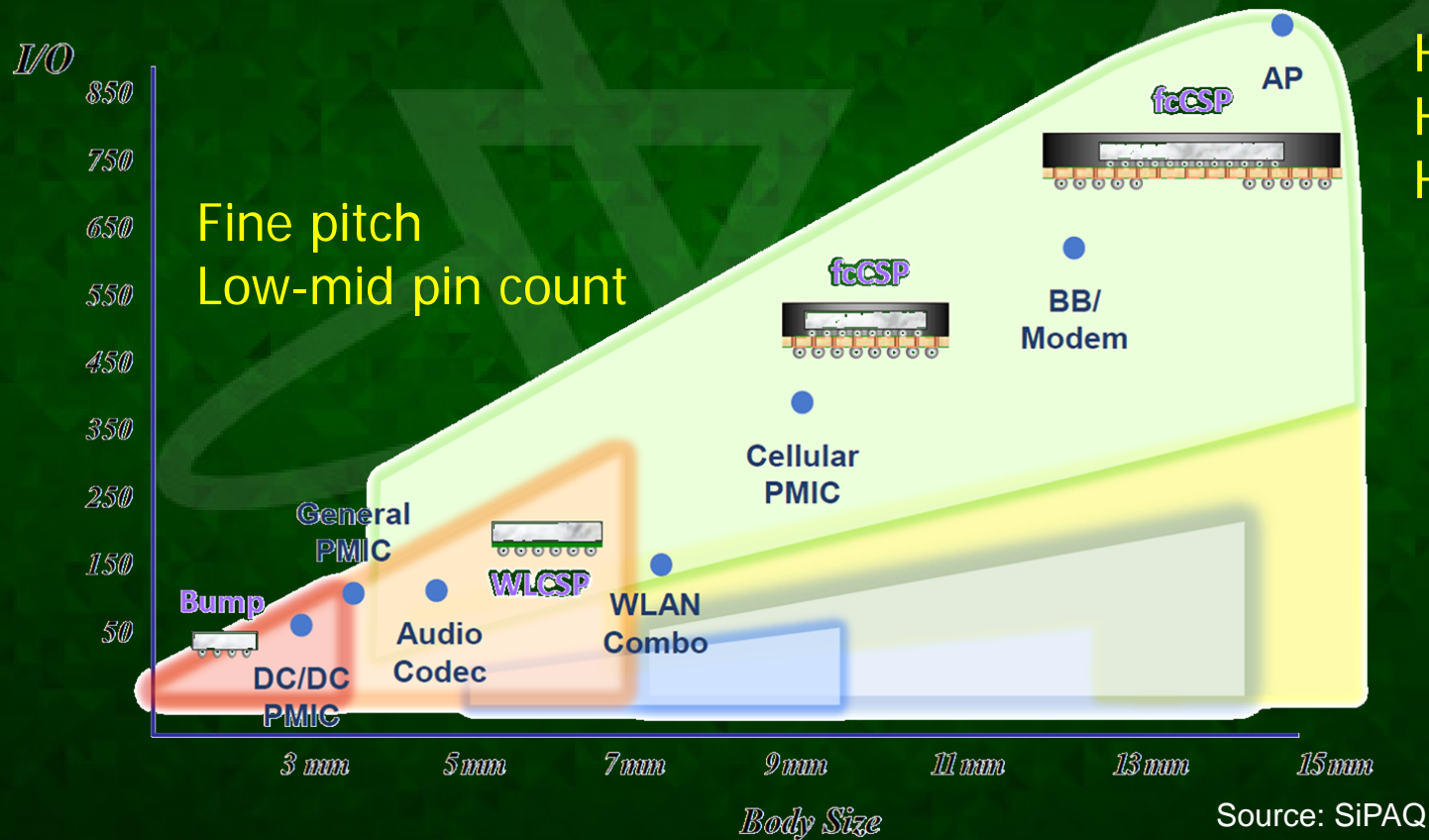
June 2-5, 2019

# Overview

- Market Forces / Industry Trends
- PCB Fabrication: basics and technology extenders
- ViaBond as the latest Technology extender
- ViaBond Applications
- ViaBond Next Steps
- Summary

# Industry Trends

- IC package size, pitch, IO count & parallelism drive complexity into the ATE interface



# Impact on Production Test ATE Interface

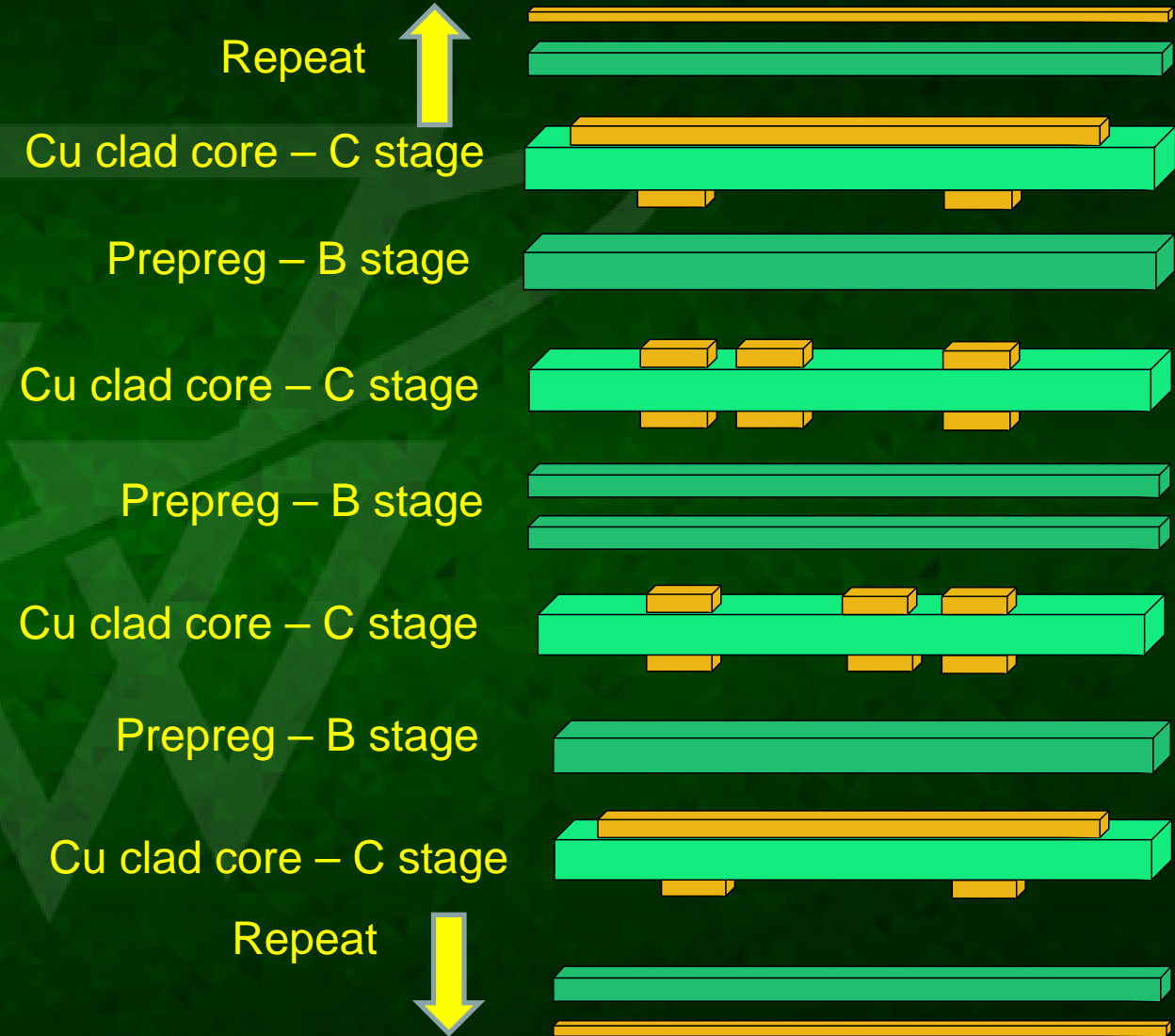
- PCB manufacturing techniques need augmenting just to keep up
- Harbor emphasizes extending mechanical drilling as far as it can go

| Complexity | Device Pitch               | Device Ball Count | Parallel Test | Power (Current) | Speed                      | Test Cell Configuration                                    |
|------------|----------------------------|-------------------|---------------|-----------------|----------------------------|--|
| Low        | 0.5mm - 1mm                | 100               | 1up – 4up     | < 1A            | <1GBS                      | Singulated package test<br>Staggered die                   |
| Med        | 0.40mm<br>0.35mm<br>0.30mm | 200+              | 4up – 16up    | 100A / DV 50mv  | 10GBS                      | WLSCP<br>Extended temp range<br>(Automotive)               |
| High       | < 0.30mm                   | 6000              | 16up - 128x   | 400A / DV <25mV | 28GBS NRZ /<br>112GBS PAM4 | Direct Attach<br>1 mil Flatness<br>pad condition<br>OTA 5G |



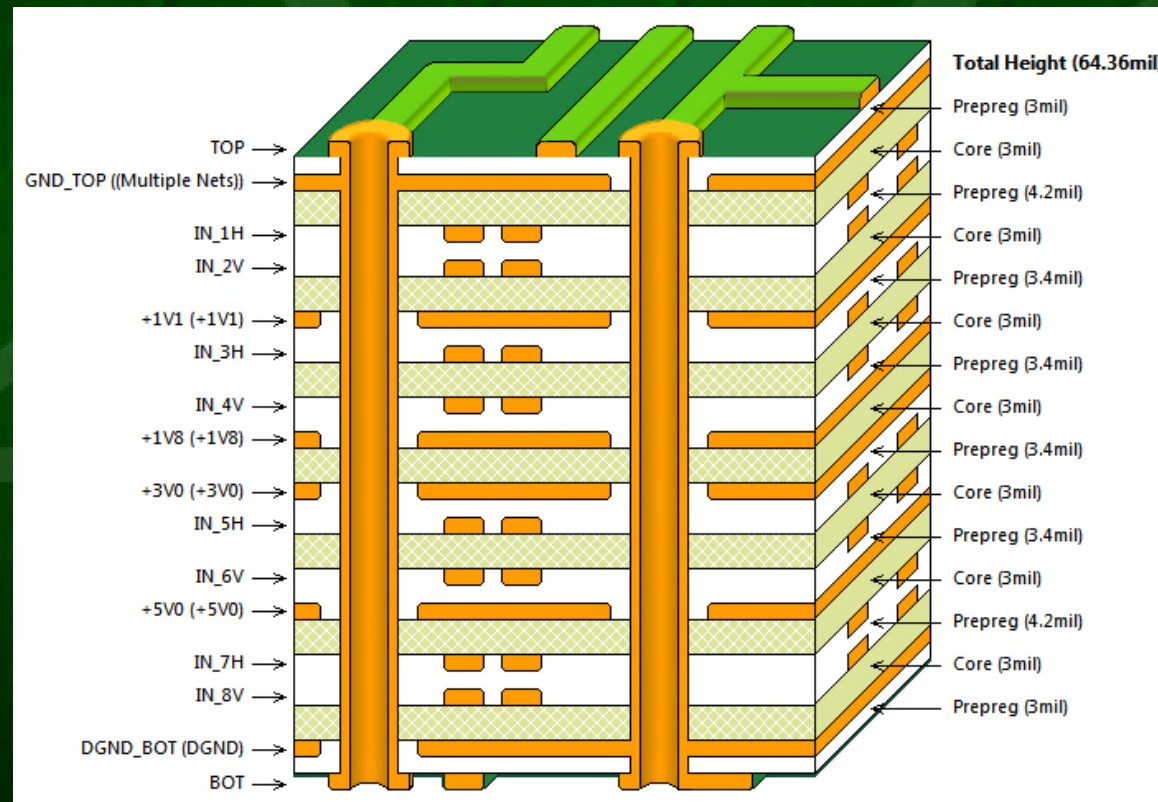
# PCB Fabrication Basics

- The basic building blocks of the PCB are the same as they have been for years
- Double sided C-stage Cu clad cores and B-stage prepreg to bond the cores together
- Repeat this basic structure over and over as necessary to complete the multi-layer PCB



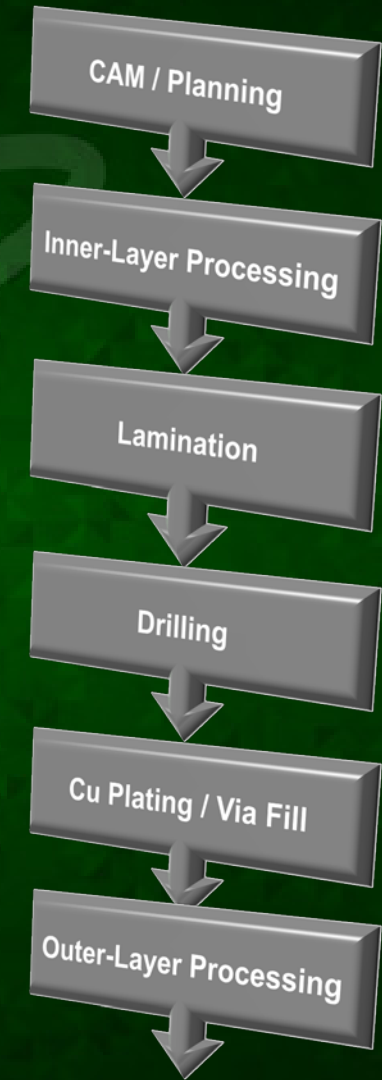
# PCB Fabrication Basics

- Controlled impedance layers; add some power planes
- Balanced stack-up to minimize warpage



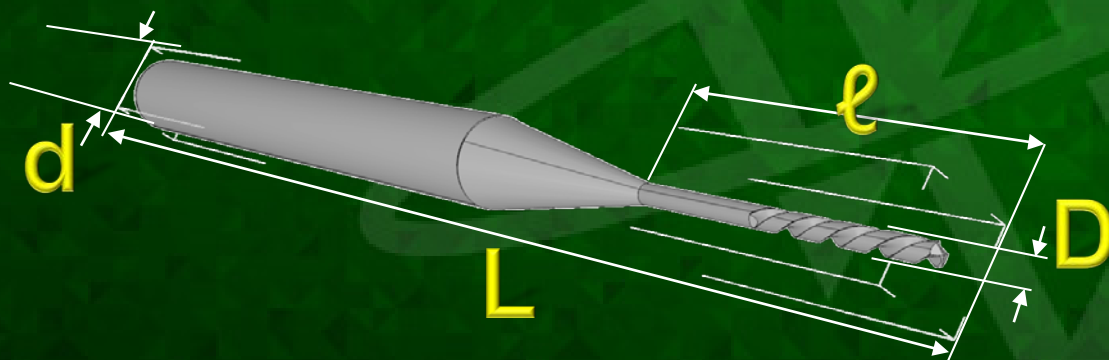
# PCB Fabrication Basics

- So far, so good, ~5 day turn



# PCB Thickness vs Drill Flute Length

- Now ramp up the complexity factors
- DUT pin count / parallelism drives up layer count
- Layer count drives overall PCB thickness
- Encounter limitations of PCB drill dimensions, specifically Flute Length
- Flute Length limits PCB Thickness



- Note that Flute Length varies with drill diameter  
Smaller the drill diameter, shorter the flute length
  - 10 mil drill, flute length = 0.220"
  - 6 mil drill, flute length = 0.120"

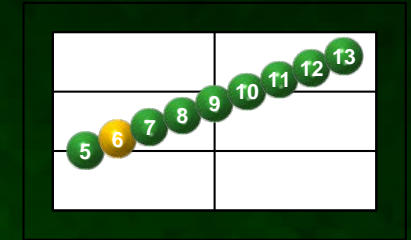
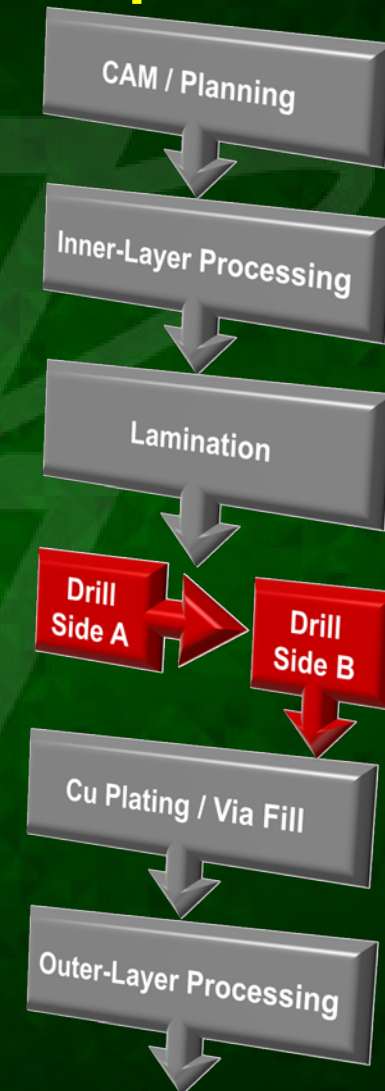
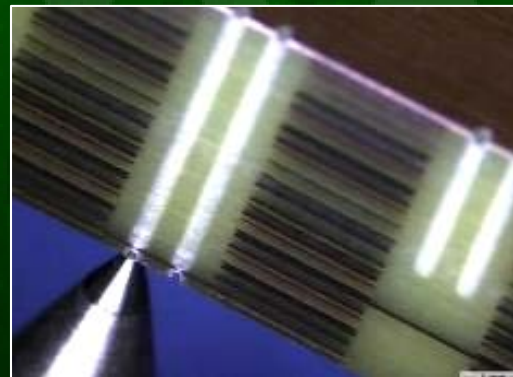
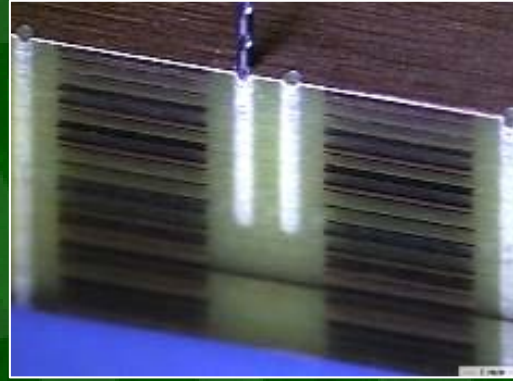
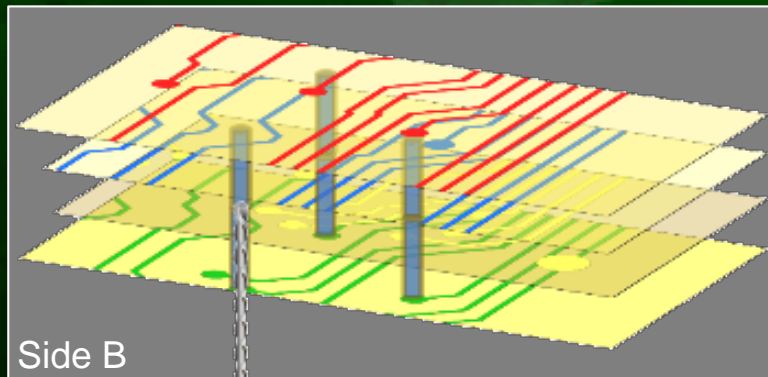
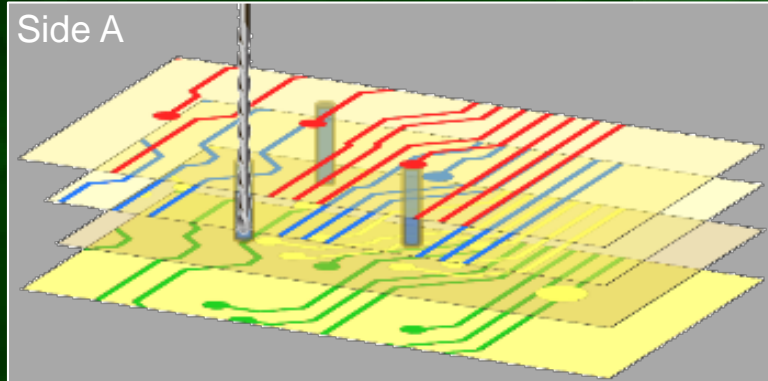
| Drill Size | Dimensions (in) |     |        |       | Point Angle |
|------------|-----------------|-----|--------|-------|-------------|
|            | D               | d   | ℓ      | L     |             |
| .10mm      | 0.0040          | 1/8 | 0.0700 | 1 1/2 | 118°        |
| .13mm      | 0.0050          | 1/8 | 0.0700 | 1 1/2 | 118°        |
| #97        | 0.0059          | 1/8 | 0.1200 | 1 1/2 | 118°        |
| #96        | 0.0063          | 1/8 | 0.1200 | 1 1/2 | 118°        |
| #95        | 0.0067          | 1/8 | 0.1200 | 1 1/2 | 118°        |
| #94        | 0.0071          | 1/8 | 0.1500 | 1 1/2 | 118°        |
| #93        | 0.0075          | 1/8 | 0.1500 | 1 1/2 | 118°        |
| #92        | 0.0079          | 1/8 | 0.1500 | 1 1/2 | 118°        |
| #91        | 0.0083          | 1/8 | 0.1500 | 1 1/2 | 118°        |
| #90        | 0.0087          | 1/8 | 0.1500 | 1 1/2 | 118°        |
| #89        | 0.0091          | 1/8 | 0.2200 | 1 1/2 | 118°        |
| #88        | 0.0095          | 1/8 | 0.2200 | 1 1/2 | 118°        |
| .25mm      | 0.0098          | 1/8 | 0.2200 | 1 1/2 | 118°        |
| #87        | 0.0100          | 1/8 | 0.2200 | 1 1/2 | 118°        |

<http://www.kyoceramicrotools.com/micro/drilling/Series-105-6>



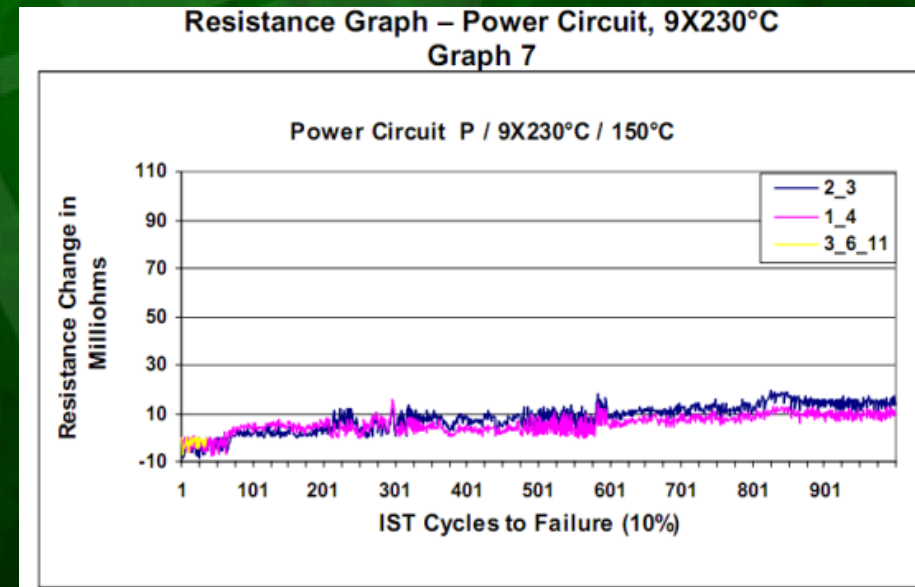
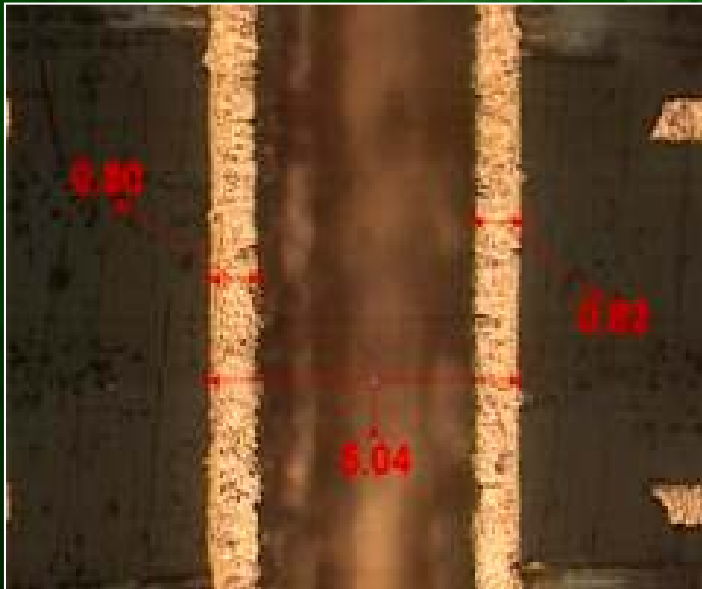
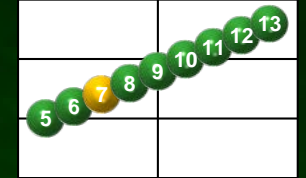
# Technology Extender: Flip Drill

- Drill side A, flip PCB, drill from side B
- Doubles the PCB thickness which can be drilled
- Also doubles the number of holes to drill



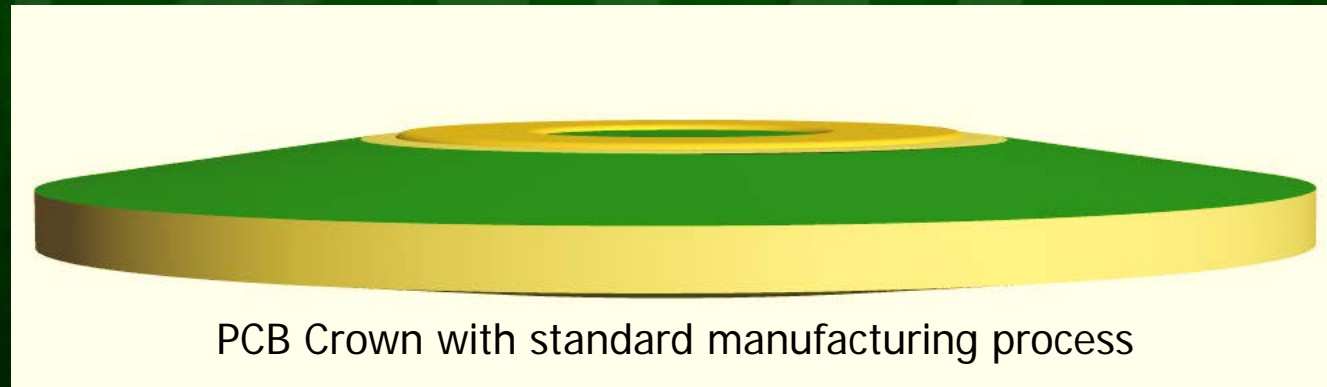
# Plating High Aspect Ratio Vias

- Small diameter holes through thick PCBs make for aspect ratios in excess of 30:1
- Technology extender: pulse plating
- Plating the holes adequately is non-trivial, but well understood
- However, pulse plating techniques add to processing time



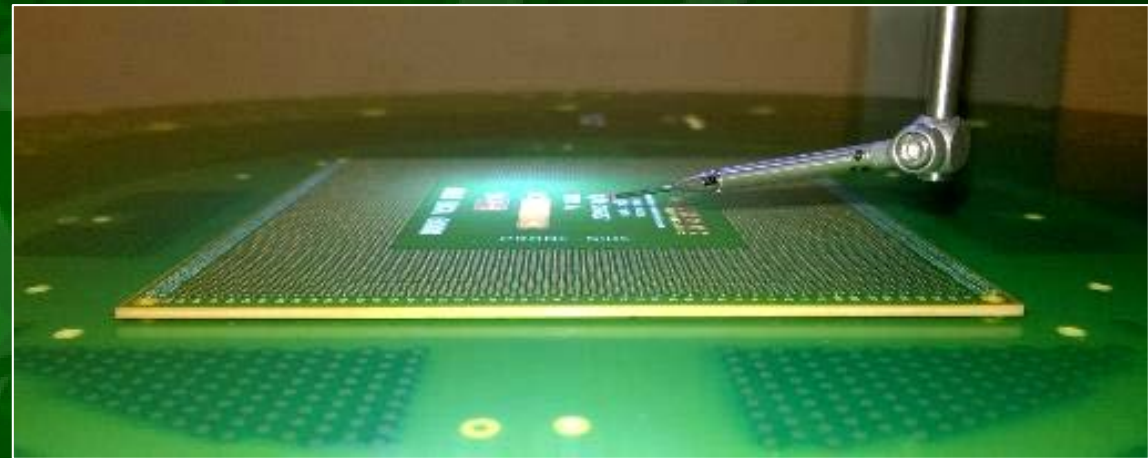
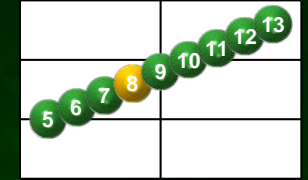
# WLCSP Planarity Requirements

- Multi-site testing effectively increases area of DUT site
- So-called 'Direct Attach' applications which require excellent planarity ( 1 mil across entire DUT area )
- In the PCB, Cu density is usually greatest at center / DUT sites
- Prepreg squeezes out the edge of the panel during lamination
- Rate varies with Cu density
- Creates a board with 'crown' at / near center of PCB



# Technology Extender: UltraFlat™

- Improves flatness / warpage across the DUT area and across the entire board
  - 0.1%-0.15% (0.001"-0.0015" per inch) on most applications
  - 0.2% on dual lamination
- Adds processing time



Harbor UltraFlat™ Technology



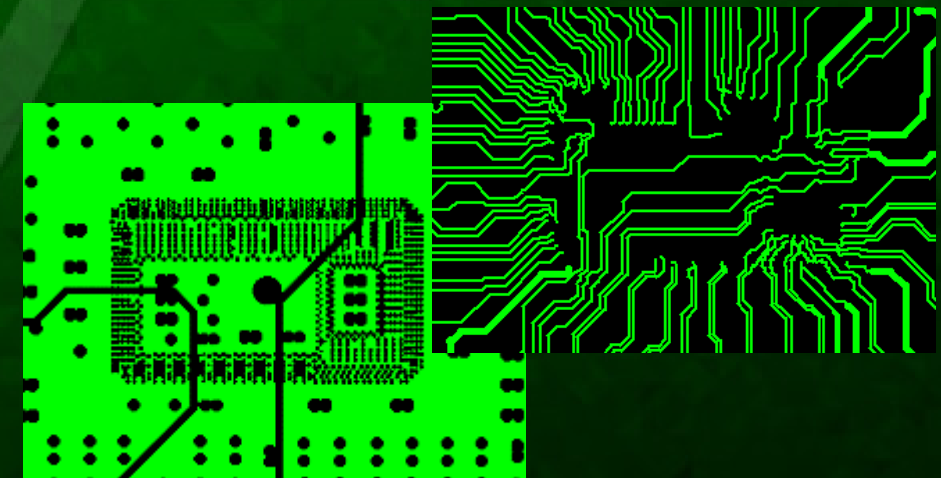
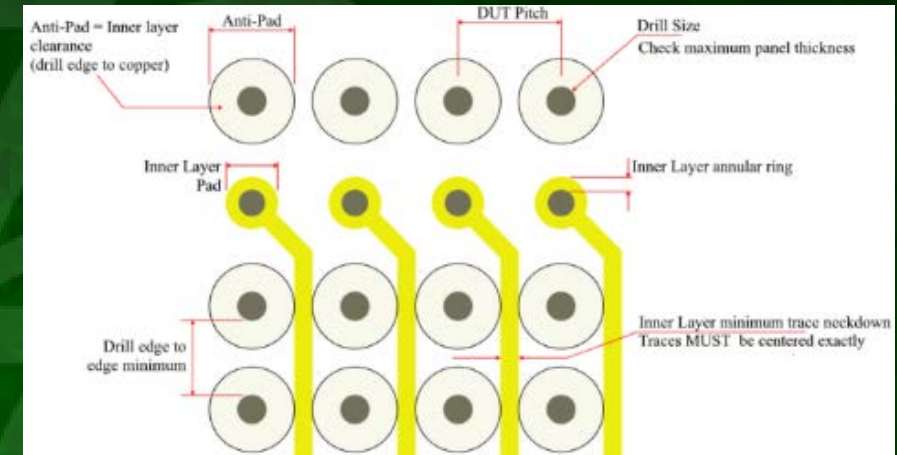
PCB Crown with standard Mfg. Process



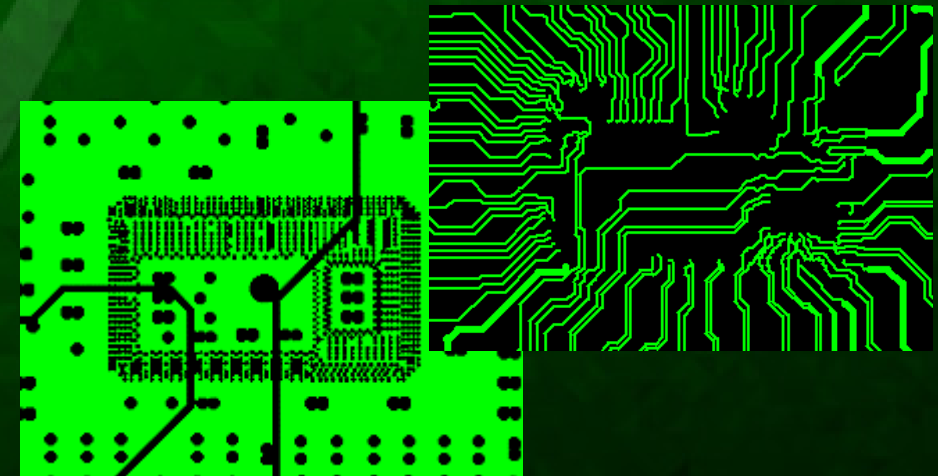
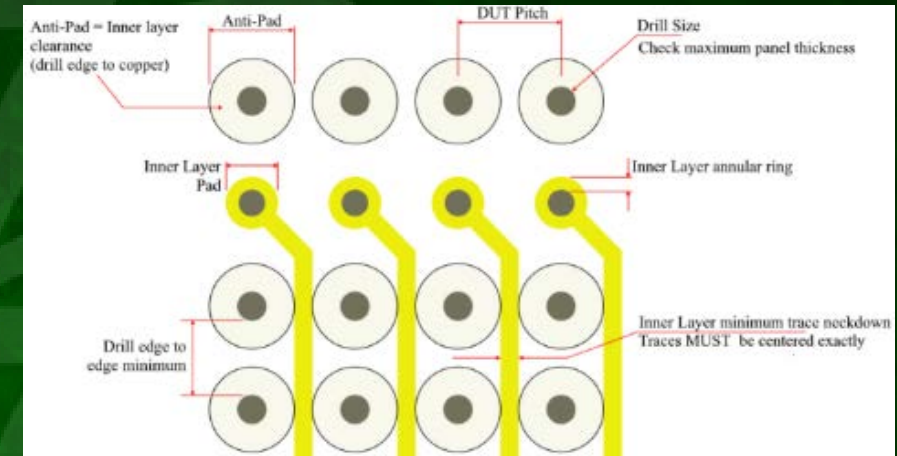
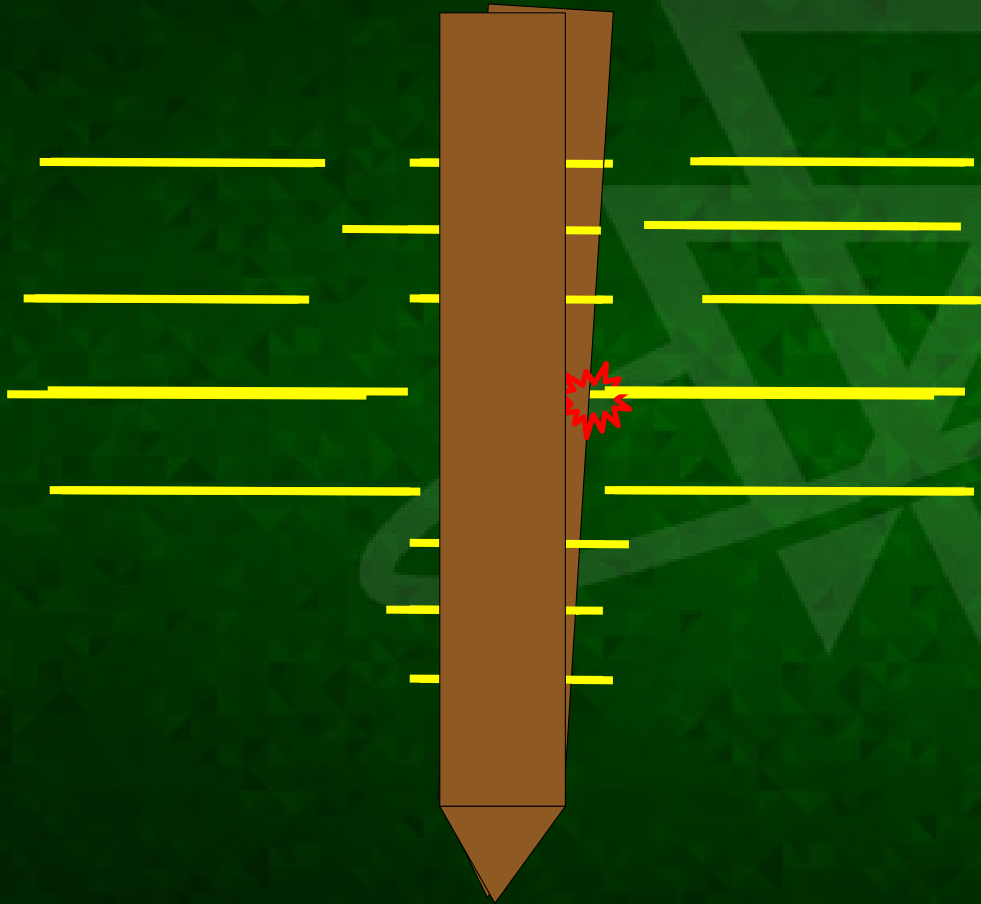


# Fine Pitch Devices

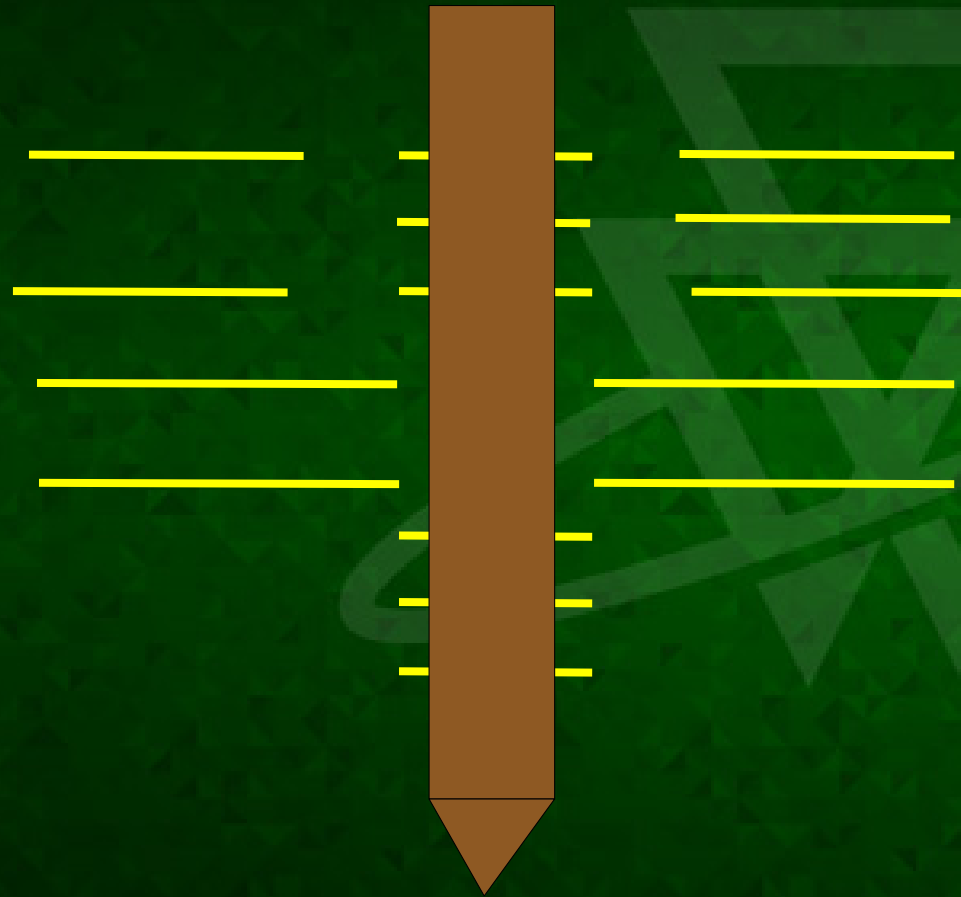
| Fine Pitch DFM          |   |  |   |
|-------------------------|---|--|---|
| Registration Geometries | 0.4mm pitch                               | 0.35mm pitch   | 0.30mm pitch  |
| Drill Diameter          | 0.13mm (0.0051")                          | 0.13mm (0.0051")   | 0.10mm (0.0041")  |
| Anti-pad                | 0.322mm (0.0127")                         | 0.0307mm (0.0121")   | 0.236mm (0.0093")   |
| Trace/Web               | 0.0762mm (0.003")                         | Trace: 0.0635mm (0.0025")<br>Web: 0.0445mm (0.00175")                  | 0.0635mm (0.0025")  |
| Thickness               | 5.08mm (0.200")                           | 5.08mm (0.200")  | 2.286mm (0.090")  |
| Layer Count             | ≤ 50                                      | ≤ 50   | ≤ 22  |
| Registration Challenges | - Lay-up precision<br>- Material movement | - Same drill size as 0.4mm<br>- Narrower trace width<br>- Narrower web | - Smaller drill diameter allows relief to trace width and web |



# Layer to Layer Registration is Key



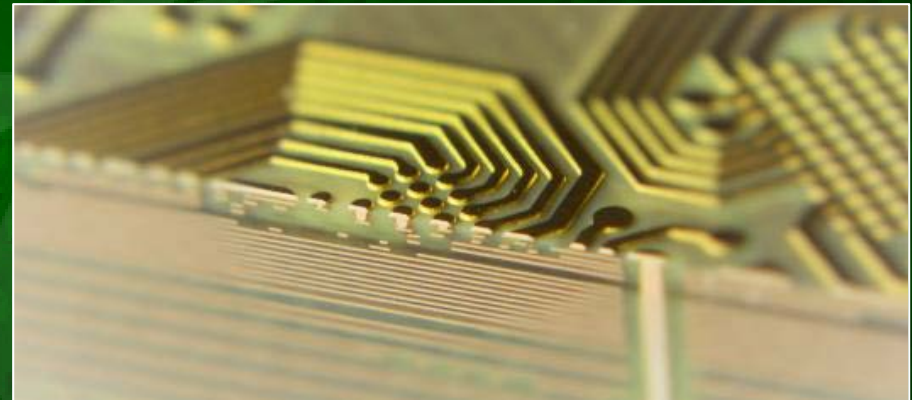
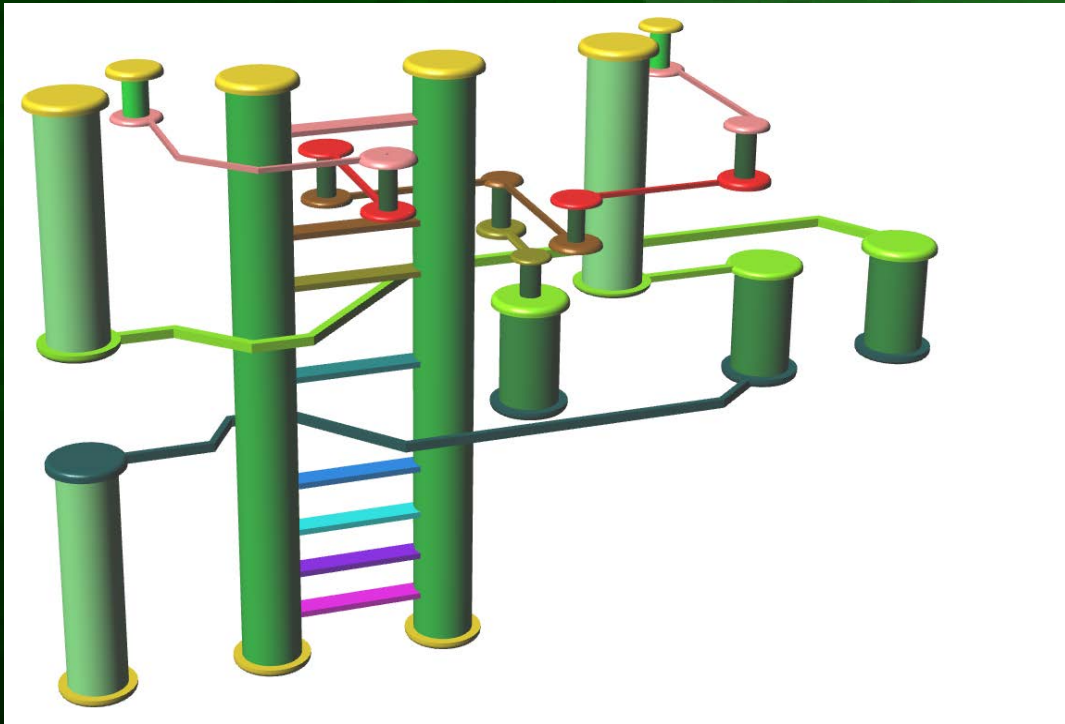
# Technology Extender: Superior Registration



- Shrinkage compensation / Scaling
- Pluritec – Xray + Xact DB
- Optimized Laser Direct Imaging (LDI) for superior Front to back registration
- Precision Post Etch Punch & Pin lamination
- Pilot lots when necessary

# Need to Conserve Routing Area

- Available routing lanes increases when vias do not go all the way through the PCB.
- Blind and buried vias are employed to accomplish that.
- Laser drilled micro vias for HDI implementations

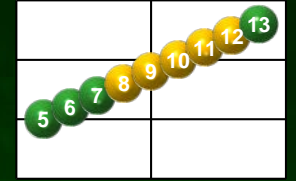


- Blind Vias
- Micro-Vias (Laser Drilled)
- Plated Thru Holes
- Buried Vias
- Buried Micro-Vias



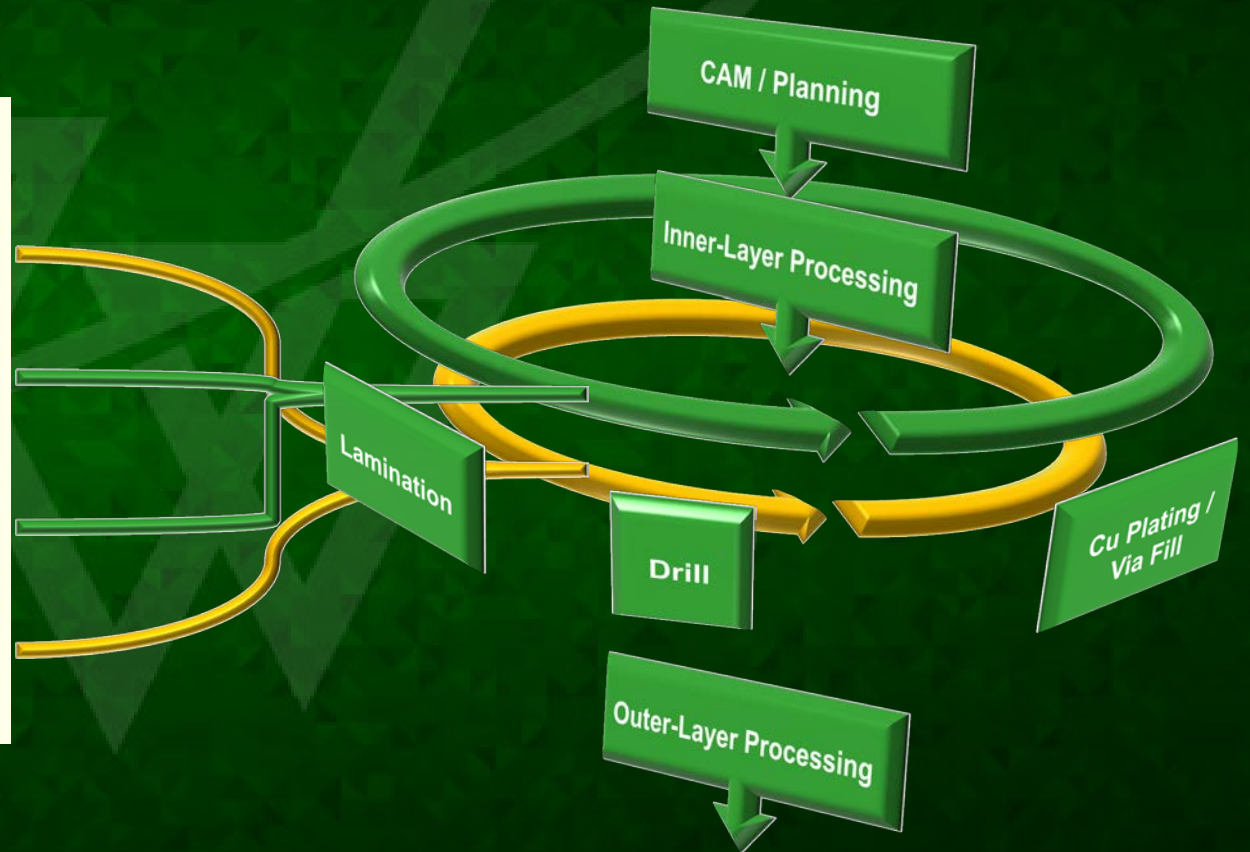
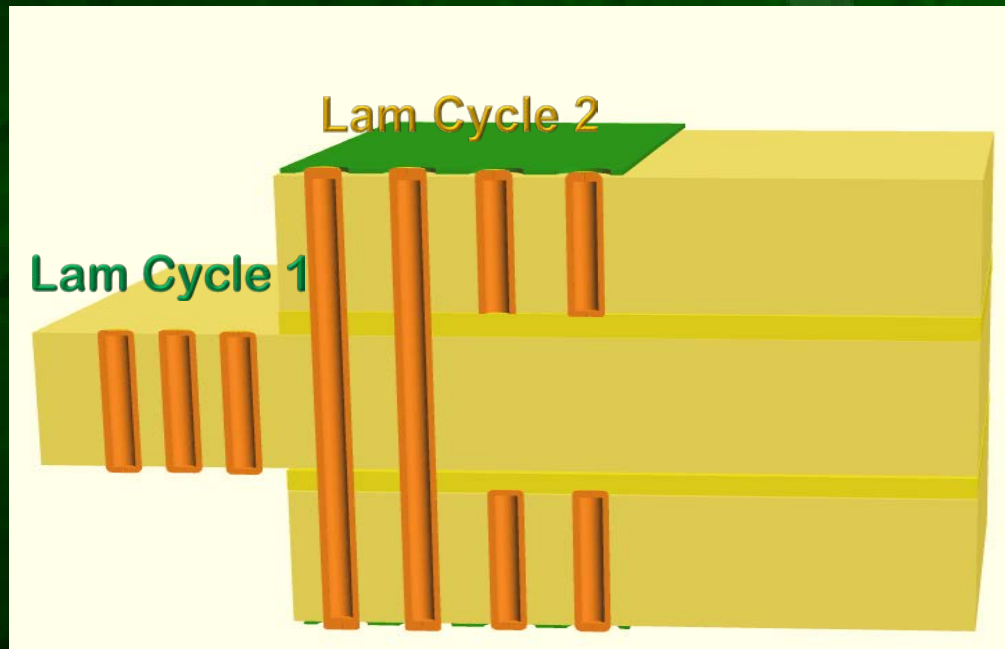
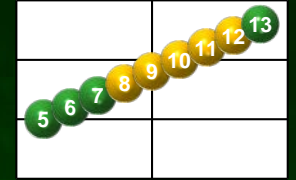
# Technology Extender: Multiple Lamination Cycles

- Overall thickness may still be an issue for the through-vias



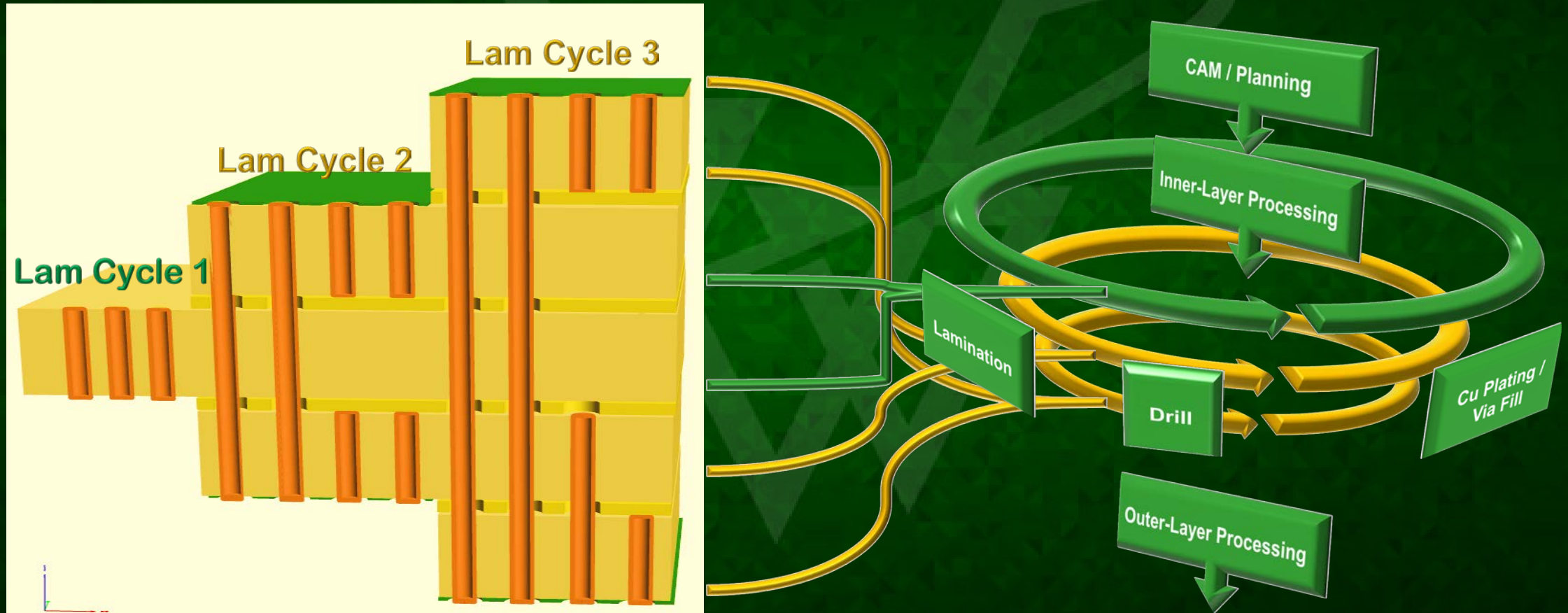
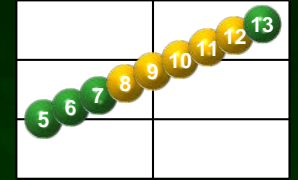
# Technology Extender: Multiple Lamination Cycles

- Overall thickness may still be an issue for the through-vias



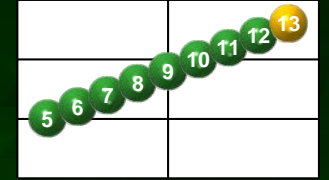
# Technology Extender: Multiple Lamination Cycles

- Overall thickness may still be an issue for the through-vias

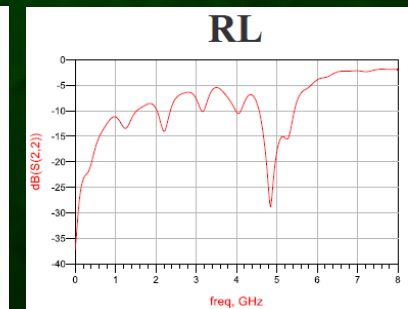
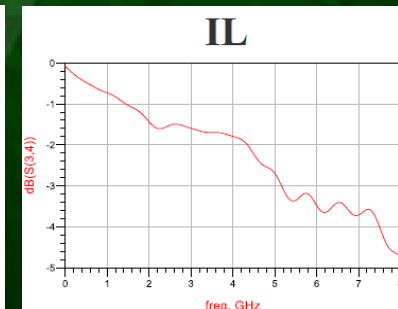
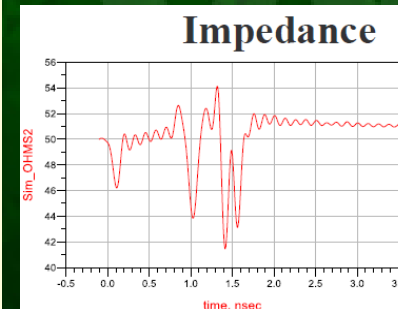
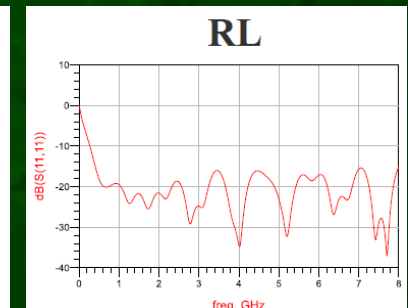
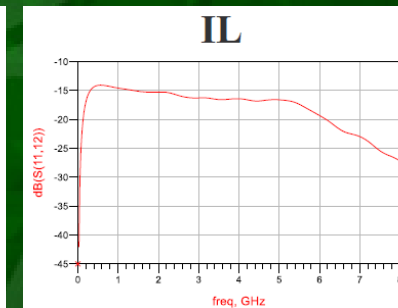
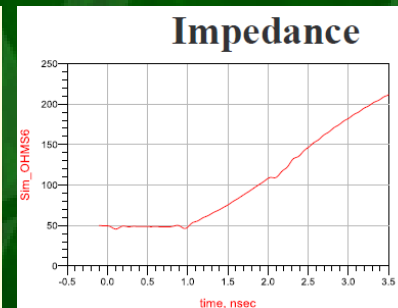
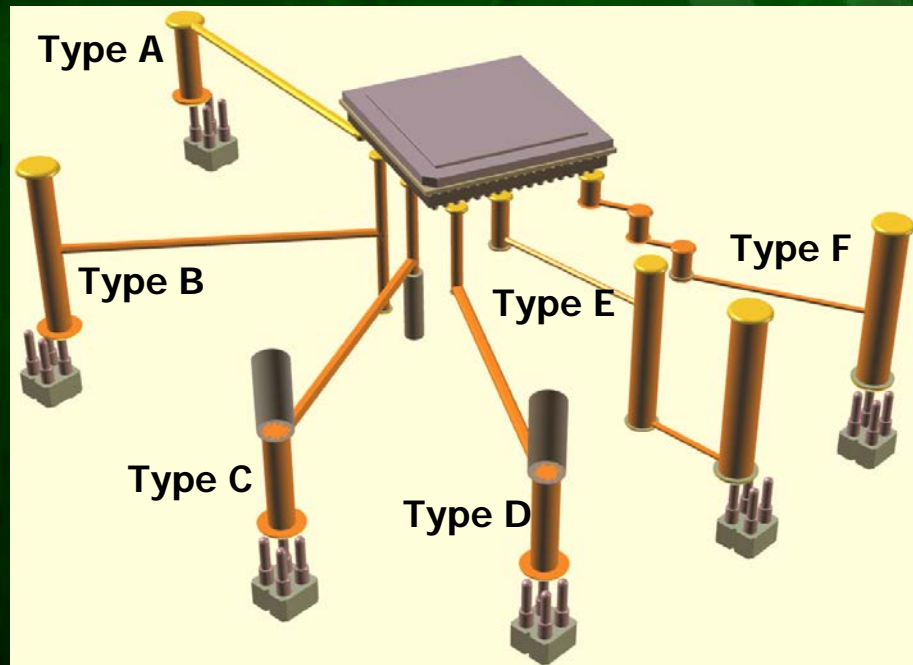


# Signal Integrity

- Signal Integrity Requirements are always in play
  - Single lam, with backdrill, dual-lam, with backdrill, multi-lam
  - In all cases, the thickness of the PCB or “book” is limited to some degree by drill flute length



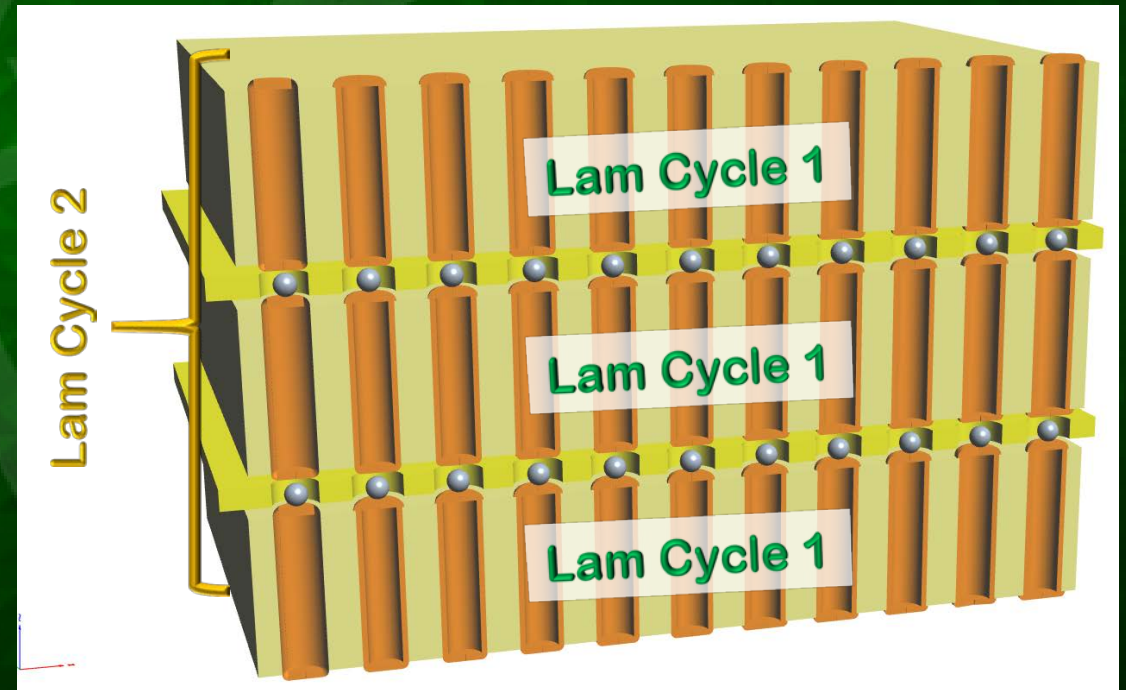
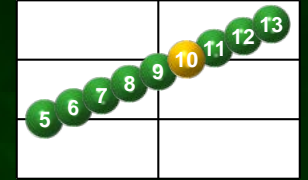
## Signal Integrity DUT to Tester





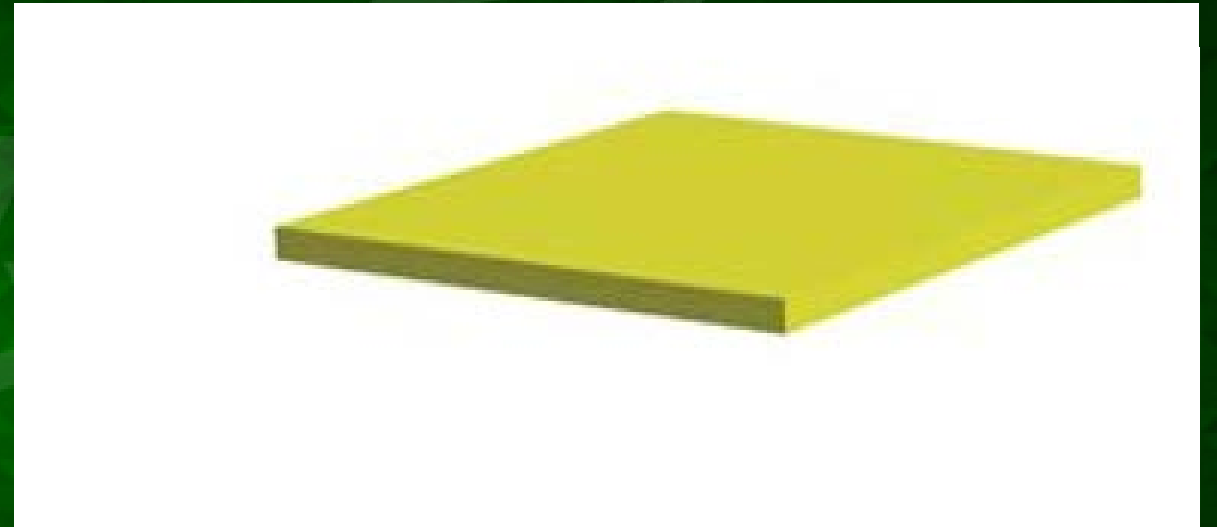
# Technology Extender: Viabond

- Viabond uses sintering paste to bond PCBs together
- Maximum PCB thickness is no longer limited by drill flute length, as each “book” is drilled individually
- Flute length limits thickness of the sub-books, but the overall PCB can be 300, 400, 500, even 600 mils thick
- Adds just one lamination cycle to fab time, as books 1, 2 and 3 are processed independently and in parallel, then the three boards/books are bonded together in a 2nd lamination step



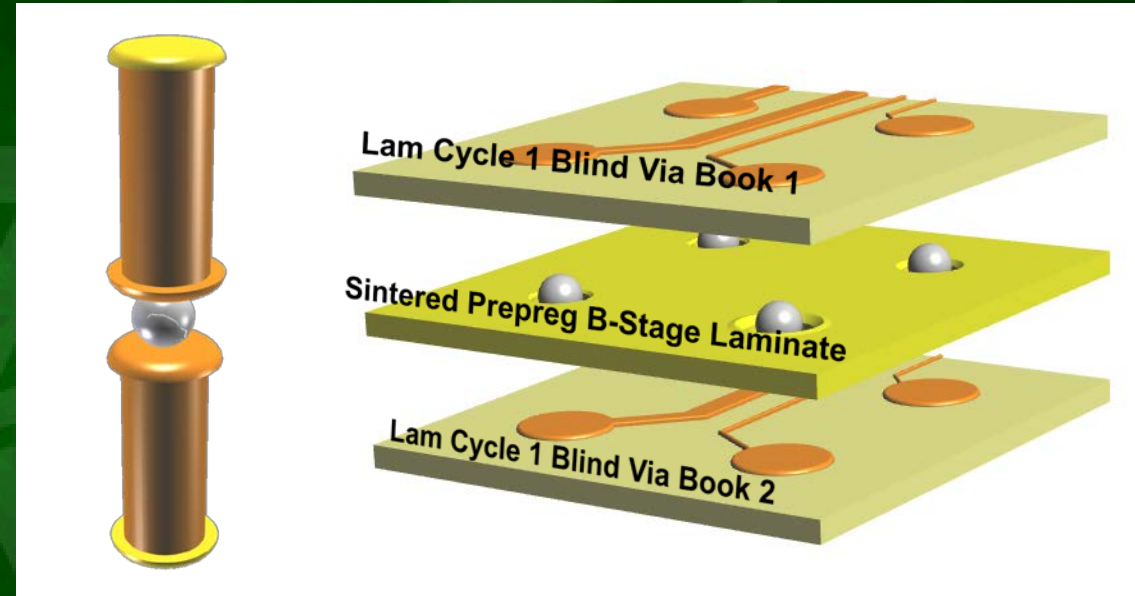
# Viabond Process

- Begin with a sheet of prepreg
- Laser drill holes in the prepreg
- Fill holes with sintering paste



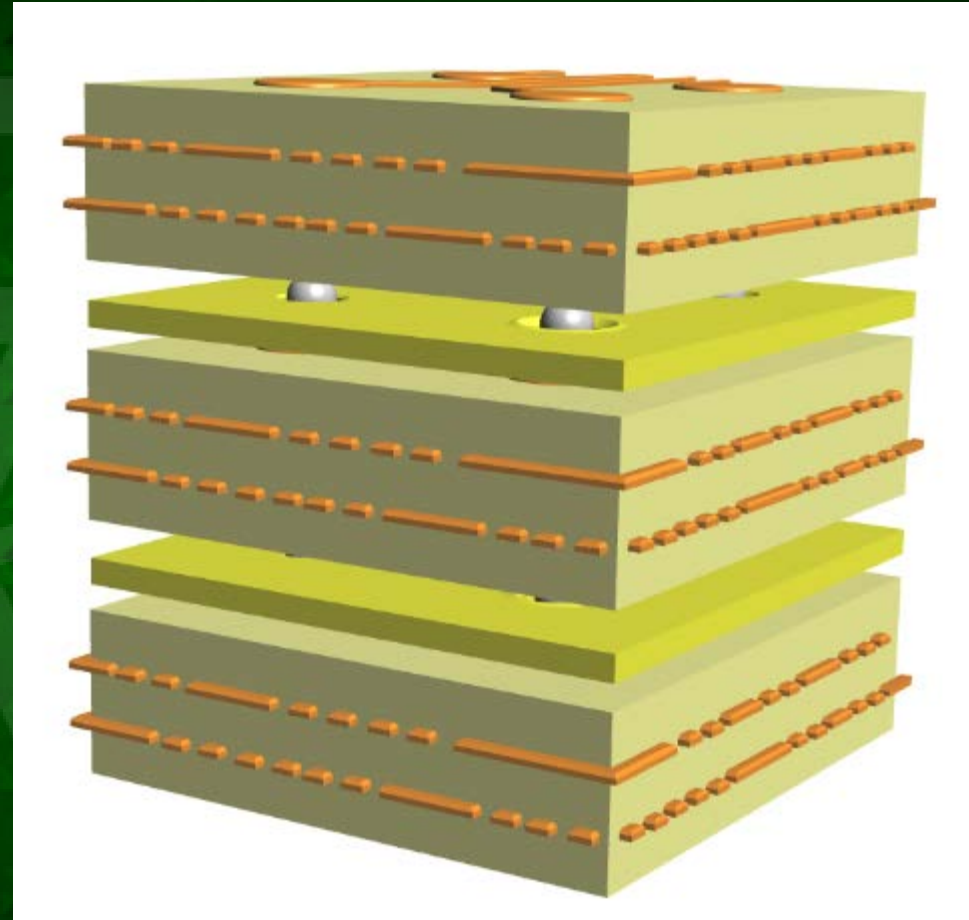
# Viabond Process

- Begin with a sheet of prepreg
- Laser drill holes in the prepreg
- Fill holes with sintering paste
- Bond books together with sintered prepreg

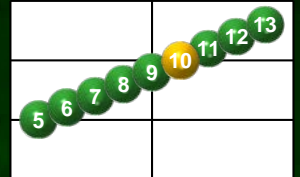


# Viabond Process

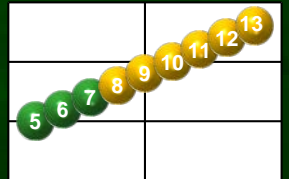
- Drill Flute length limits PCB thickness only in individual books
- Overall thickness can now be 400, 500, even 600 mils
- 2 lamination cycles
  - Books 1 - 3 are processed independently and in parallel
  - 3 boards/books bonded together in a 2nd lamination step



This



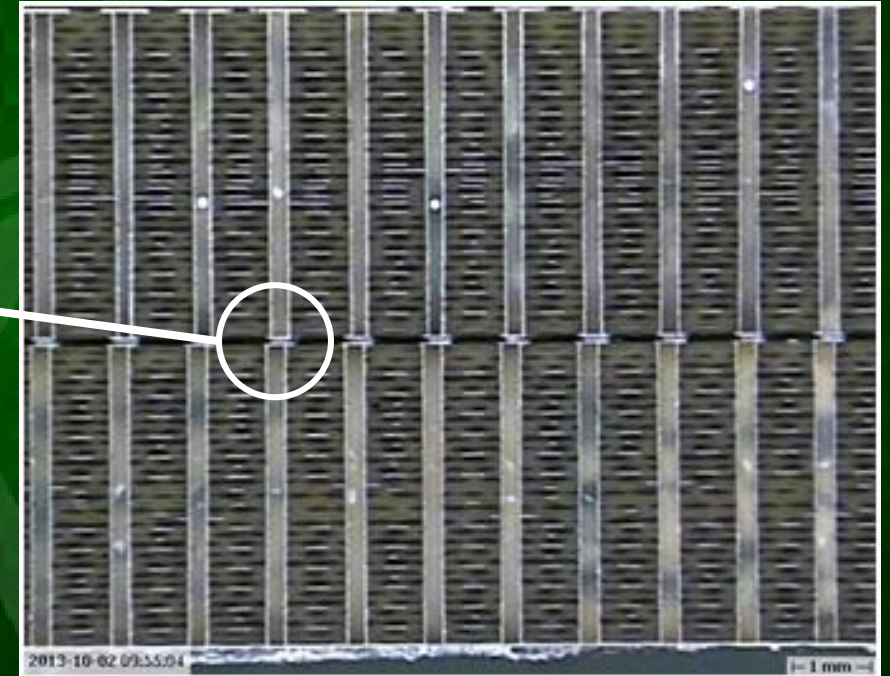
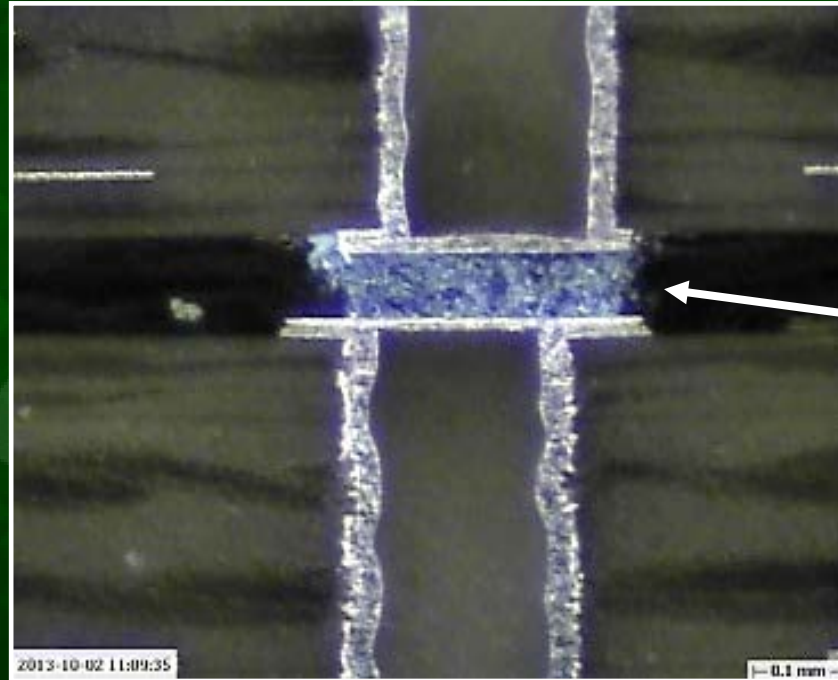
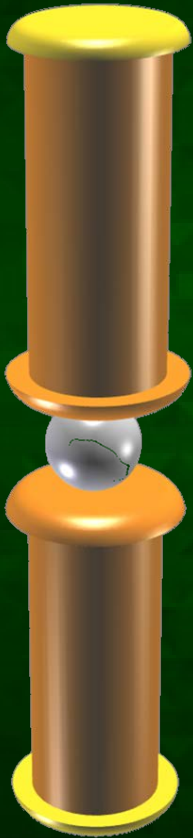
Instead of:





# Technology Extender: Viabond

- Vias are bonded together using sintering paste

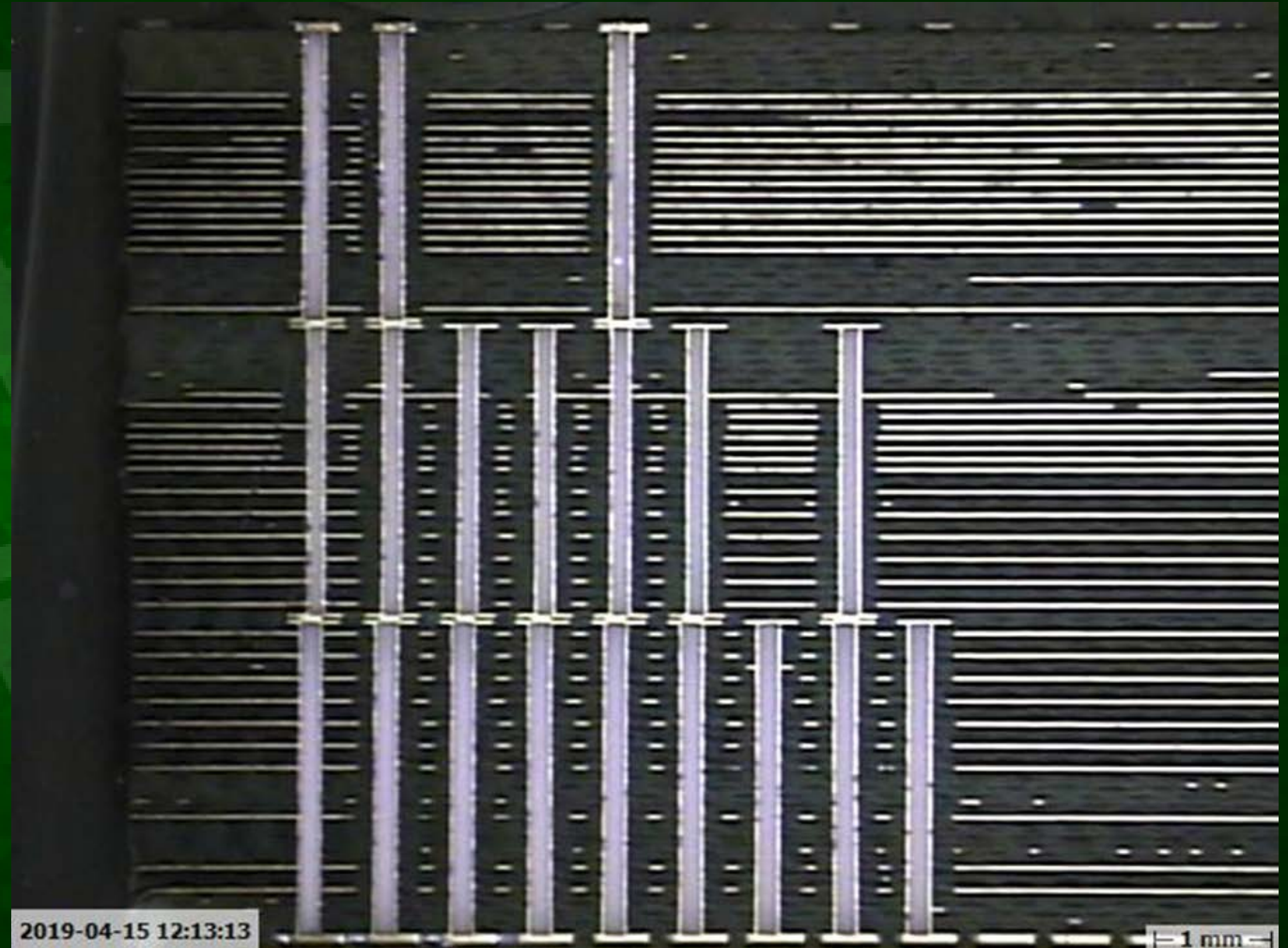
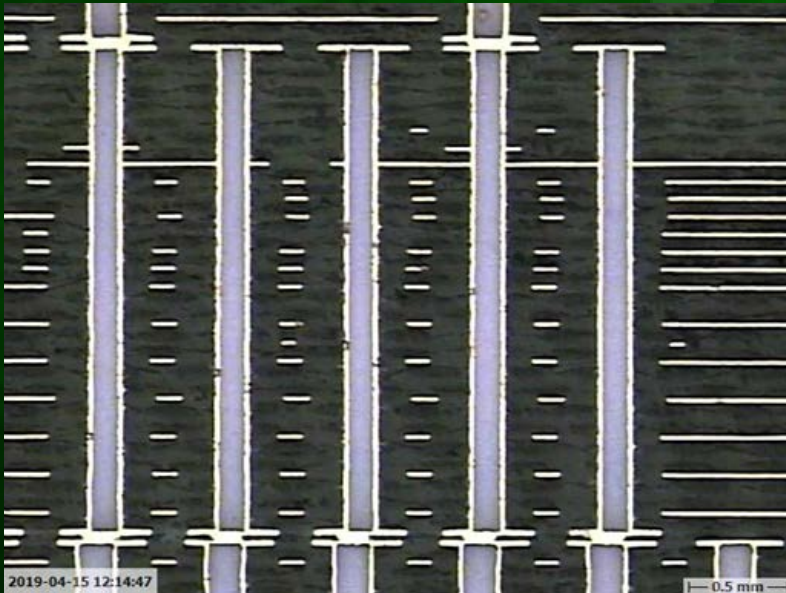


# Technology Extender: Viabond

- 3 Book Cross Section

Note:

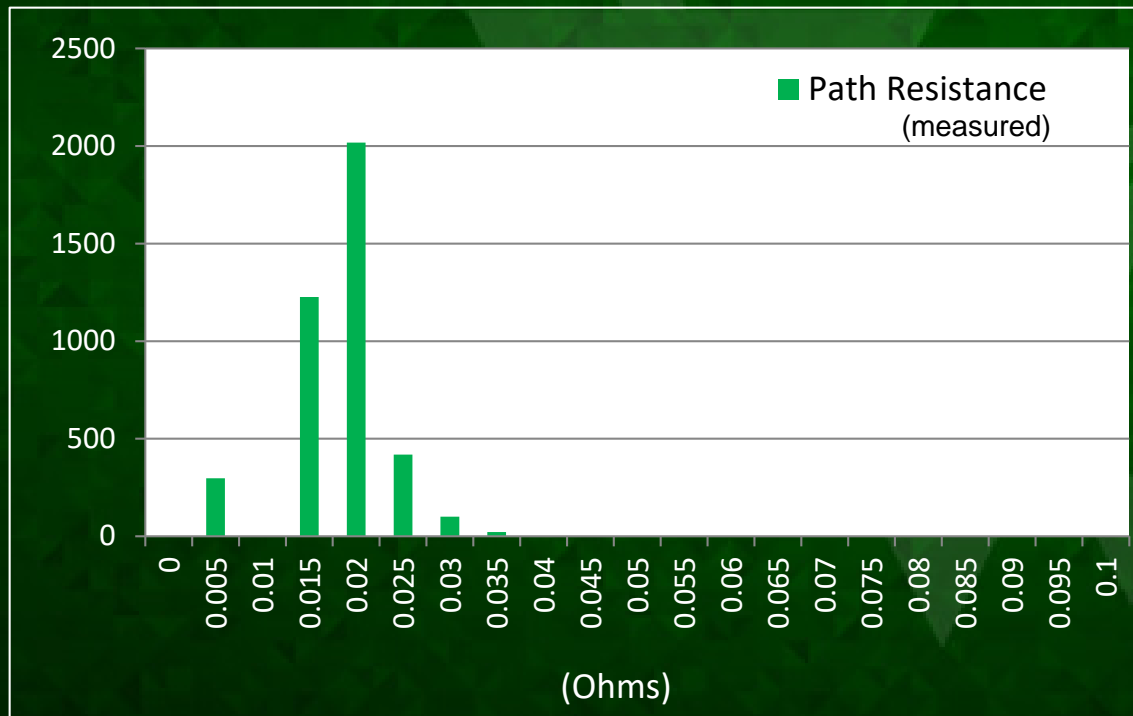
- Inner layer registration
- Registration between books



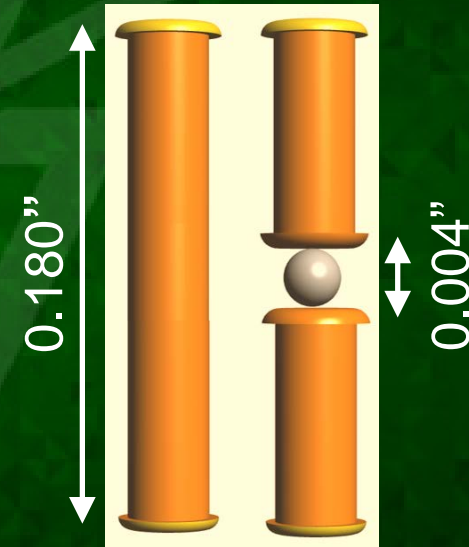


# Viabond Path Resistance

- Delta in path resistance between Cu and Viabond is negligible for signal integrity (SI) purposes, but may not be negligible for power integrity (PI) purposes



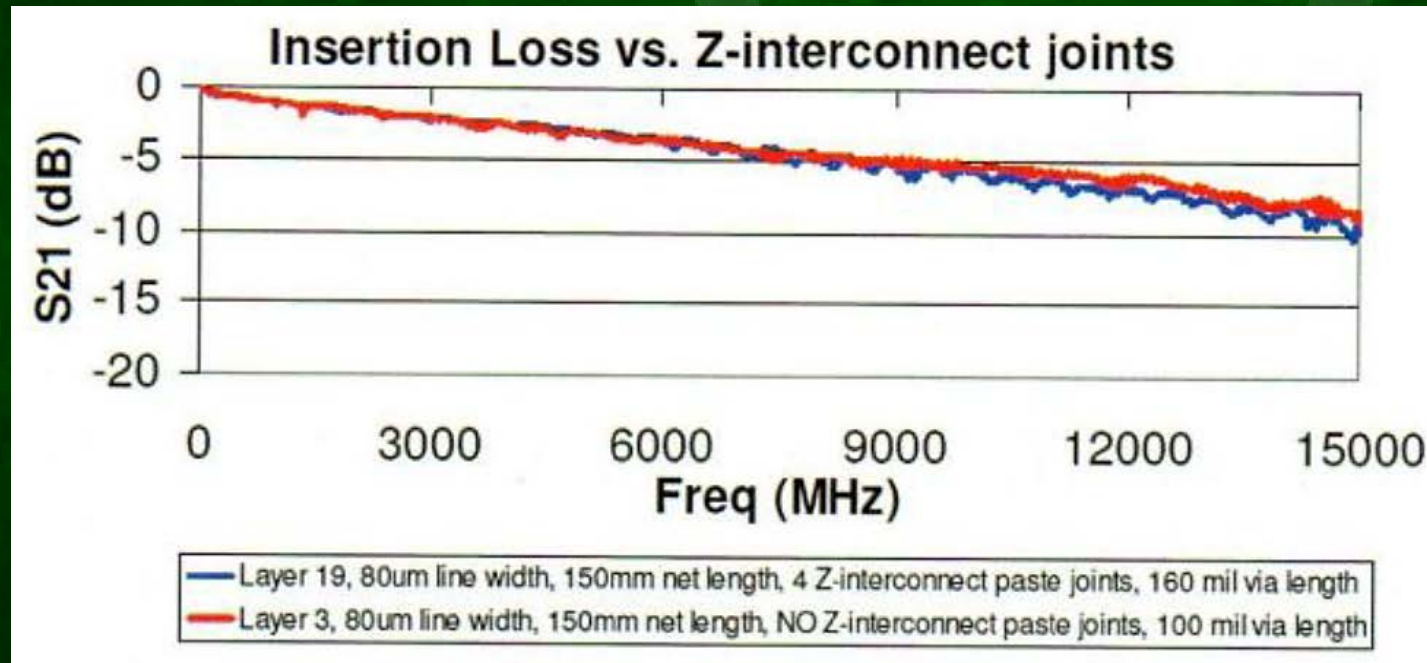
0.006" Dia. Drill on 0.180" Thick PCB



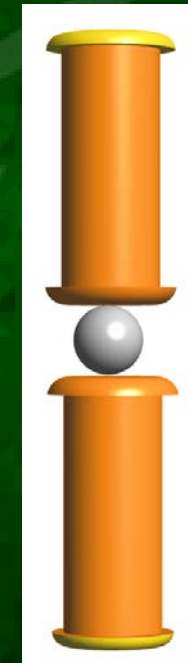
Cu = 8 mohms  
VB + Cu = \*14 mohms  
(\*Calculated)

# Viabond Signal Integrity

- Maintains signal integrity through 15Ghz when signal path traverses vias, Cu only vs Cu + sintering paste



Source: Endicott Interconnects



0.004"

~150μm

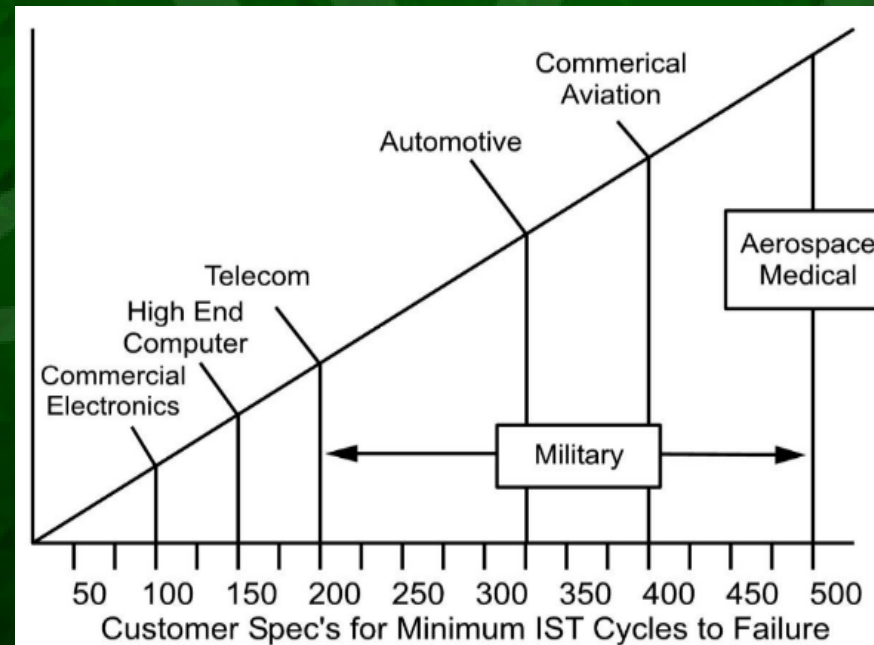
~1ps prop delay

~Invisible to 100Ghz

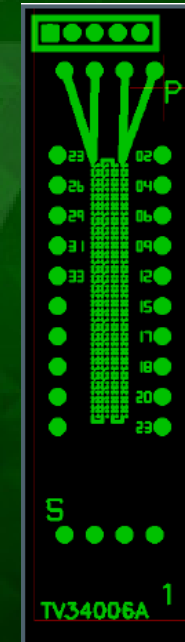


# Viabond Reliability

- Interconnect Stress Test (IST) to same standard as Harbor's traditional PCBs
  - IPC-TM-650, Method 2.6.26
  - Precondition: 9x Pb-free reflow cycles
  - Test: 1000 x 25°C-125°C thermal cycles
- 0 failures



Source: PWBcorp

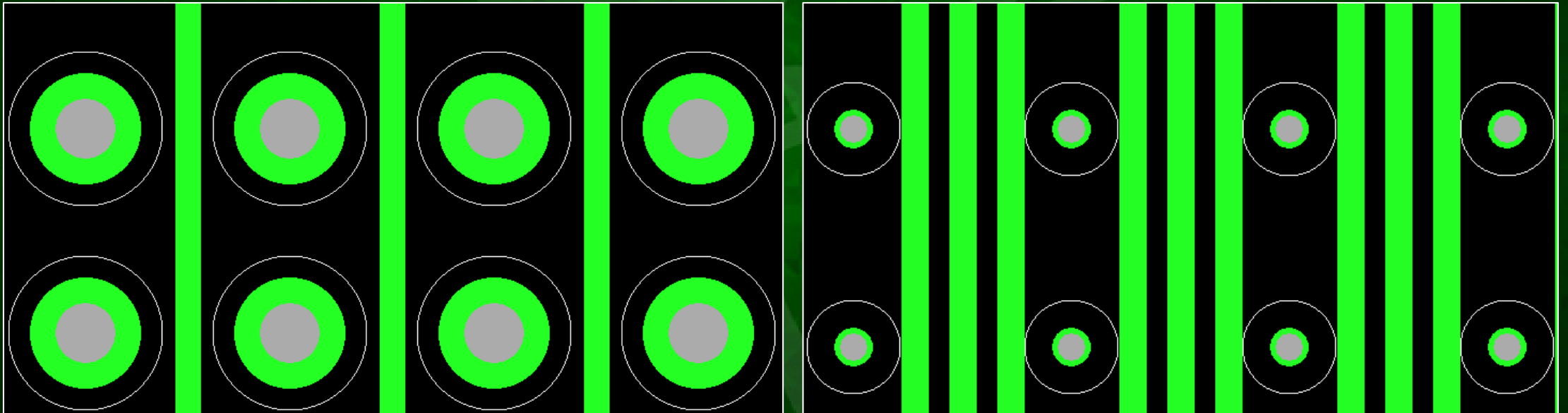


# Viabond Yield

- Yield presented the biggest challenge, took a long time to get right
- Now approaching parity with the more traditional PCB fabrication techniques
  - Sintering paste recipes are straightforward
  - Applying to ATE PCBs is another matter
  - Large form factor PCB, large number of vias
  - In-process metrology is key ( AOI, Kelvin flying probe test )

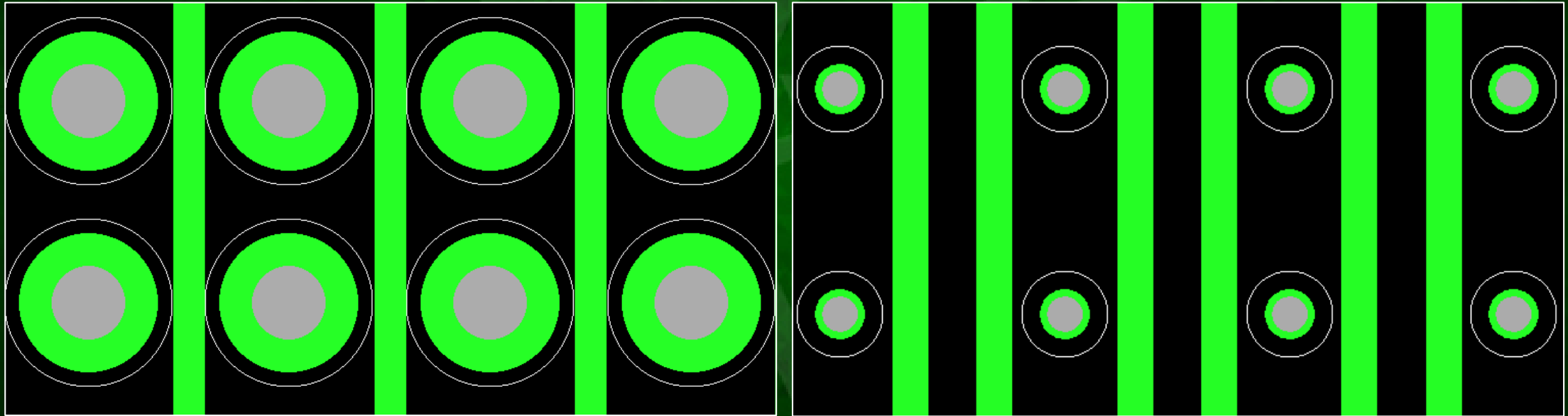
# Viabond Applications

- Overall layer count can be reduced by improving DUT area breakout routing density
- 1mm pitch: 3:1 layer reduction in signal layers



# Viabond Applications

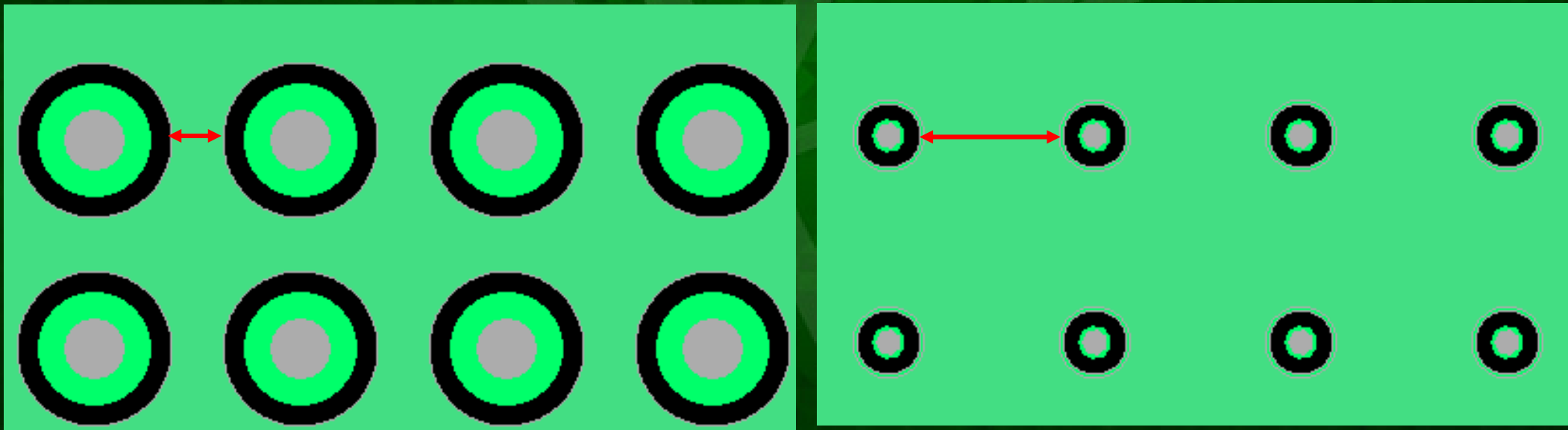
- 0.8mm pitch, 2:1 layer count reduction





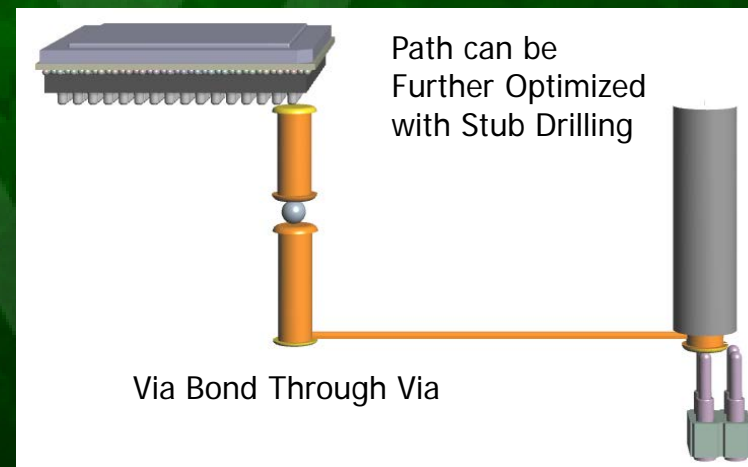
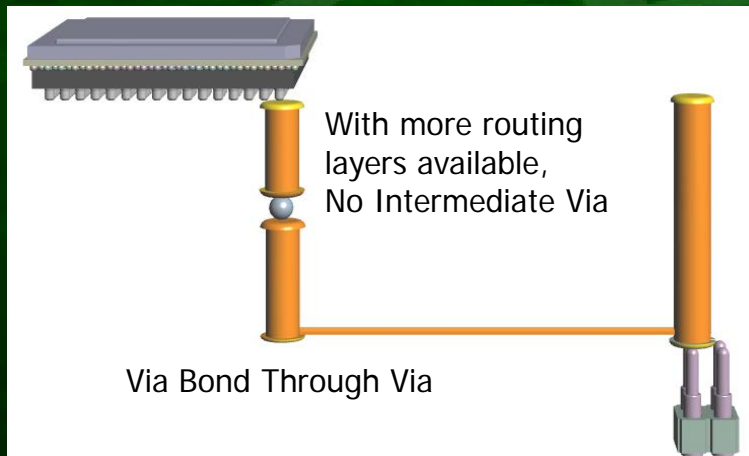
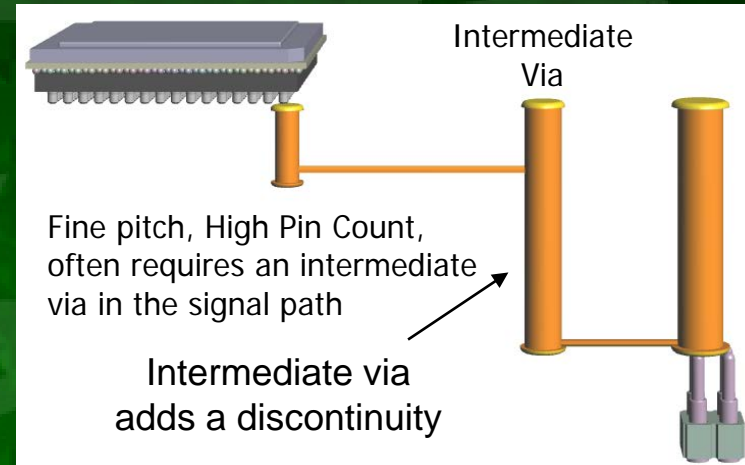
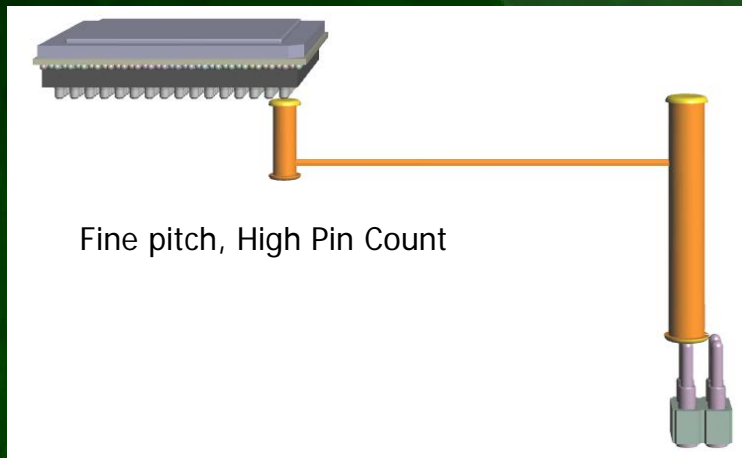
# Viabond Applications

- Power Delivery
- 1mm pitch: 180% increase in Cu width between array pins  
9.4mils -> 26.4mils, ~1/3 the path resistance  
Equivalent to using 1oz Cu vs 1/2 oz Cu



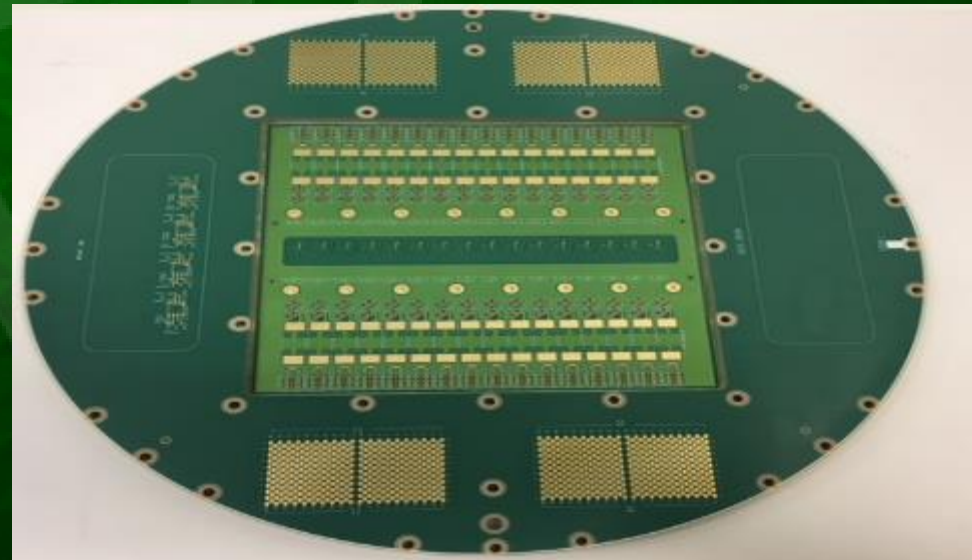
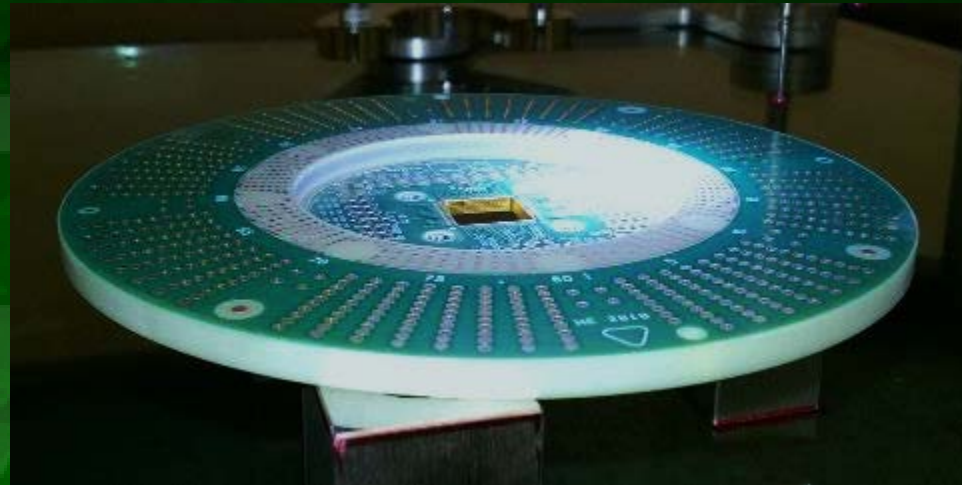
# Viabond Applications

- Simplifies fanout, can improve signal integrity for fine pitch / high pin count DUTs



# Noteworthy Viabond Applications

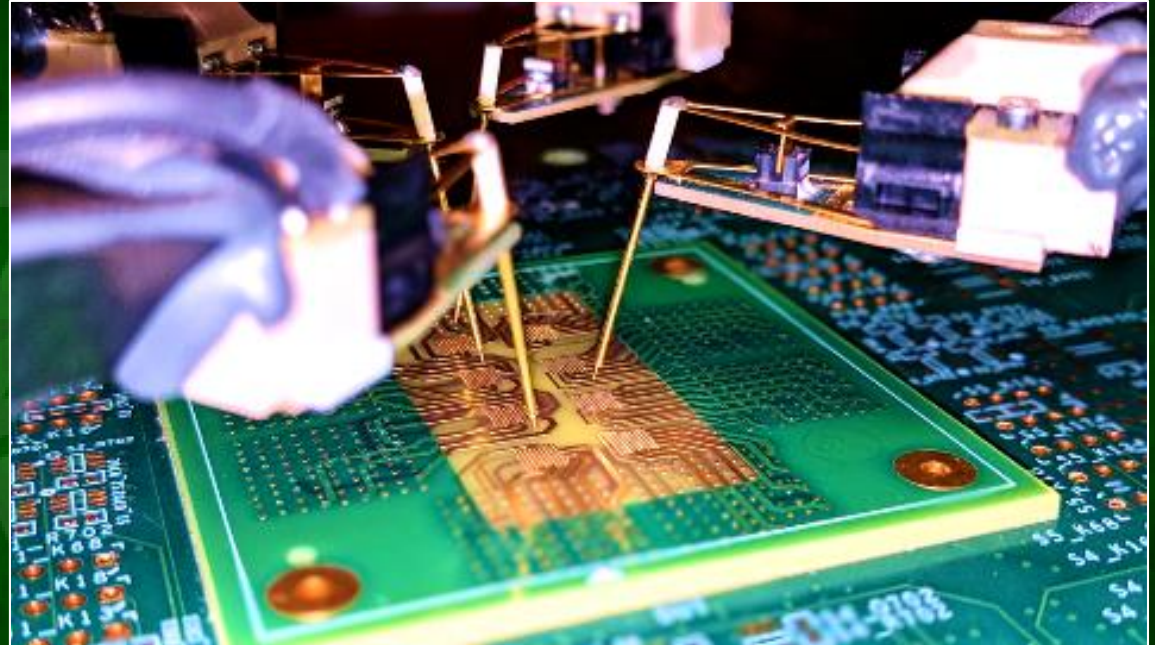
- Multi-tier PCB
  - 0.65 mm pitch, 0.590" thick PCB
  - Recessed cavity
  - 10,000 Viabond interconnections
  - Board alone weighs 25 pounds!
- Multi-tier PCB
  - 0.35mm pitch, 0.310" thick PCB
  - Recessed cavity, 16x site
  - 36 layers





# Noteworthy Viabond Applications

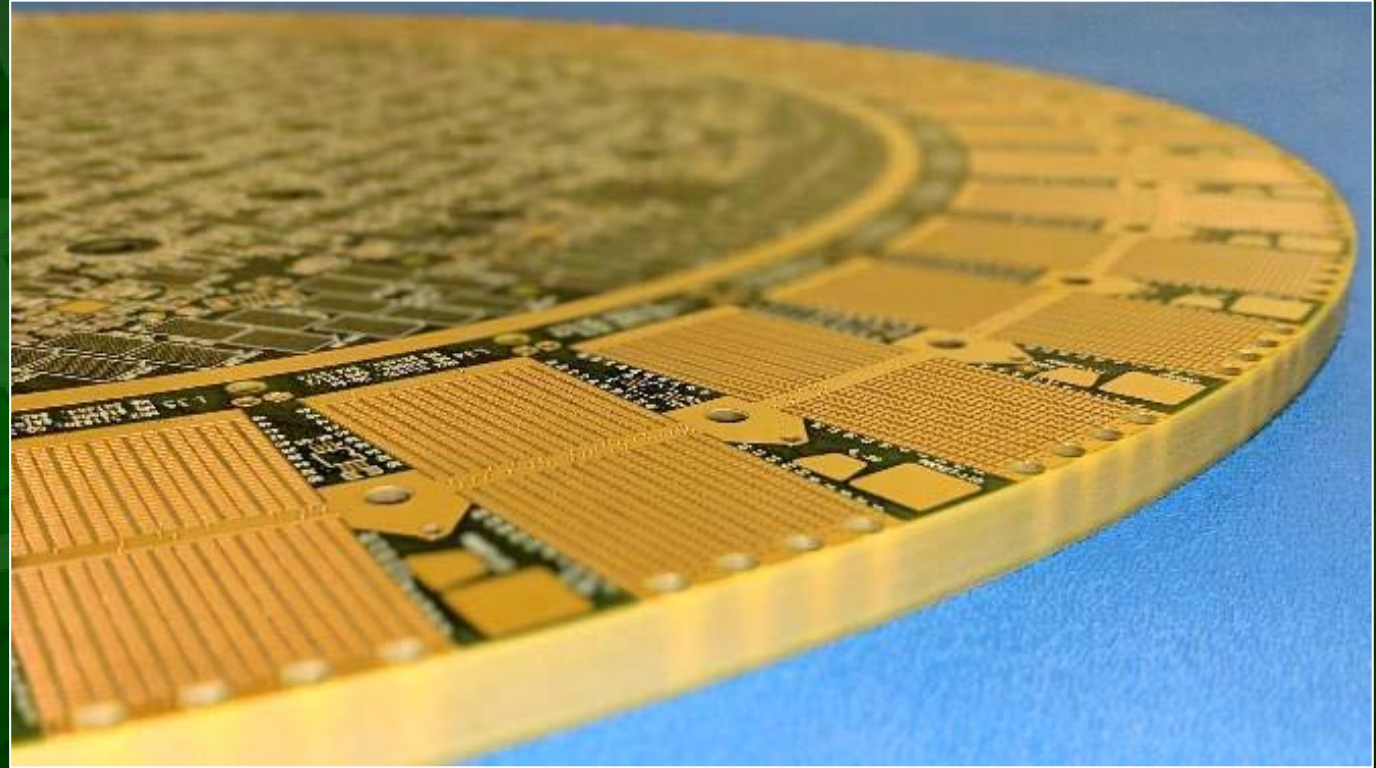
- Motherboard – Daughterboard
  - Daughterboard:  
Fine pitch, higher cost PCB
  - Motherboard:  
Gross pitch, low cost PCB
  - Space transformation from  
PCB pitch to IC package pitch
    - At DUT site or to adapt to  
specialty component  
footprints





# Noteworthy Viabond Applications

- Memory test application
  - 0.335" thick PCB
  - 0.50mm pitch
  - 81 layers
  - 3 books, 2 Viabond layers
  - 100,000 Viabond junctions



# Future Applications for Viabond










- Incorporate fully additive 3D printed solutions
  - Conductor dimensions at 3mil line and space now
  - ATE XYZ dimensions not yet available, ATE layer counts not yet available
  - Hybrid structures may have legs:
    - 3D printed small feature structure laminated to standard PCB using Viabond
- To Be Determined
  - Will be driven by market need and customer creativity

# Viabond Next Steps

- Continue to Improve Routing Lanes ( smaller diameter Viabond interconnects )
- In-depth Power Integrity characterization
- Signal Integrity / via tuning
- Simulation to measurement correlation
- In-process metrology continuous improvement
- Space transformer integration studies
  - Flatness
  - Design & fabrication timeline compression
  - Compare viabond to solder attach + underfill

# Summary:

- Viabond extends the reach of what can be achieved in the ATE Interface PCB
  - Thicker, high aspect ratio, high layer count PCBs
  - Fine pitch plated holes ( small drills ) through thick PCBs
  - Alternative to sequential lamination, with fewer lamination cycles

|                  | Flip Drilling   | Multiple Laminations  | Backdrilling  | UltraFlat   | Viabond   |
|------------------|---|---|---|---|---|
| Layer Count      |    |    |    |   |    |
| DUT Pitch        |    |    |    |   |    |
| Routing Density  |   |    |    |   |    |
| Signal Integrity |   |  |  |   |  |
| Power Delivery   |  |  |   |   |  |
| Direct Attach    |   |   |   |  |  |