SWTEST

PROBE TODAY, FOR TOMORROW

# A Journey to Achieve Lower Test Cost - Massive High Multi-site

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# Overview

- Introduction
- Methods
- Results
- Conclusion
- Follow-On Work

# Introduction

- Cost of test plays a significant role in COB ( Cost of Build)
- As lowering test cost has become increasingly important, Massive multi-site is essential for wafer probe to further reduce test cost
- This presentation will guide you on the journey to lower test cost by designing massive multi-site for microcontroller class of circuits
- Numerous challenges had to be resolved in order to achieve our multi site target

# Methods

- **Introduction**
- **Methods**
  - Device under test
  - Probe solution selection
  - Test resource constraint identification
  - PCB component area estimation
  - Layout consideration
- **Results**
- **Conclusion**
- **Follow-On Work**

# Methods-Device Under Test

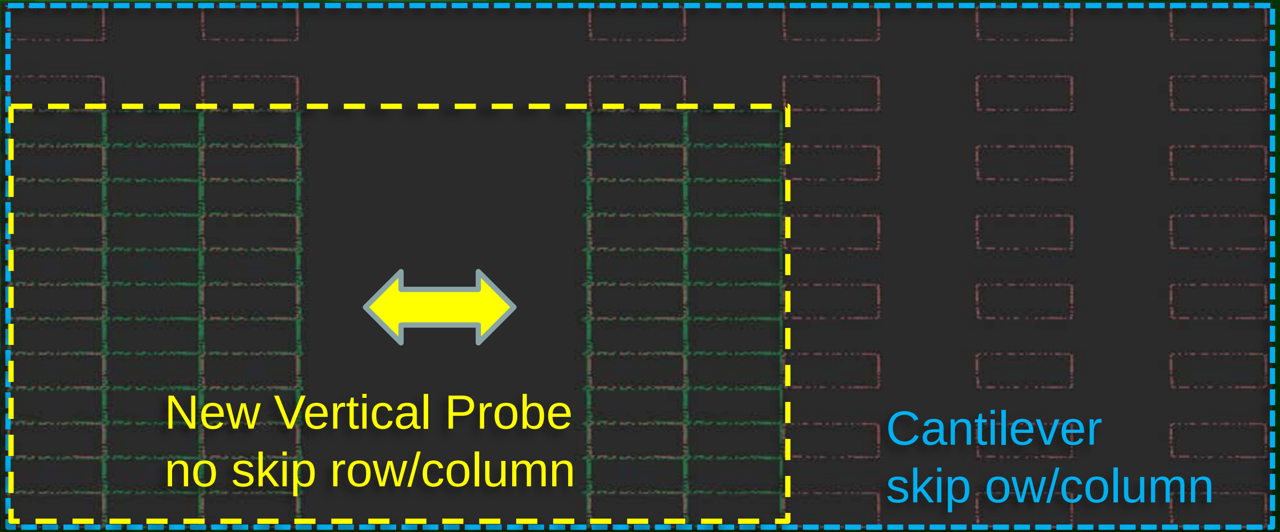
- **The DUT (Device under Test) is a microcontroller with integrated high performance analog IPs**
- **The target multi-site for the DUT is 50% more than its predecessor (N sites)**

| **Device Feature** | **DUT vs Predecessor** |
|---|---|
| Processor | 50% more |
| Memory (Flash, Ram) | 50% more |
| Peripherals IPs | 20% more |
| Die Size | 30% more |
| Analog IP( high performance ADC, DAC, Comparator, etc) | Same |

# Methods-Probe Solution Selection

- The predecessor was N sites cantilever solution
- Target site count for our new DUT is 1.5N sites to further reduce test cost
- Vertical Probe was selected for the new DUT because of its compact and high density design that supports the target site count

| Probe technology | Cantilever | Vertical Probe |
|---|---|---|
| Maturity | Matured | New |
| Site | 0.8N | 1.5N |



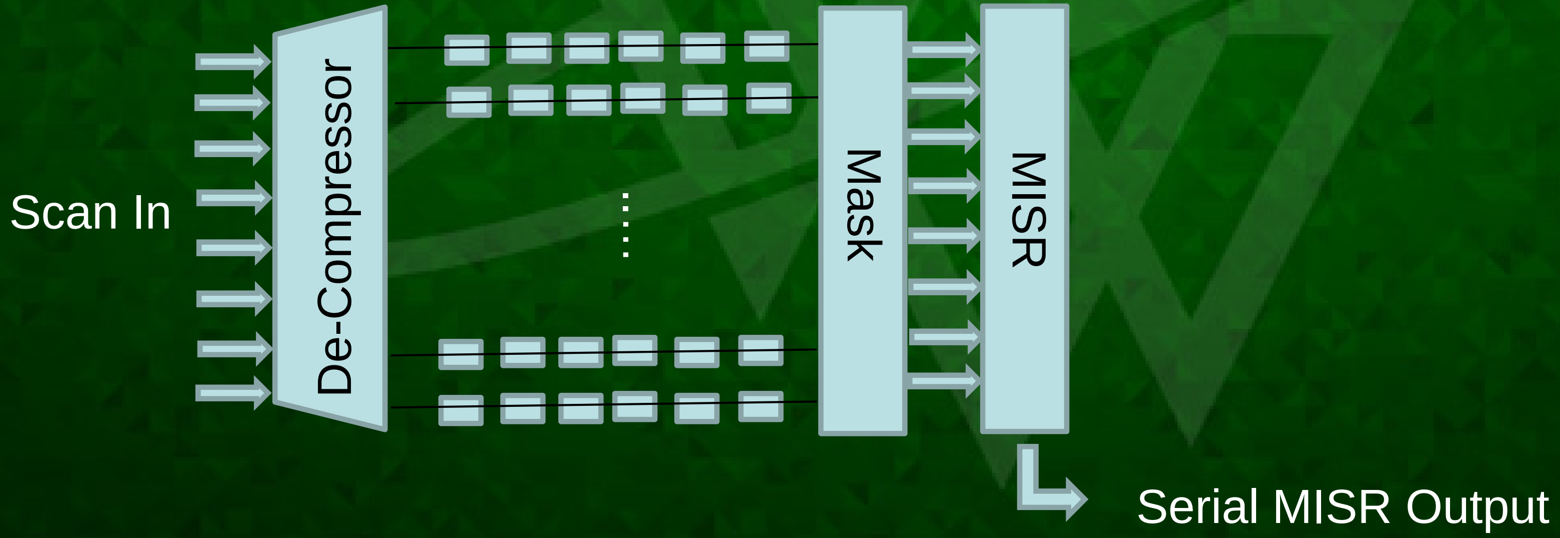
# Methods- Resource Constraints Identification

- **The 50% increase in number of sites from the previous design resulted in insufficient dedicated resource in almost all ATE instruments**

| ATE Instrument | Available Resource | Resource Needed 1.5N sites | Final Resource 1.5N sites w/sharing | Solution |
|---|---|---|---|---|
| Digital channel | 16N | 22.5N | 15N | On chip DFT with reduced scan-in/scan-out |
| Analog channel | N | 1.5N | 0.75N | Shared between sites using Relay |
| Power supply | 6N | 7.5N | 6N | Ganged Digital and Analog supply using Noise coupling isolation |
| Hi-Res Analog force | 2N | 3N | 1.5N | Shared between sites using Relay |
| Hi-Res Analog capture | 0.5N | 1.5N | 0.5N | Shared among sites using Relay |
| Hi-Res Reference | 2N | 1.5N | 1.5N | N/A |

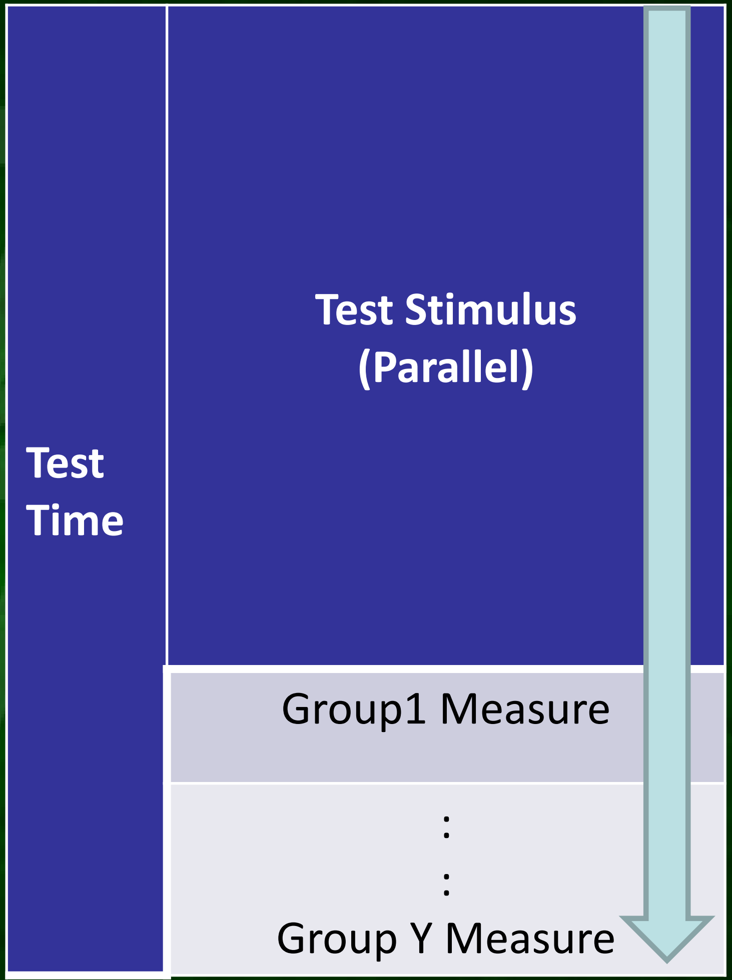
# Methods-DFT

- **Scan Compression, such as MISR (**Multiple Input Signature Register ), **supports high multi-site with reduced scan input pins.**
- **Parallel application of scan data from De-Compressor also greatly reduces scan test time.**



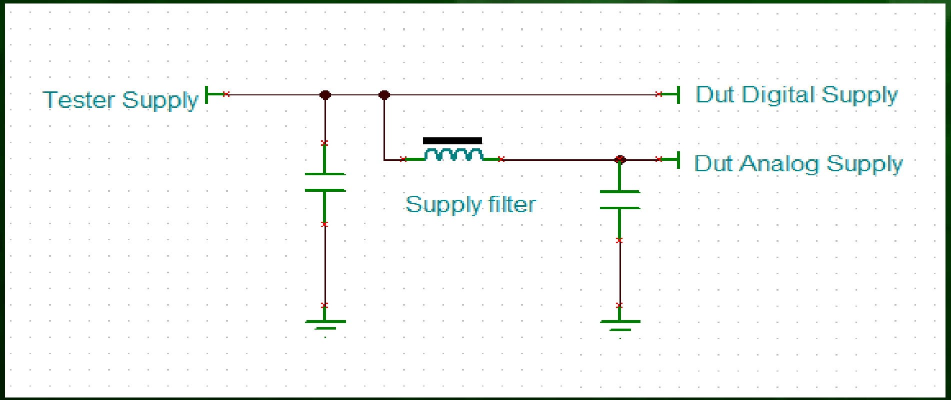
# Methods-Muxing

- **The signals using the following instruments can be shared by sites with relays or mux**
  - Digital Channel
  - Analog Channel
  - Hi-res Analog Force
  - Hi-res Analog Capture
- **Due to the nature of sharing, additional test time will incur due to serial testing but it is generally a small portion of total test time**

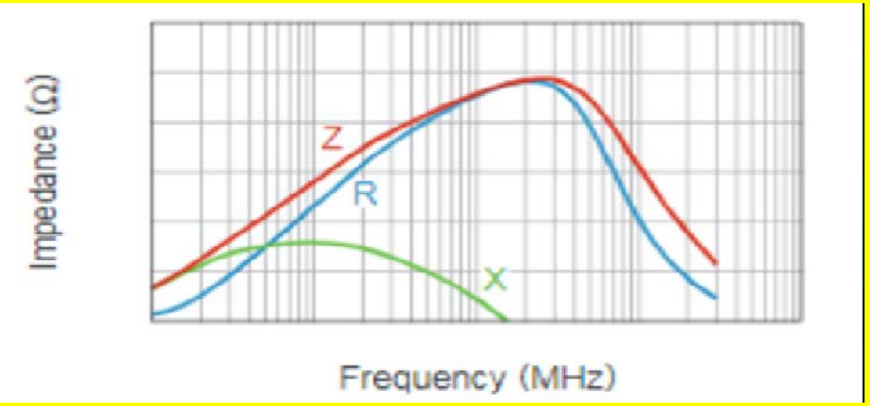


# Methods-Noise coupling isolation

- **Noise coupling isolation filter attenuates high-frequency signals from digital supply that can propagate into critical analog supply. At high frequency, the resistance of the filter dominates, hence the noise will not pass through**
- **This filter reduced 1.5N tester supplies and incurring very small component area**
- **Based on the DOE(Design of experiment), analog performance was comparable between separate digital/analog supply vs gang digital/analog supply with noise coupling isolation filter**



Noise Coupling Isolation Characteristic

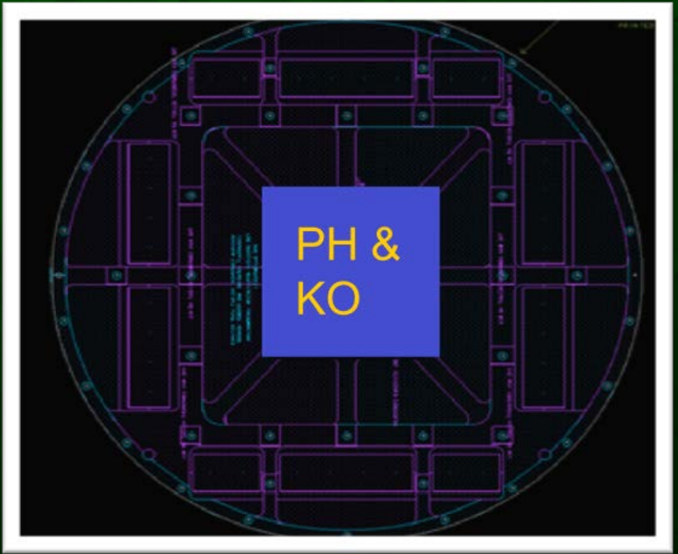


# Methods-Estimate PCB Component Area

- **Total Component Count**
  - 4500 Capacitors & Resistors
  - 288 Op Amps
  - 1106 Relays

- **Because the DUT has high performance ADCs , many active components(Op amp) are added to improve the source bandwidth, which was not in the previous design**
- **Component area can be calculated from each component's dimension to reduce the risk of PCB placement surprises**
- **Available Component Area = (Board Area – PH Keep out – Stiffener keep out – Pogo Area) * Routing Margin**
- **Component area 64% utilization → low risk with placement**

| Components | QTY | Component Area ($mm^2$) | Total Area ($mm^2$) |
|---|---|---|---|
| Size1 CAP & Resistor | 3063 | 1.28 | 3921 |
| Size2 CAP & Resistor | 1432 | 2.5 | 3580 |
| Relay | 1106 | 3.78 | 4181 |
| Opamp | 288 | 15 | 4320 |
| Total Component Area | | | 16001(64%) |



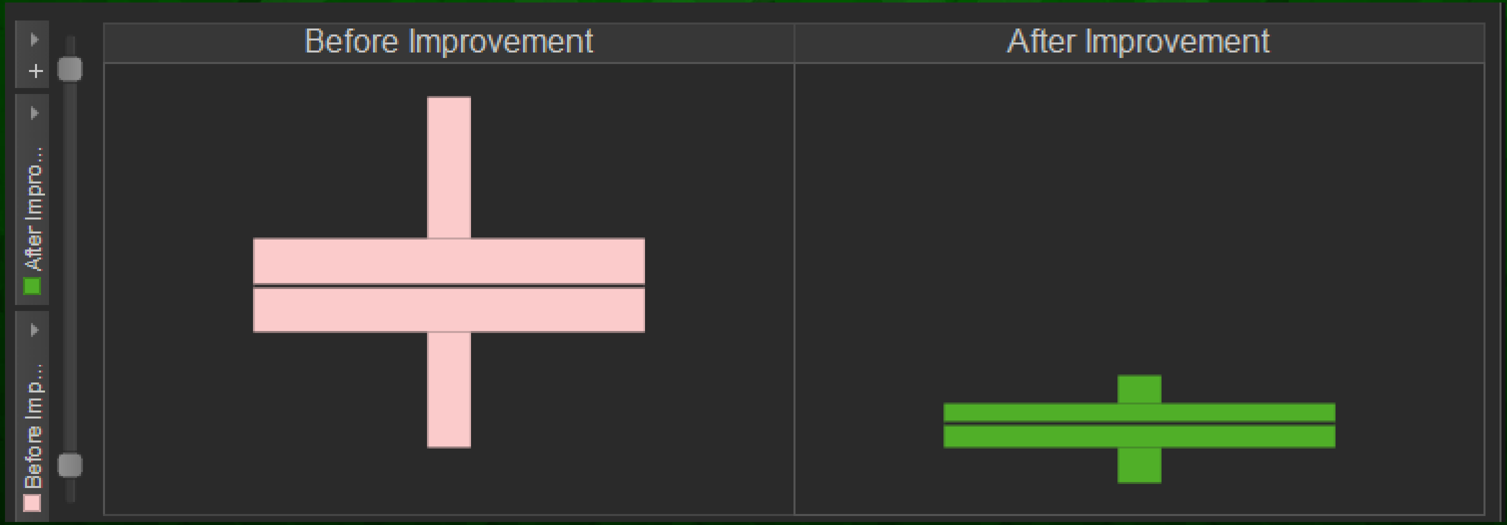
# Layout Consideration

- Maximum layer count for PCB is 50+ due to PCB thickness restriction
- PCB layout is critical to ensure optimum analog performance and minimal site to site noise coupling issues. Therefore sufficient isolation between analog and digital layers is very important
- Due to the large amount of signals for 1.5N sites, it was difficult to estimate the # of layers required. As a result, 4 Digital pins were not routed and the test coverage had to be moved to package test

| Layer Stack |
|---|
| Top |
| Analog |
| Digital |
| Relay Control |
| Analog |
| Supply |
| Analog |
| Bottom |

# Results

- Test Cost per die $= \frac{Tester\ Hour\ Rate}{3600} * \frac{Test\ Time(s)*PTE}{\#\ of\ sites\ *Yield}$
- Test Cost Reduction = 1 - $\left(\frac{\frac{Tester\ Hour\ Rate}{3600} * \frac{Test\ Time(s)*PTE}{1.5N\ *Yield}}{\frac{Tester\ Hour\ Rate}{3600} * \frac{Test\ Time(s)*PTE}{0.8N\ *Yield}}\right)$ * 100%
- **1.5N massive multisite solution resulted in massive test cost reduction of 25%**
- **Added active components resulted in significant improvement on ADC tests**



# Conclusion

- Massive multi-site solution resulted in 25% reduction in test cost.
- Savings from increase of parallel testing outweighs the loss of efficiency in serial testing due to ATE resource sharing.
- The added complexity of analog IPs did not deter us from taking the road less traveled. We were able to work through the challenges and achieve lower test and better analog performance

# Follow-on work

- **Develop high PTE test to reduce the penalty of going high multi-site. For example : CPU based BIST tests**
- **Develop method to estimate layer count and reduce site to site variation through simulation up front**

# Acknowledgement

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