SWTEST

PROBE TODAY, FOR TOMORROW

2023 CONFERENCE

Enabling High-speed Loopback Tests for Serdes, PCIE Gen5/6 on Probe Using Embedded Capacitors on the MLO

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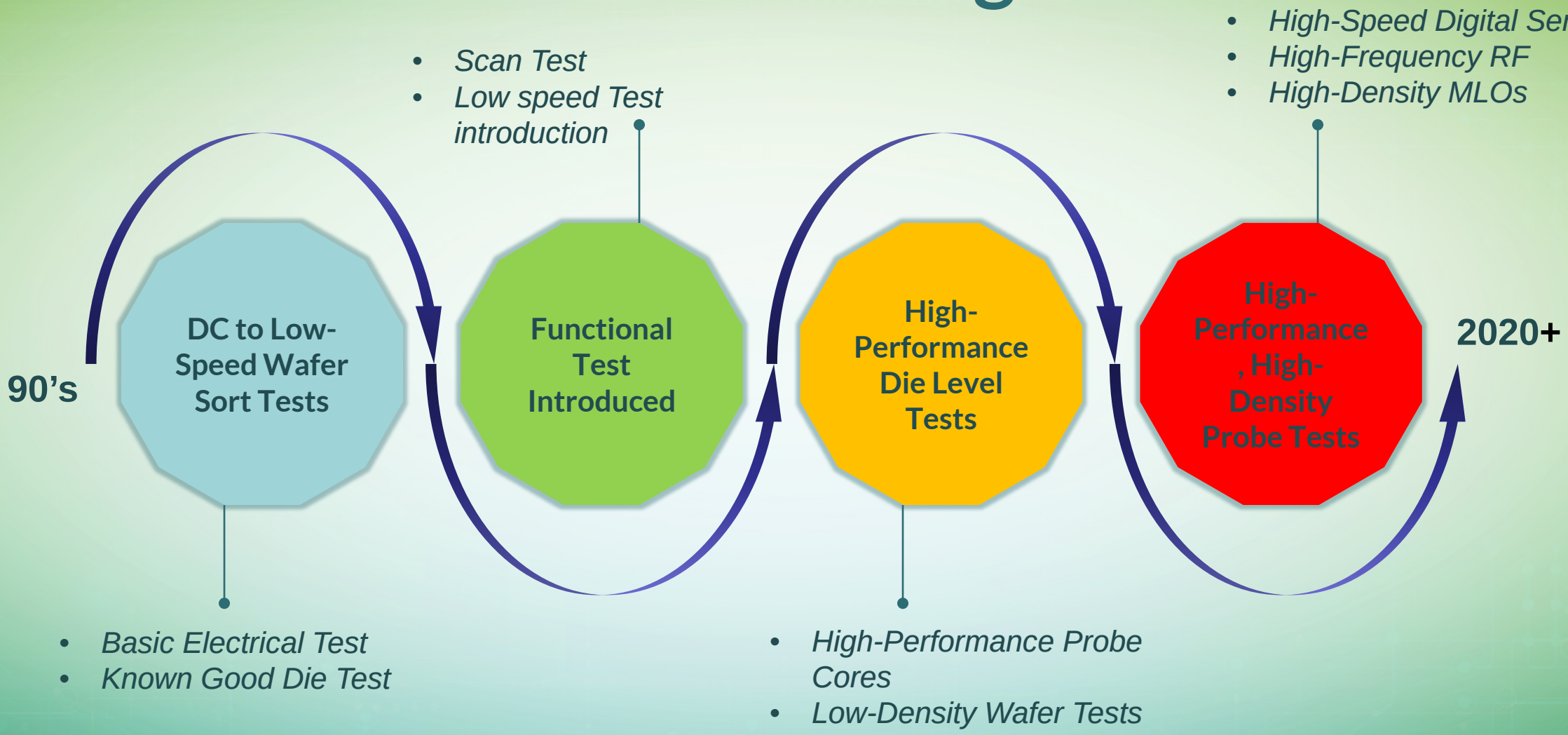
Agenda

- Wafer Test: The Need for Speed!
- Embedded Components and MLOs
- Technology Overview: Enabling High-Speed Testing on Probe
- Design, Development and Measurement Test Setup
- Measured Performance and Simulation Correlation
- Performance Comparison – ECMLO Vs. Traditional Probe PCB
- Reliability and Thermal Tests
- Conclusion

A New Paradigm

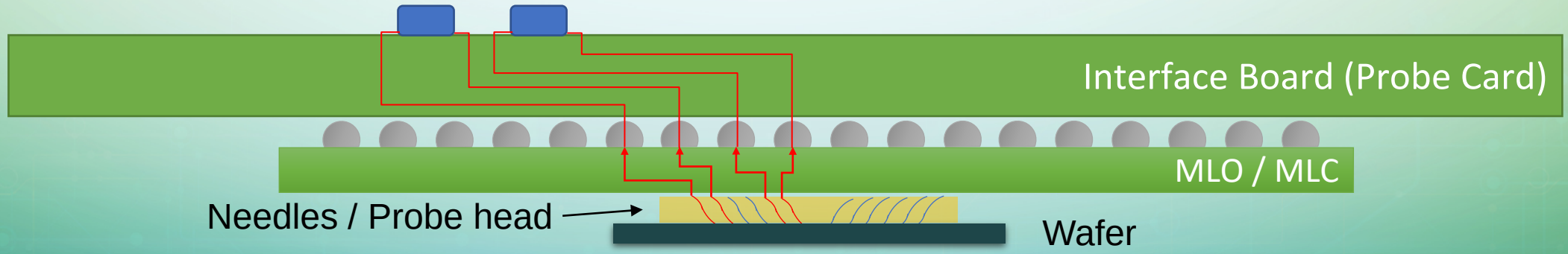


High-Speed Digital and RF Wafer Probing

High-Performance probe cores are available in the market

- High-density and high-performance MEMs type pins are available
- High-performance cores are available
  - Limited density with high performance
  - Limited number of dies

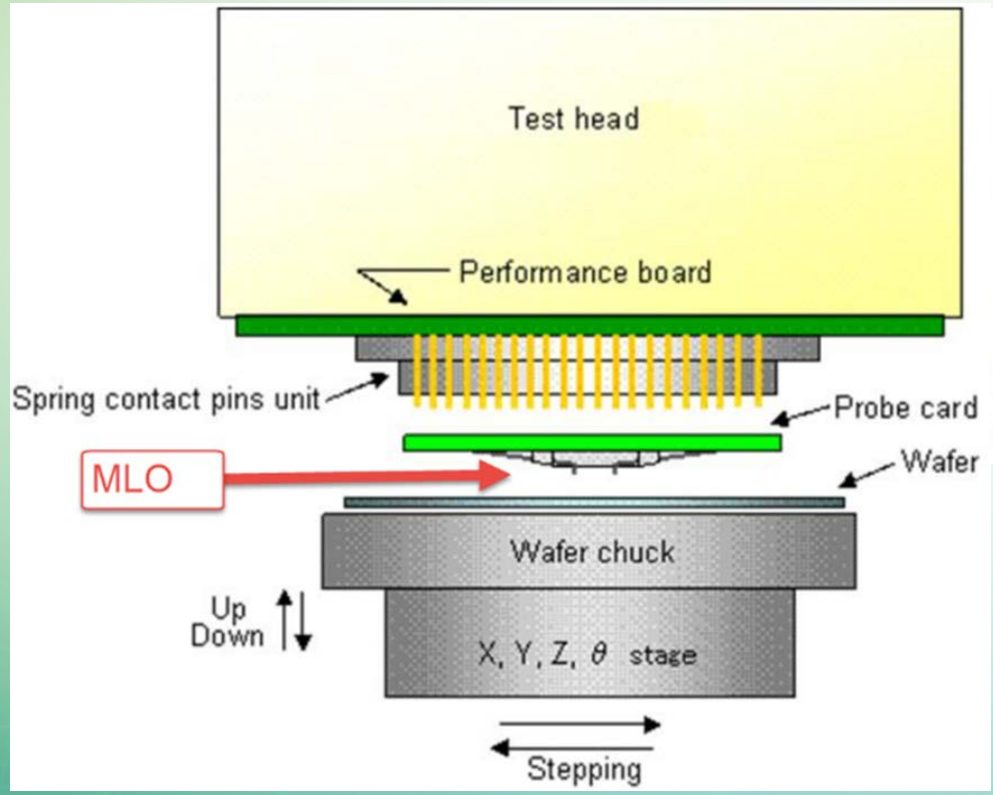
At probe, the high-speed digital signal traverses a series of interconnects. All interface hardware has its own sets of keep-outs.

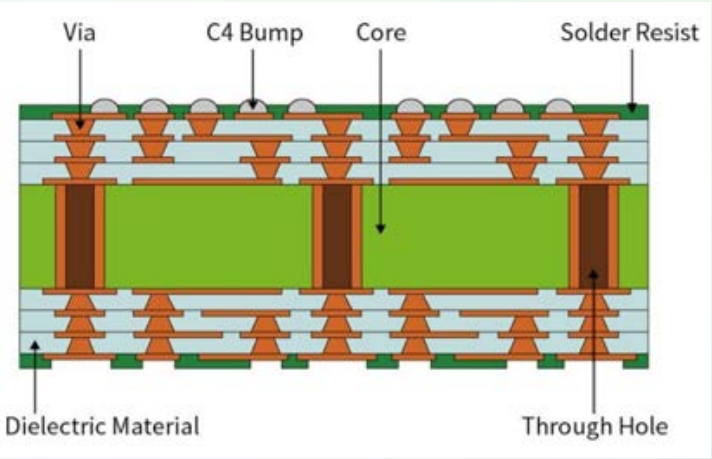


Multilayer Organic (MLO) PCBs

Essentially a PCB-based pitch translation technology

- Different from MLC (Multilayer Ceramic) transposers

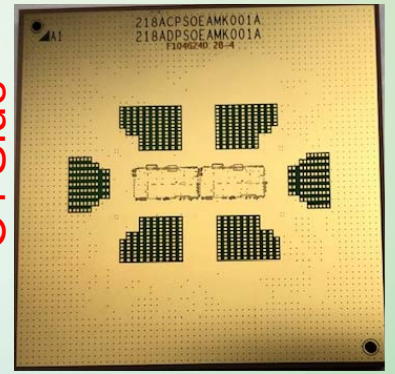


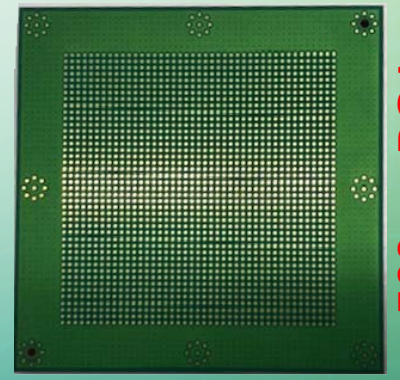


MLO Stack usually referred to X + N + X

X = Buildup layers on top and bottom
N = Number of layers in center core

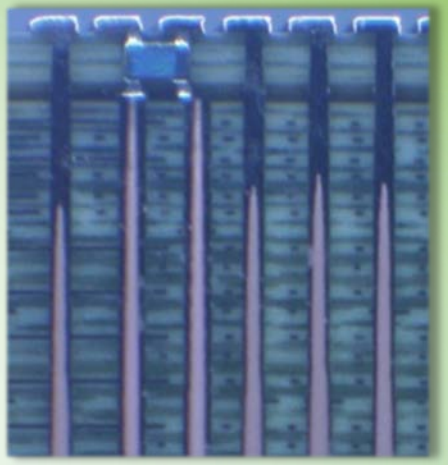
e.g.
12 + 30 + 12 means 12 buildups on top and bottom with a 30-layer center core



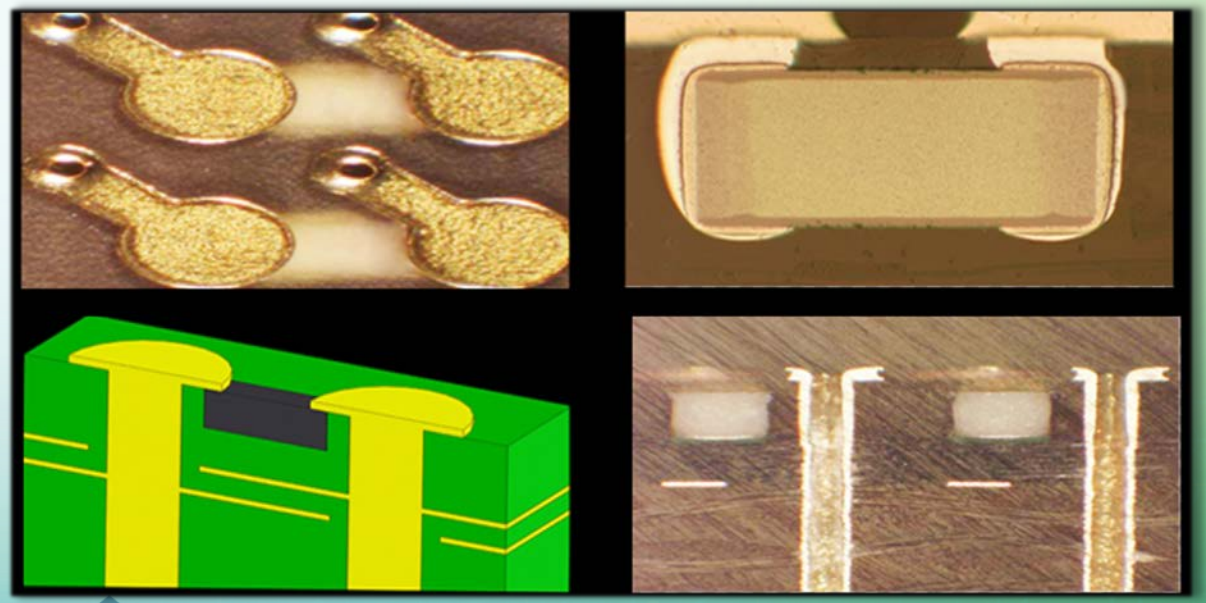


Embedded Components Overview

Physical capacitors embedded in the PCB board

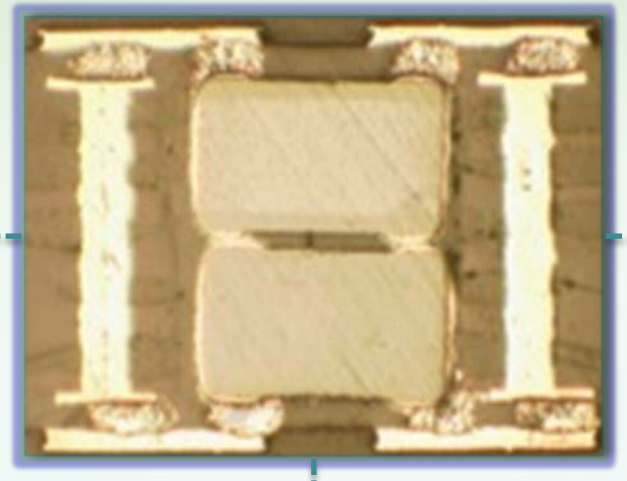


- DUT Pitch >= 0.4mm on final test ATE boards
- 01005, 0201, 0402 and 0603 case sizes
- Capacitance values up to 2.2uF
- Embedding
  - Thin film resistors
  - Capacitors
  - Chip inductors
- Stacked capacitance allowed
- MLO embedding allowed with 01005 or 0201 case capacitors/resistors

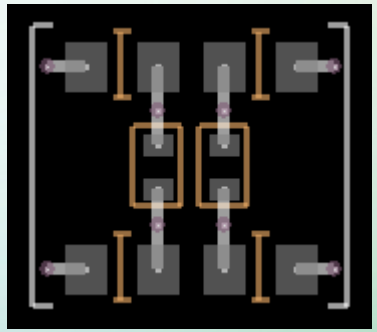


Embedded Component Applications

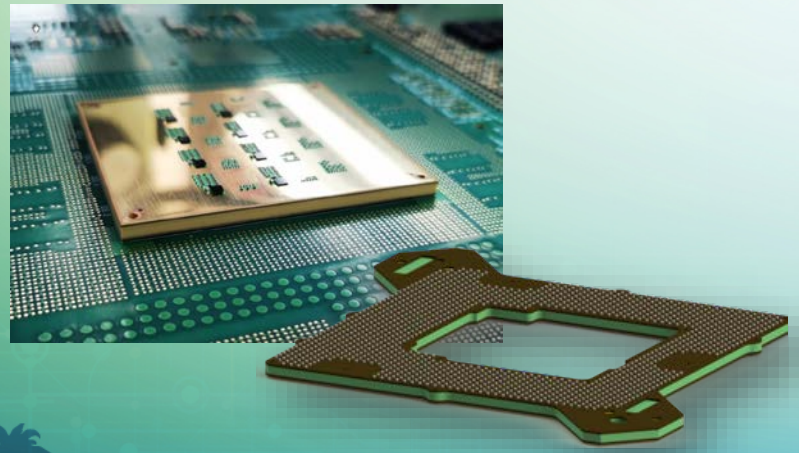
Embedded capacitor for power integrity
- DUT Boards and MLOs with embedded components
- Embedded component interposers attached via invisipin interposer technology



High-Performance probing and other applications
- Embedded resistors
- Embedded chip inductors



High-Performance loopbacks
- Loop back capacitance
- RC/LC based bias tees



Solution: Embedding Loopbacks on MLO

Eliminates the extra layer of interconnects and reduces losses

- Capacitor is embedded in the center core of the MLO
- An optimized through via through the center core connects the capacitor to an RDL layer
- Mostly stub-free design because HDI technology enables performances at DC to higher frequencies
- High-density loopback component embedding is possible depending upon the device die map
- RC based or LC-based (chip inductors) biased-T loopback circuit is acceptable to enable high-performance loopback and ATE parametric testing

Test Vehicle: Design Details

MLO and Probe PCBs are designed using Allegro & APD for design layout and simulated using CST Microwave Studios

MLO Design

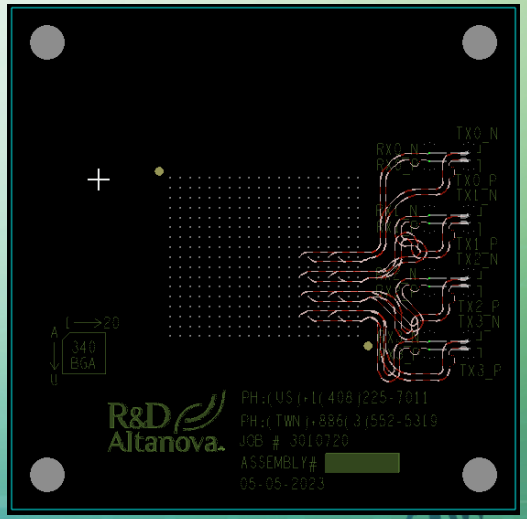
- 3+4+3 construction using the Highspeed GL102 material. 0.57mm thick
- 250um to 1000um pitch translation
- Capacitor embedded in the center core of the MLO
- HDI build – stub-free design!
- Two MLO options
  - Loopbacks with broadband capacitors
  - Loopbacks with standard capacitors

Lyr	Copper Weight (Oz)	Generic Name	Family	Image	Foil
SMT					
L1, TOP	0.07	20um_Outer-Lay...	Substrate Foil		0.07oz
		30 UM	GL102		
L2, RDL1	0.07	15um_Inner-Lay...	Substrate Foil		0.07oz
		30 UM	GL102		
L3, GND1	0.07	15um_Inner-Lay...	Substrate Foil		0.07oz
		40 UM	GL102		
L4, GND2	0.5	0.50 oz - Foil	Foil		0.5oz
		1035 (75%)	MetWave2000		
L5, BLANK1	0.5	0.007 SHxSH	MetWave2000		0.5oz
L6, BLANK2	0.5				0.5oz
		1035 (75%)	MetWave2000		
L7, INR1	0.5	0.50 oz - Foil	Foil		0.5oz
		40 UM	GL102		
L8, GND3	0.07	15um_Inner-Lay...	Substrate Foil		0.07oz
		30 UM	GL102		
L9, RDL2	0.07	15um_Inner-Lay...	Substrate Foil		0.07oz
		30 UM	GL102		
L10, BOTTOM	0.07	20um_Outer-Lay...	Substrate Foil		0.07oz
SMB					

Probe PCB Design

- 12-Layer, 3mm thick board
- Broadband capacitor on the underside of the board
- Through hole board design with back-drilled vias
- High-performance meteor wave 4000 material
- Optimized PCB DUT launches and loopback structures for minimal loss possible

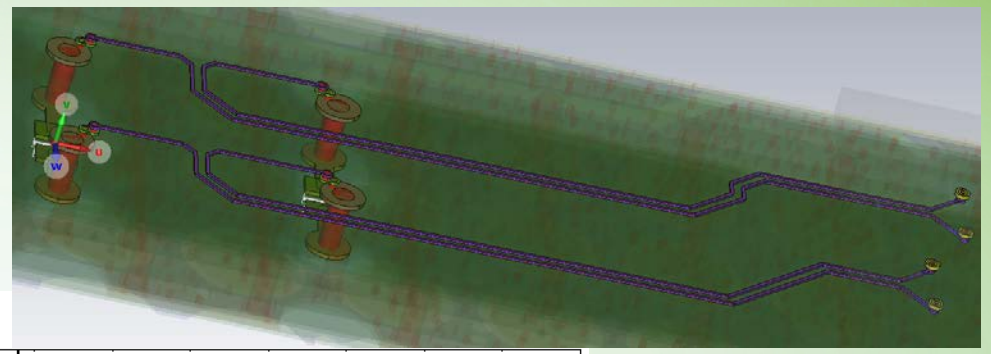
Lyr	Copper Weight (Oz)	Generic Name	Family	Image	Foil	Thk
SMT						1
L1, TOP	0.25	0.25 oz - FoilT	Foil		0.25oz	2.86
		1035 (79%)	MetWave4000			
		1035 (79%)	MetWave4000			5.96
L2, GND1	0.5	0.005 SHxSH	MetWave4000		0.5oz	5.3
L3, INR1	0.5				0.5oz	
		1035 (79%)	MetWave4000			
		1035 (79%)	MetWave4000			5.72
L4, GND2	0.5	0.005 SHxSH	MetWave4000		0.5oz	5.3
L5, GND3	0.5				0.5oz	
		1035 (79%)	MetWave4000			
		1035 (79%)	MetWave4000			5.96
		0.015 SHxSH	MetWave4000			15.3
		1035 (79%)	MetWave4000			
		1035 (79%)	MetWave4000			5.96
L6, GND4	0.5	0.005 SHxSH	MetWave4000		0.5oz	5.3
L7, GND5	0.5				0.5oz	
		1035 (79%)	MetWave4000			
		1035 (79%)	MetWave4000			5.96
		0.015 SHxSH	MetWave4000			15.3
		1035 (79%)	MetWave4000			
		1035 (79%)	MetWave4000			5.96
L8, GND6	0.5	0.005 SHxSH	MetWave4000		0.5oz	5.3
L9, GND7	0.5				0.5oz	
		1035 (79%)	MetWave4000			
		1035 (79%)	MetWave4000			5.72
L10, INR2	0.5	0.005 SHxSH	MetWave4000		0.5oz	5.3
L11, GND8	0.5				0.5oz	
		1035 (79%)	MetWave4000			
		1035 (79%)	MetWave4000			5.96
L12, BOTTOM	0.25	0.25 oz - FoilT	Foil		0.25oz	2.86
SMB						1

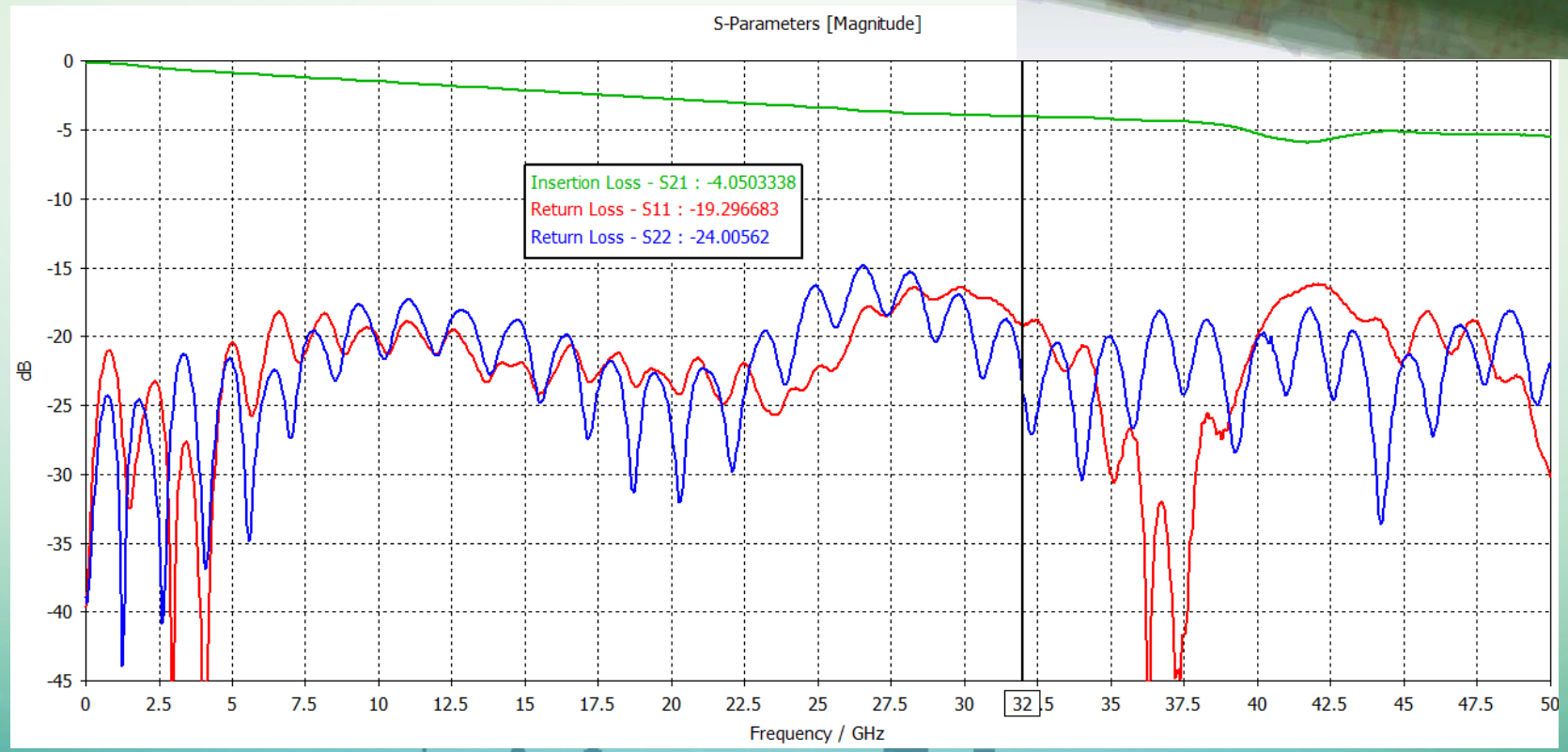


Full 3DFS Modeling (MLO Loopback)

Modeled with broadband capacitors:

- Broadband Capacitor P/N: 1005BB104MW4R0 / Passive Plus

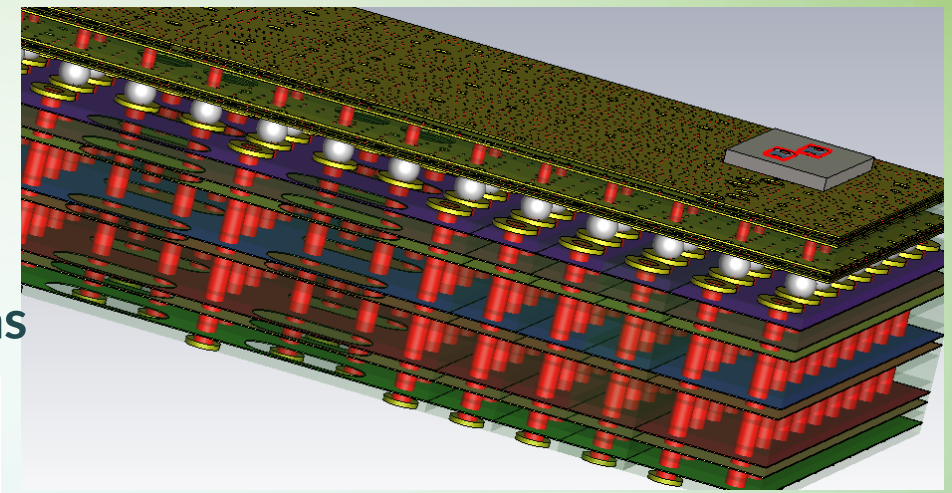


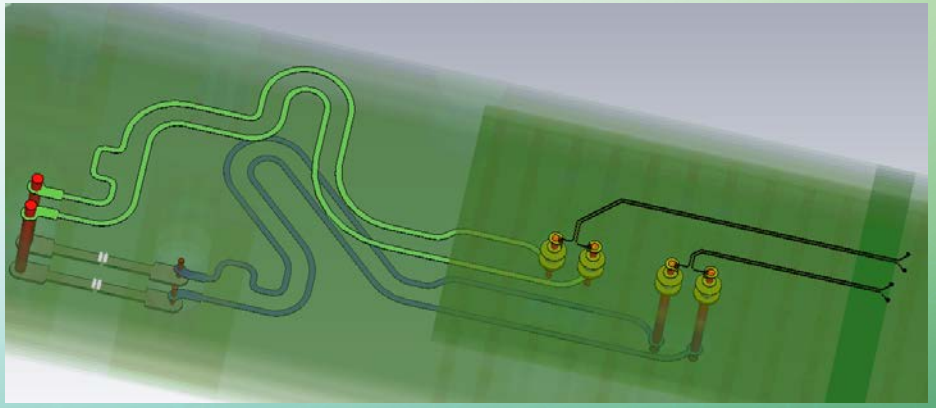


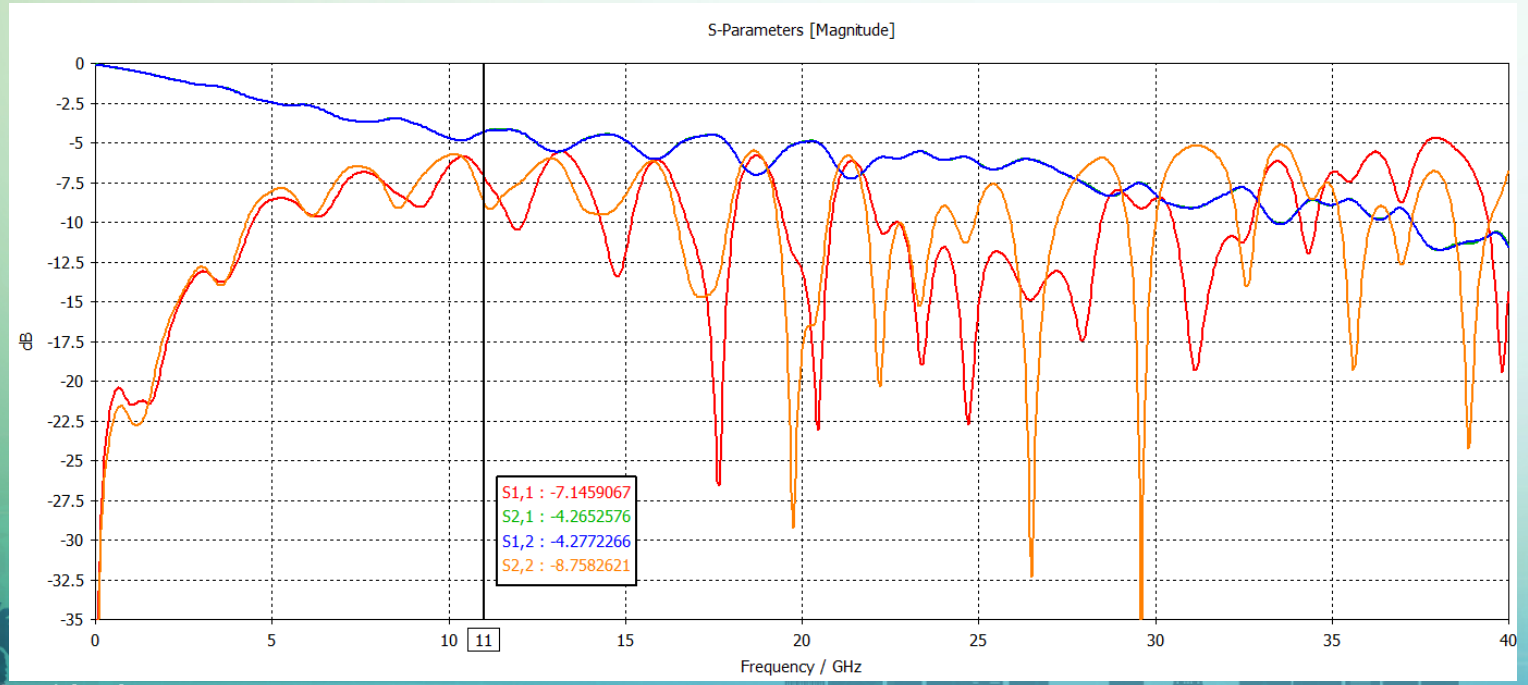
Full 3DFS Modeling (MLO & Probe PCB path)

Layout design for best case, thin PCB and optimized PCB stacking to show best case results

- Simulations included Solder ball attach between MLO and Probe PCB
- Broadband capacitor on the bottom side of the PCB
- Simulated with a 10 mil back-drill stub on through hole vias



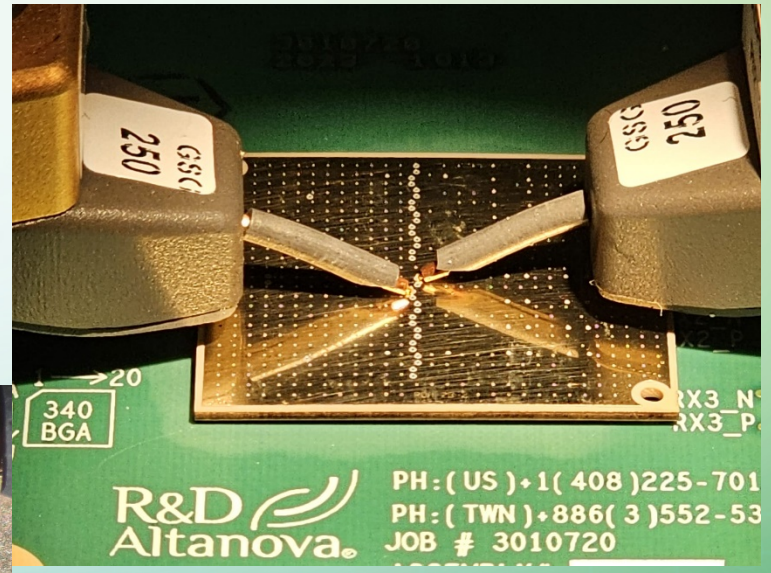


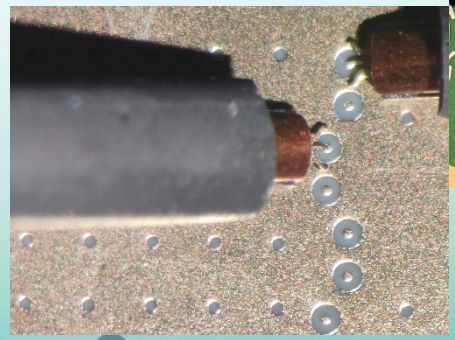


Measurement Test Setup

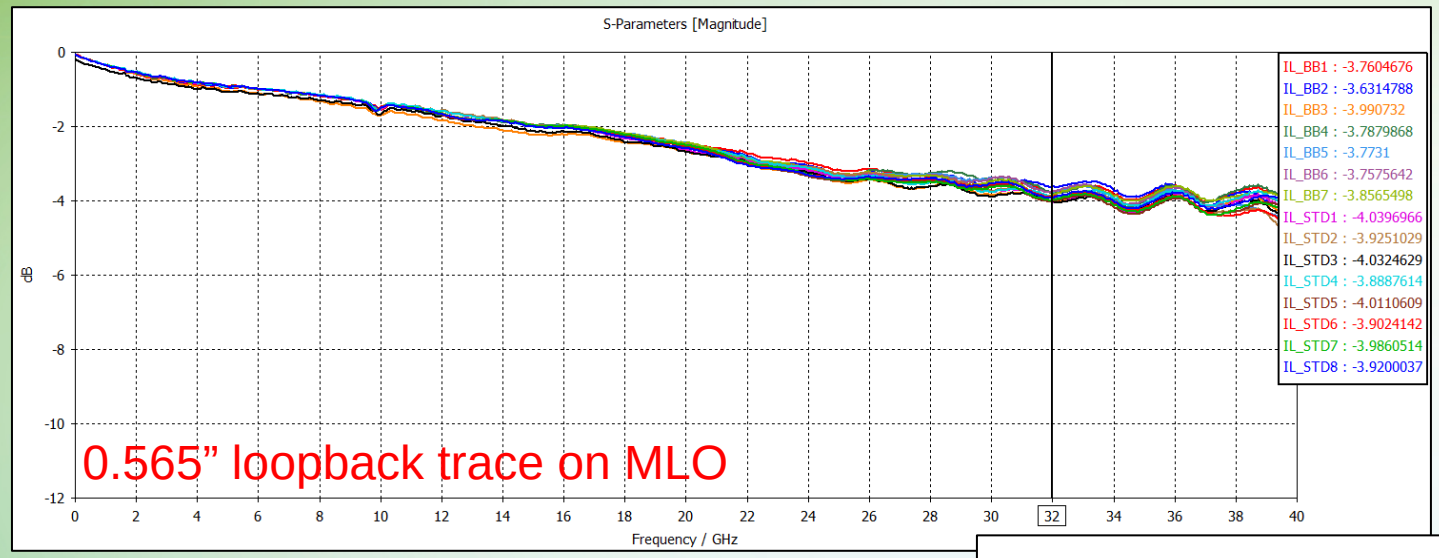
Test Setup Includes:

- A 4-Port 70GHz Anritsu VNA/PNA
- 65 GHz 250um GSGSG & 250 GSG probes for C4 side loopback measurements
- Bench probe station with micro positioners
- Probes were not de-embedded in measurements
- Measured loopbacks on C4 side of the MLO
- MLO C4 side designed as GSGSG – 250um pitch
- Measured full path on MLO only
- Measured full path from MLO to probe PCB and back





MLO Loopback Measured Performance



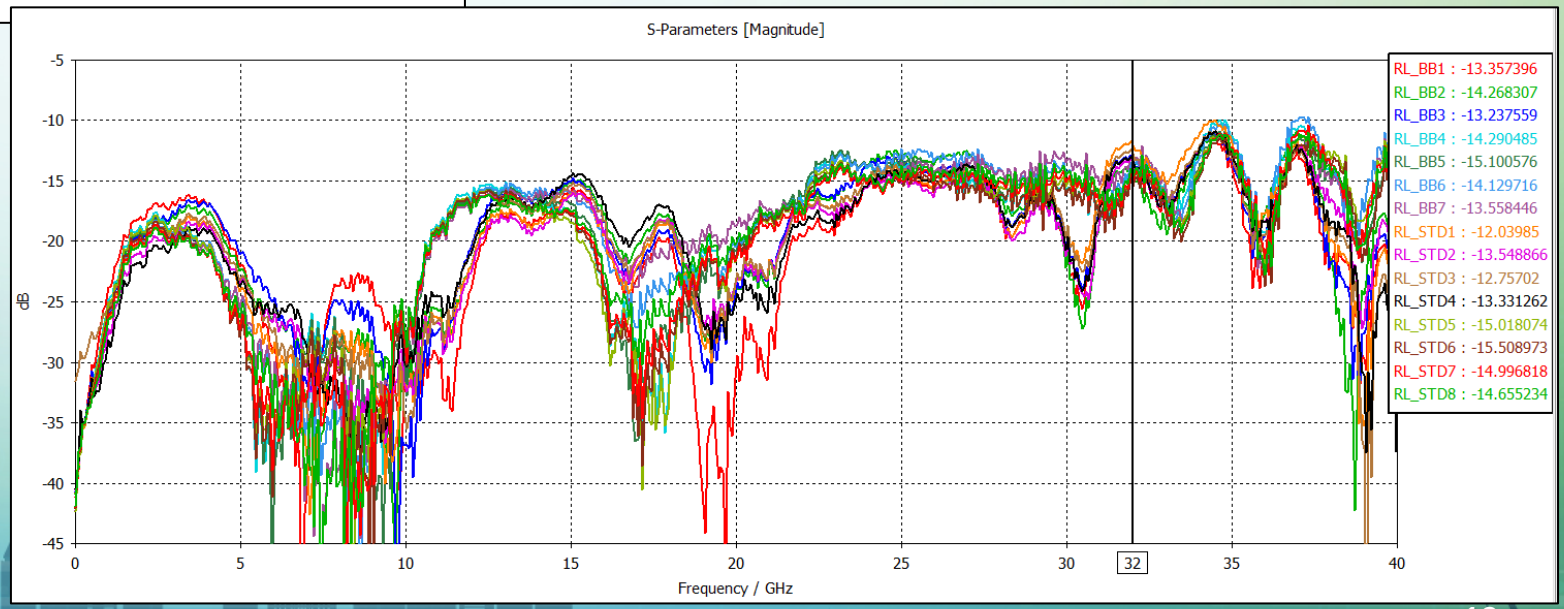
Great performance up to 40 GHz

Two capacitor options used for manufacturing:

Broadband Capacitor P/N: 1005BB104MW4R0 / PPI

Standard Capacitor P/N: C0402X5R0G104M020BC TDK

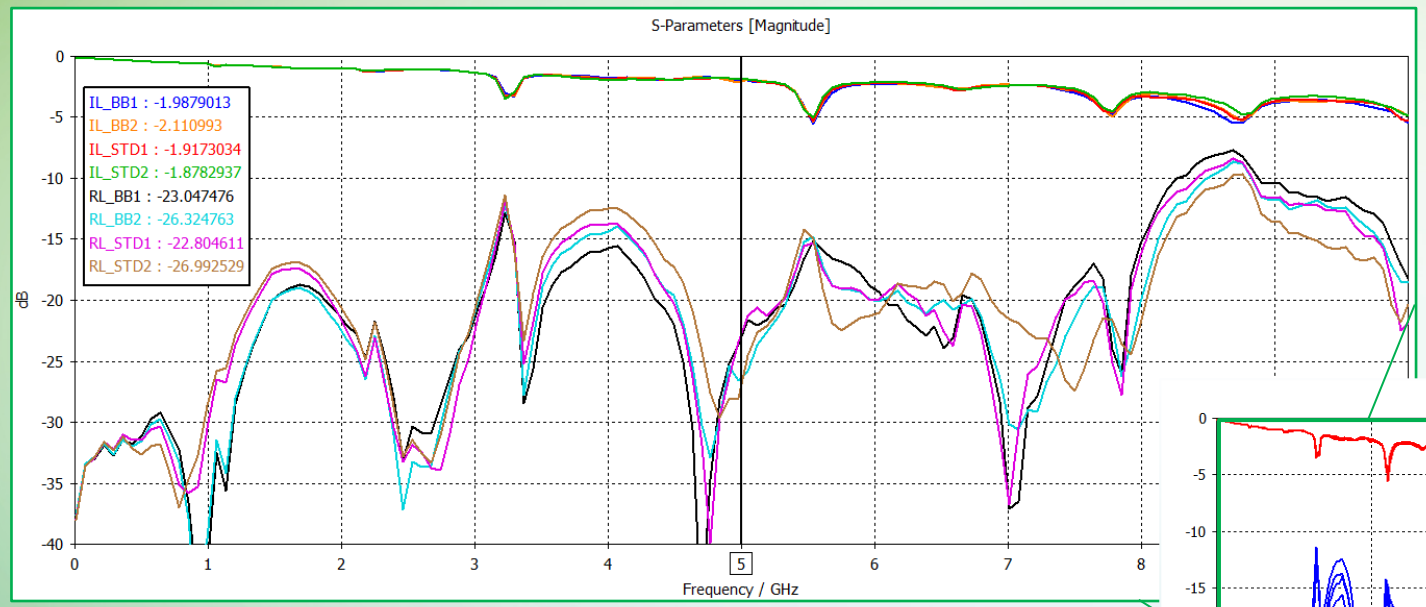
Enables 200G+ PAM4 and PCIE Gen5/6 on Probe



*** Probes not de-embedded**

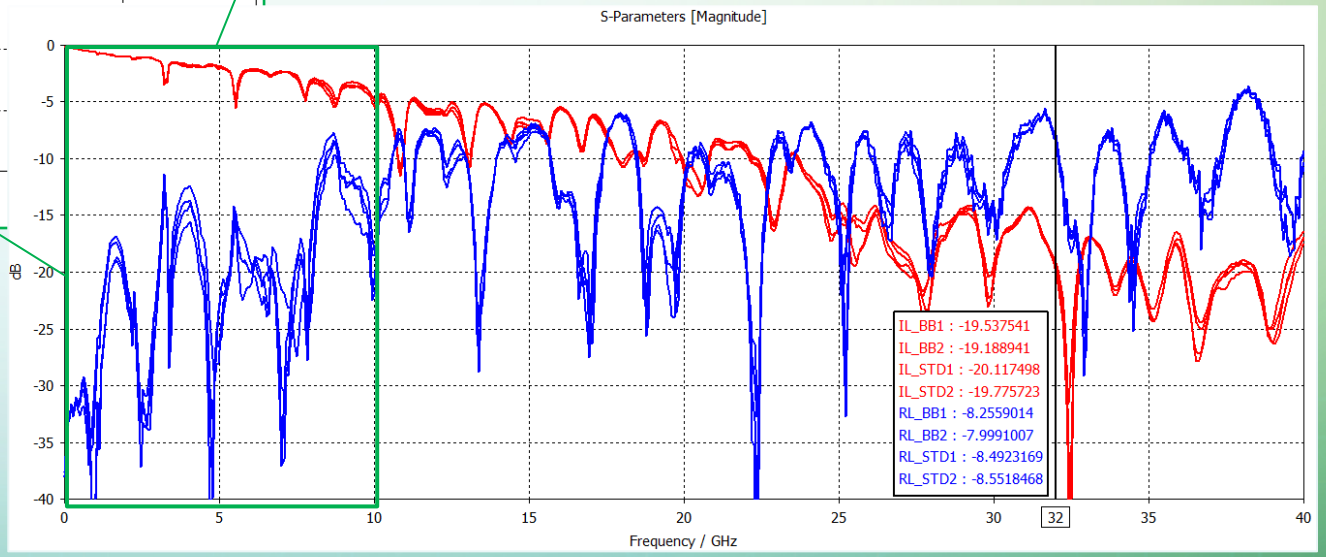
MLO & Probe PCB Measured Loopback Path

Mostly resonance-free performance up to 5GHz – Limited frequency response



1.84” loopback Total MLO + Probe loopback Trace

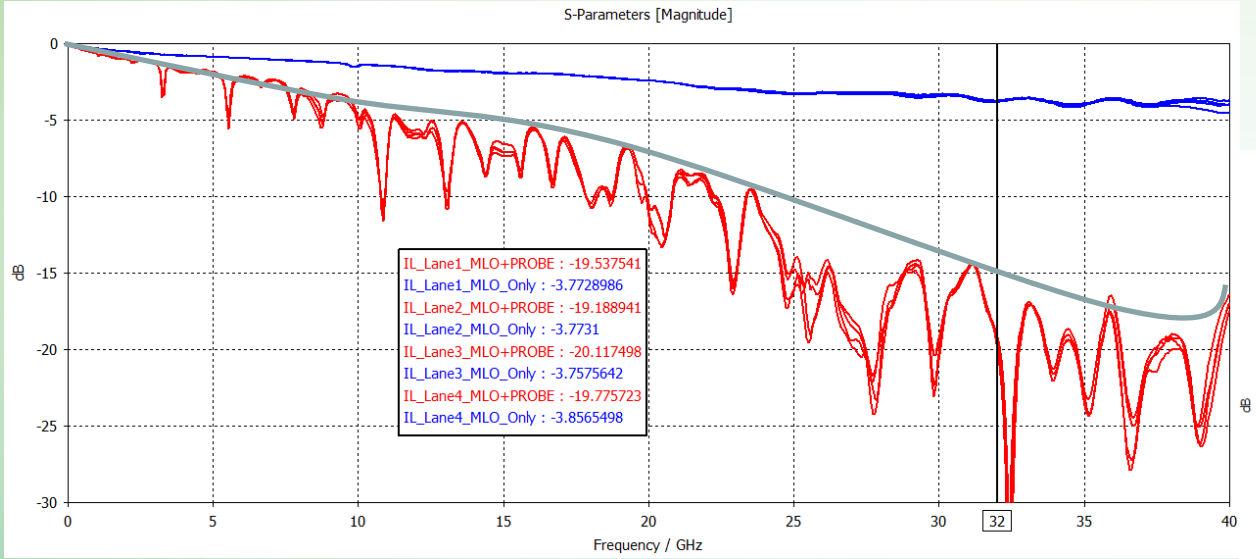
Performance measured showed higher return loss due to the discontinuity measured due to MLO and PCB attach using copper spheres

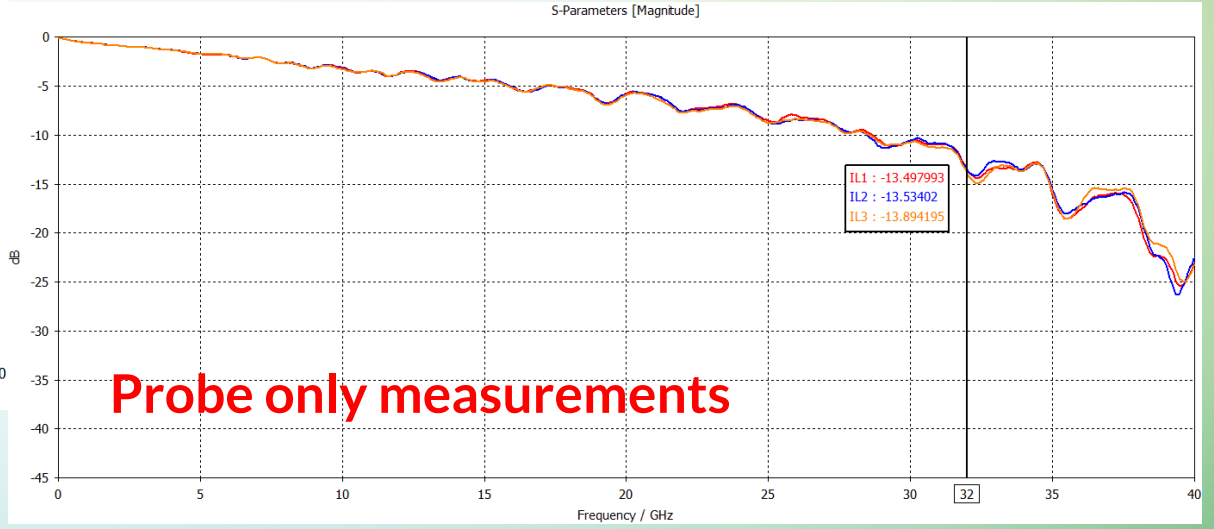


*** Probes not de-embedded**

Performance Comparison

MLO loopback has a distinct advantage for HS signal routing with embedded loopbacks!!

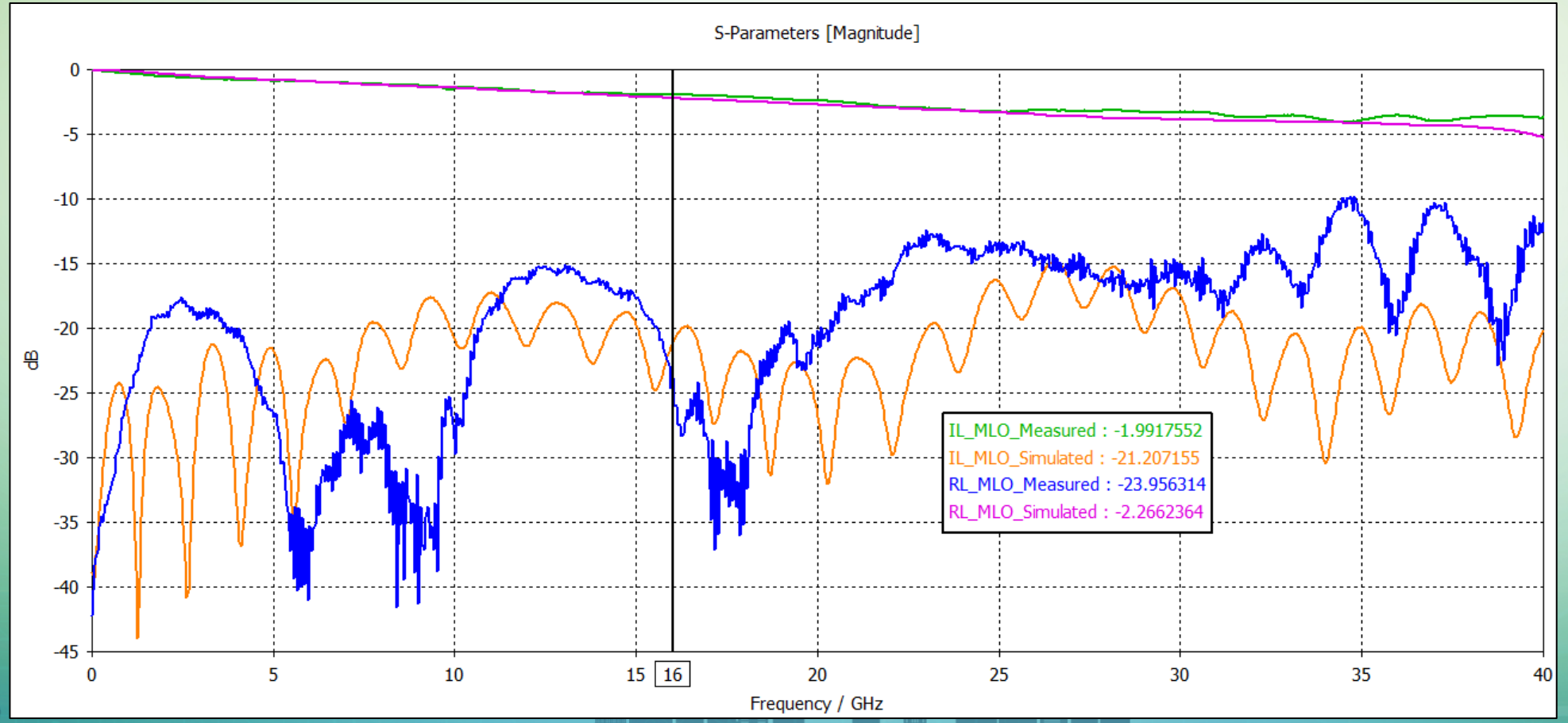




- **Resonance observed due to:**
  - Impedance discontinuity due to MLO to Probe PCB attach
  - Slightly longer back-drills than simulated values on the probe PCB fixture

Simulation and Measurement Correlation

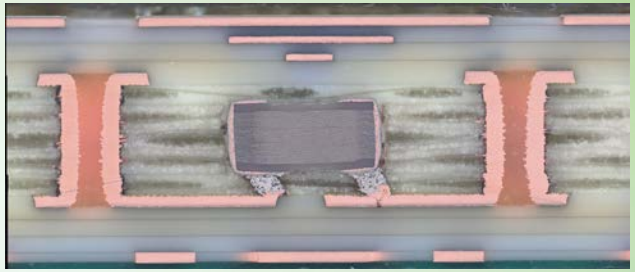
Good correlation of simulated to measured performance for embedded loopbacks

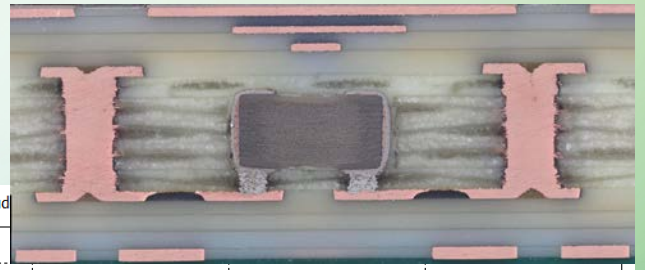


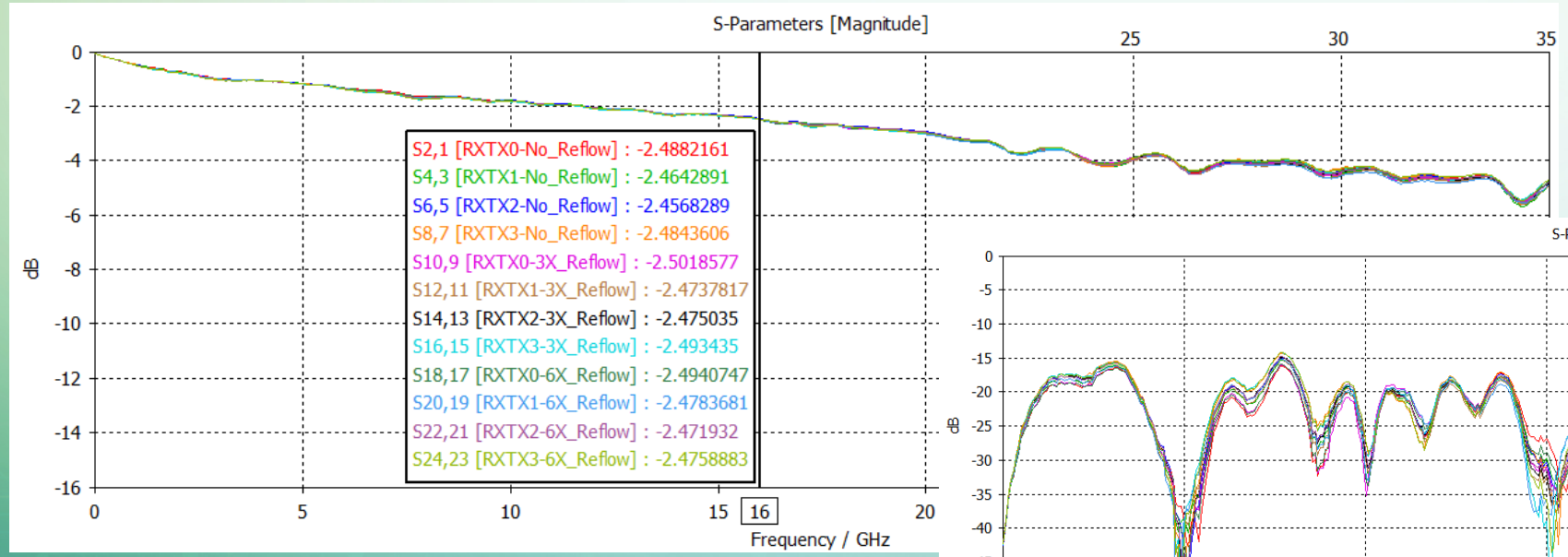
Measured higher frequency return loss is higher as 250GSGSG probes are not de-embedded

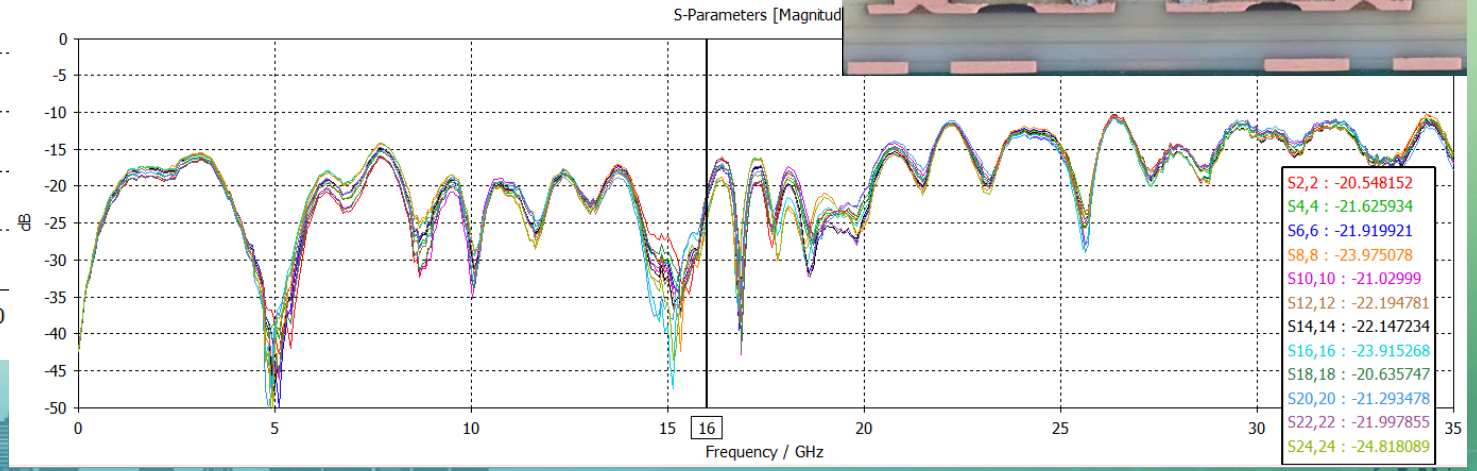
Manufacturing Yield & Thermal Reliability Tests

- High yields: > 80% manufacturing yield for embedded components on MLOs
- Thermal reliability tests conduction as per IPC-600-TM method:
  - 3x & 6x reflow cycles
- Identical measured performance after 3x and 6x reflow cycles









Conclusion

- Embedded component MLO is a useful technology to enable digital and RF performance for probe
- Process shows a good correlation between simulated and measured performance on the loopback paths with ECMLO
- High manufacturing yields mean affordable technology and less turnaround time because of fewer fab re-spins
- Thermal reliability studies show similar performance and no failures after 6 reflow cycles
- Significant performance benefits over the traditional probe card routing approach
  - Enables 200G+ PAM4, PCIE Gen5/6 and other high-speed SerDes IPs on probe

Thank You

Questions?