SWTEST

PROBE TODAY, FOR TOMORROW

2023 CONFERENCE

STAYING AHEAD OF THE PROBE CARD COMPLEXITY CURVE

TERADYNE

Eric Shoemaker

Steve Ledford

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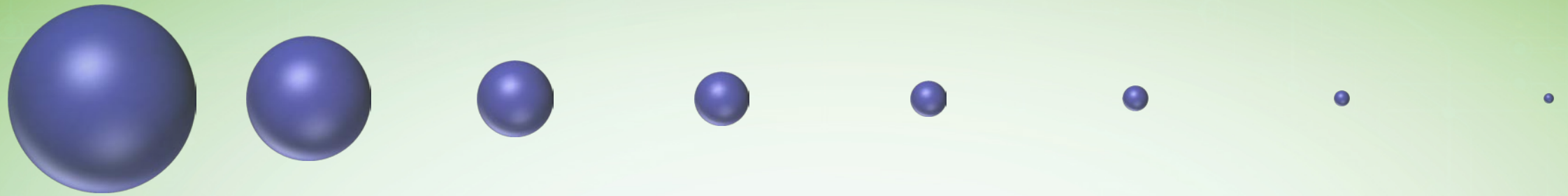
Reminder: We are in the Era of Complexity



1990	1995	2000	2005	2010	2015	2020	2025
0.8um	0.35um	130nm	65nm	28nm	14nm	5nm	2-3nm






Era of Functionality

- Rapid Data Rates increases
- Mixed signal CMOS
- High rate of technological obsolescence for ATE

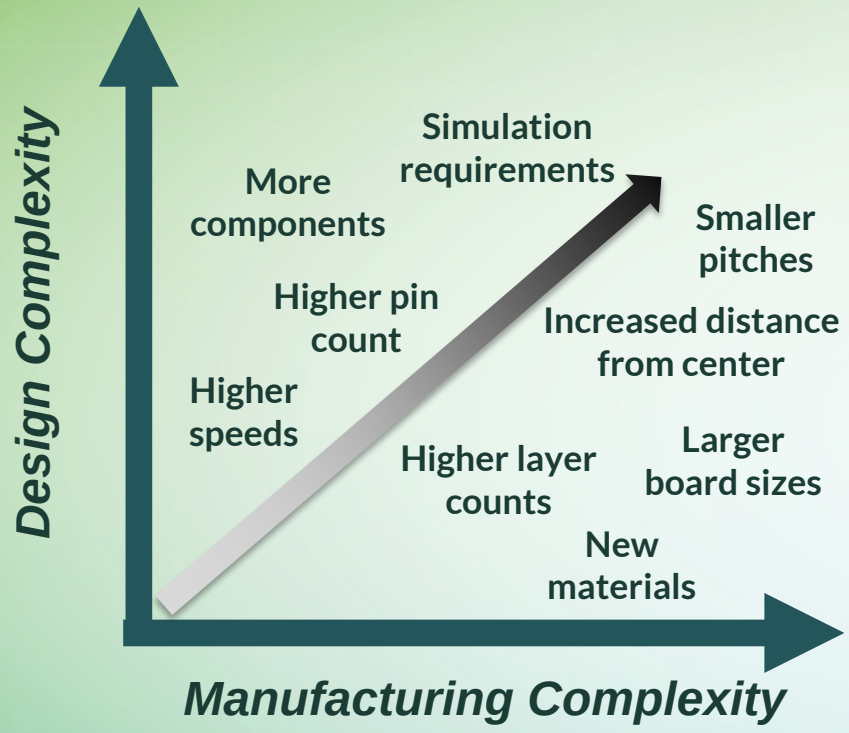
Era of Capital Efficiency

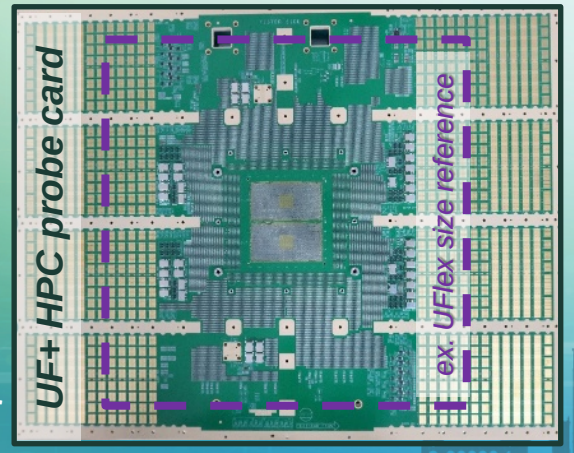
- Standards based interfaces (DDR, PCI, USB)
- Innovation in DFT (Scan Comp, BIST, Loopback)
- Rapid increase in parallel test

Era of Complexity

- Transistor counts grow faster than DFT
- Site count increase blocked by interface complexity
- Short market windows for complex devices

What is Interface Complexity?





Product of *Design* & *Manufacturing* Complexities:

- Design: Attributes to achieve the test requirements
  - Most are fixed and non-negotiable
    - DUT pads and pitch
    - Parallelism target
    - Test speed and accuracy requirements
  - Some solutions drive integrated design types:
    - PCB & substrate
    - Mechanical & cable designs
    - Product-family flexibility

- Manufacturing: Attributes to build the probe card
  - PCB & Substrate (pitch, size, layer count)
  - Components & assembly (quantity, size, type)
  - Managing yields, process capability, & allowed cycle time

Interface Hardware Complexity Forecast:

Following the "2 x 4 Scaling" trend demonstrated over last two decades

		Today	2030
Pin Density	Increasing DUT sites and pin count drive up the pin area density	70 um pad pitch	30 um pad pitch
	Challenge: Routing the I/O and power to the DUT combined with an increasing mechanical load	16,000 pins per cm^2	64,000+ pins per cm^2
		150+ Kg (total contact)	300+ Kg (total contact)
I/O	Connections to high performance I/O: high speed digital, wireless, and high voltage	112 Gbps (dig)	400+ Gbps (dig)
	Challenge: Signal integrity when combined with very tight pin and DUT spacing and high DUT count	54 GHz (5G)	110+ GHz (6G)
		2 kV (automotive)	8 kV (automotive)
Power	Large number of high current (>25A) device supplies require excellent precision	700 mV (main power)	<500 mV (main power)
	Challenge: Supply voltage reduction (<700mV) combined with increasing number of power rails	750 A (single rail)	2000 A (single rail)
		500 µOhm (impedance)	100 µOhm (impedance)
Thermal	Removal of the DUT thermal energy due to self heating and support increased operating temp ranges	0.5 KW (self heating)	1.0 KW (self heating)
	Challenge: Increasing transistor count combined with tight DUT spacing rapidly increases thermal density	0C to +125C	-40C to +160C

Does your probe card supply chain have an R&D roadmap aimed at achieving these requirements?

What Probe Card Customers Want

- **High Performance**
  - Best test coverage and repeatability
  - Fastest test speed for maximum throughput
- **High Quality**
  - 1st pass acceptance rate for fastest bring-up
  - Good site-to-site matching for limit-setting
  - Longer MTBF and faster MTTR

"Good"

- **On-Time Delivery & Shorter Lead Times**
  - Hardware arrives when scheduled
  - Fast response to upside demand for new HW

"Fast"

- **Low Cost**
  - Make my purchasing decision easy!

"Cheap"

"We need it Good, Fast, and Cheap"

Role Playing: Who wants free probe cards?

- If you were given the opportunity to get free probe cards for your next-generation device, would you take it?
  - "Of course! Why not?"

- What if they were delivered 4-6 weeks late with a 1st pass rate of 60% for NPI bring-up?
  - Do you think your CEO would agree it was the right choice to save money on the probe cards when your next-gen device's release to market slips?
  - These OTD and Quality metrics are realistic for high-complexity probe cards today from suppliers who are behind the complexity curve
    - And it will only get worse for them in the future if they don't invest to catch up

“Cheap” Depends on What is Measured

- Hidden costs can add up to many times the purchase price of a probe card over its operating life → Total Cost of Ownership (TCO)
  - Example from SWTest ‘22 Paper, “Probe Card Total Cost of Ownership”:
    - Operational Efficiency & Quality
      - $78K savings
    - Time to Market
      - $139K savings
    - Entitled Yield
      - $119K savings

- Purchase Price ($275K)
  - +$25K more expensive for a high-performance, high-quality probe card vs. “cheap” option

  - “Reduced TCO” is what customers truly mean when they say “cheap”

Stay Ahead of the Complexity Curve

- TCO advantages come from improving performance, quality, and OTD while maintaining lead times
  - You can keep your customers happy and improve your profitability at the same time!
    - Focus on improvements in three fundamental areas:

- Falling behind the complexity curve will result in:
  - Manufacturing yield challenges — Risk: profitability, quality, timing
  - Innovating in the critical path of customer projects — Risk: quality, timing
  - Underestimating engineering utilization — Risk: profitability, timing

Design Process Improvements

Larger boards @ smaller pitch
> 110 combined layers
> 600K vias

> 30K components
Assembly dpmo of ~1000
Many active switches/relays

> 3000hrs Design Eng. utilization
Same 5-week cycle time needed
Higher simulation requirements

Design for Manufacturability

- Design rules based on pre-defined manufacturing process & material selection
- Consistent manufacturing partnerships will drive continuous improvement
  - Evolving DFM rules, co-validation of new materials, more accurate simulation and yield-prediction models

Design for Testability

- Without a validation plan in mind, defect detection and 1st pass rate will suffer
  - Duration of QC and debug/repair will cause lead times to worsen
- Diagnostic-specific circuits and FPT points needed for active failure mode triggering and detection

Layout and Simulation Automation

- Improve site-to-site performance matching at higher frequencies and power levels through rigorous simulation
- Develop tools for automation of repetitive and iterative tasks in order to increase engineering efficiency & capacity
  - Reduce loading by 50% or suffer from profitability and capacity erosion

Manufacturing Process Improvements

OTD is achieved only with accurate yield estimations and process monitoring

Yield-prediction model uses determined inputs and characterized effects

Inputs & Effects come from results of test vehicles & new process characterization

Capability Test Vehicle (CTV) definition comes from R&D roadmap goals

R&D roadmap planning comes from understanding customer & market trends

- In order to stay ahead of the complexity curve, suppliers must continuously invest in better manufacturing tools & processes:
  - Larger PCB and substrate sizes
  - Higher layer counts
  - Smaller pitch fabrication
  - Smaller attach pitch and density
  - Thermal & Mechanical compensation

Ask your probe card vendor for their qualification & characterization results – Don't be a guinea pig!

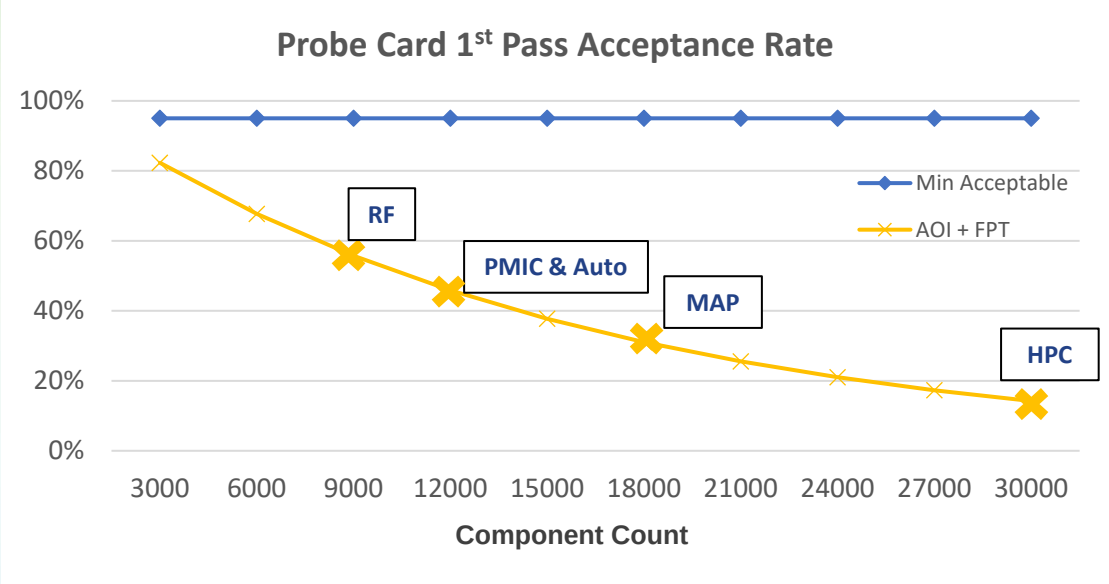
- How will you construct a new HPC probe card (200Gbps, 1000A)?
  - >100 total layers (70+ needed just for power/gnd planes)
    - Materials must all be characterized for accurate simulations
    - High-speed signals cannot be routed on subtractive process (PCB) due to etch control & line width variability
  - Need stub-less design (backdrill insufficient) for impedance matching
    - Microvias in substrates allow better escape routing at high density
  - If you haven't characterized these processes, will it ever yield?

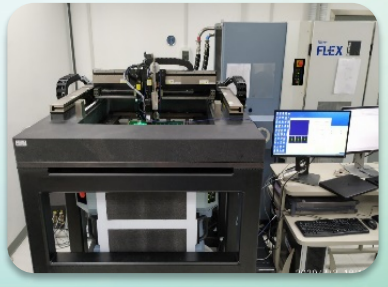
QC & Service Improvements

- NPI bring-up time is critical to achieve TTM goals
  - Three major items to debug simultaneously:
    - Probe Card, Test program, First silicon wafers
  - HW defects can cause weeks of bring-up delay

- Defect detection must keep pace with increasing component counts and failure modes
  - AOI & FPT no longer sufficient
  - Active circuit control needed for full-board validation and fault model coverage
  - Development time for diagnostic tests must not affect overall probe card lead time
  - Bonus: parametric validation will improve MTBF!

- "Self-service" diagnostics allows for on-site debug on demand by the customer test engineers
  - Shortens root cause determination and repair cycle time (MTTR), improving uptime and OEE





- High-frequency RF solutions
  - Need full-path characterization and de-embedding to guarantee performance
  - Automate!

Conclusion – Good & Fast Leads to Better TCO

- Device complexity drives innovation in the probe card market
  - Interface hardware complexity will continue to increase as the newest test platforms extend parallelism, speed, and power during wafer probe
- Investing in improvements to processes and tools is the only way to satisfy your customers and maintain profitability
  - Design, Manufacturing, and QC must all be continuously improved
    - Target to deliver high-complexity probe cards with >95% OTD and 1st pass rates, best-in-class SI/PI performance, and consistent lead times
- By staying ahead of the curve, you can offer your customers Good, Fast, and a better TCO – no longer need to pick only 2!

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Thank you!

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