SWTEST

PROBE TODAY, FOR TOMORROW

2023 CONFERENCE

# Challenges and Innovations in Developing High-Density, Low-Power DPS Solutions for 5nm and Smaller Process Geometries in ATE

ELEVATE SEMICONDUCTOR


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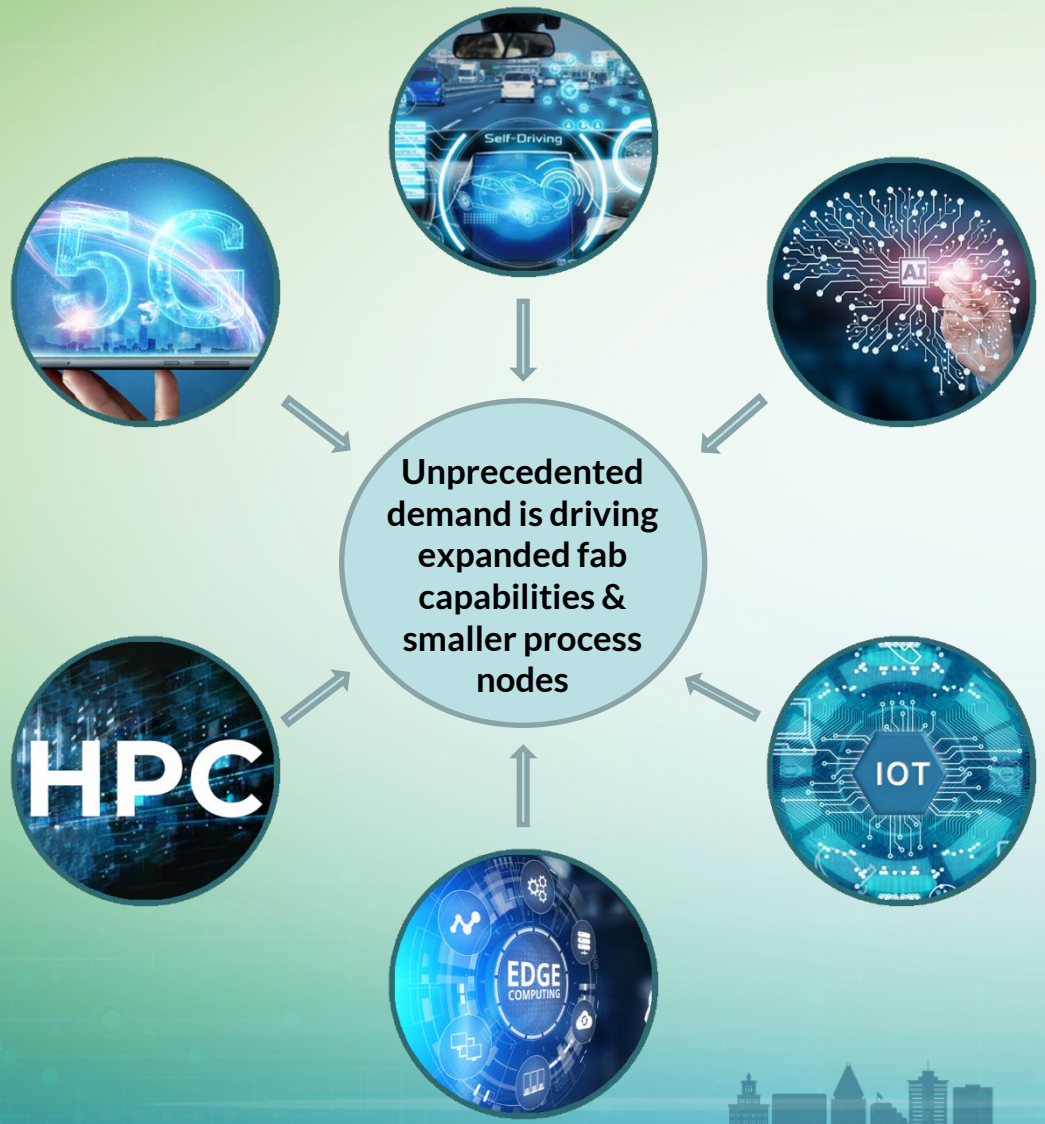
# Overview

- Demand is Driving Smaller Process Nodes
- Challenges of ≤ 5nm Process Nodes on DPS Solutions
  - Fast Load Transient Response
  - High DC Accuracy
  - High Power Efficiency
- Introduction to Elevate Semiconductor
- Future ATE Solutions
- Collaboration

# Demand is Driving Smaller Process Nodes




## $150B+ in Fabs Under Development

| Foundry | Node | Investment | Completion | Location |
|---|---|---|---|---|
| Global Foundries | 14nm | $1B | 2023 | New York |
| Intel | 7nm | $10B | 2023 | Israel |
| | 2nm | $20B | 2024 | Arizona |
| | 2nm | | 2024 | |
| | 2nm | $28B | 2025 | Ohio |
| | | | 2025 | |
| Samsung | 3nm | $17B | 2024 | Texas |
| | 3nm | ? | 2022 | Korea |
| | 3nm | ? | 2020 | |
| | 2nm | ? | 2025 | |
| TSMC | 7nm | $10B | 2024 | Taiwan |
| | 5nm | $12B | 2024 | Arizona |
| | 3nm | $20B | 2023 | Taiwan |
| | 2nm | ? | 2025 | |
| | 1.4nm | ? | 2027 | |
| Texas Instruments | 45-130nm | $30B | 2025 | Texas |

- **Intel: $100B in Europe; $80B in Ohio**
- **Micron: $100B in New York**

***Source: The Information Network and Tom's Hardware***

# Challenges of ≤ 5nm Process Nodes

Along with smaller geometries come:

- Reduced operating voltage (< 1V)
- Larger current consumption (100s or 1,000s of amps)
- Higher speeds (multiple Gbps)
- Higher pin counts (1,000s of pins)

How does this affect probe card design?

- Higher pin counts require tighter pitch and smaller pad sizes
- High-density interconnects require similarly high-density associated electronics
- Large currents cause excess heat, probe damage

Requirements for Device Power Supplies

- Fast Load Transient Response (enables fast scans)
- High DC Accuracy (increases yield, quality)
- Improved Power Efficiency (allows greater density)


**Apple A17, TSMC 3nm**
(Iphone 15 Pro/Ultra)

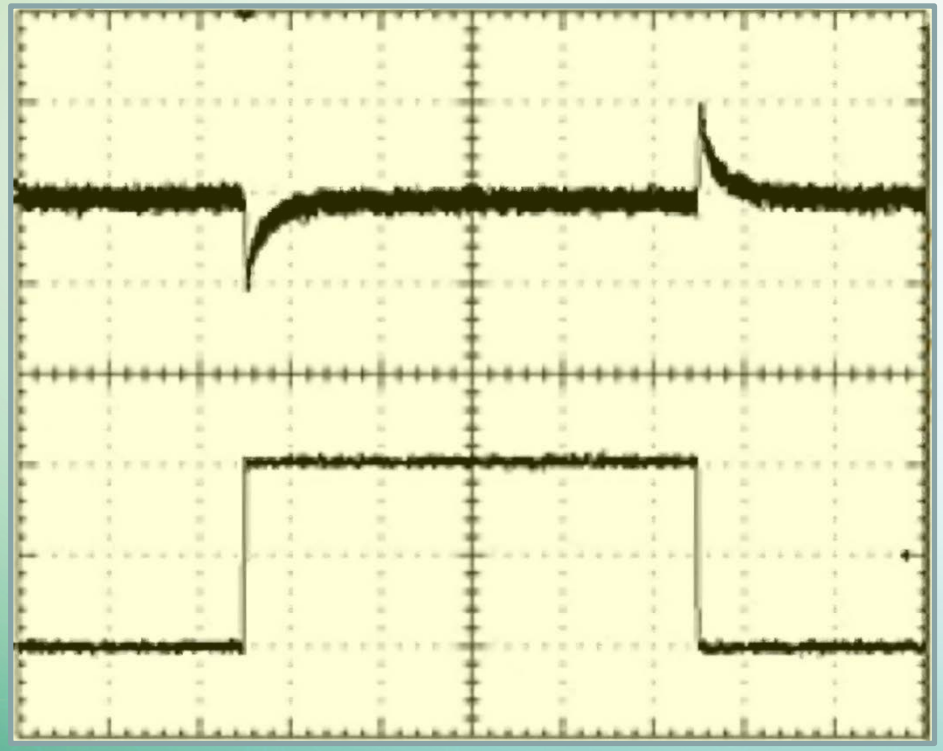

**Nvidia H100 GPU/AI, TSMC 4nm**

# Challenges of ≤ 5nm Process Nodes

**DPS: Fast Load Transient Response**

Vout

Iout

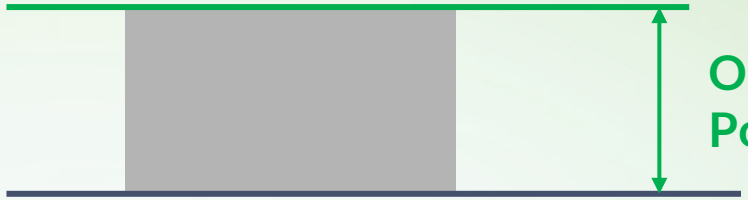


- As scan patterns begin, large current causes Vdroop
- If too large, can reset DUT and cause a false failure
- Running scans at a slower speed or staggering starts can mitigate droop, but this will increase test time and COT

# Challenges of ≤ 5nm Process Nodes

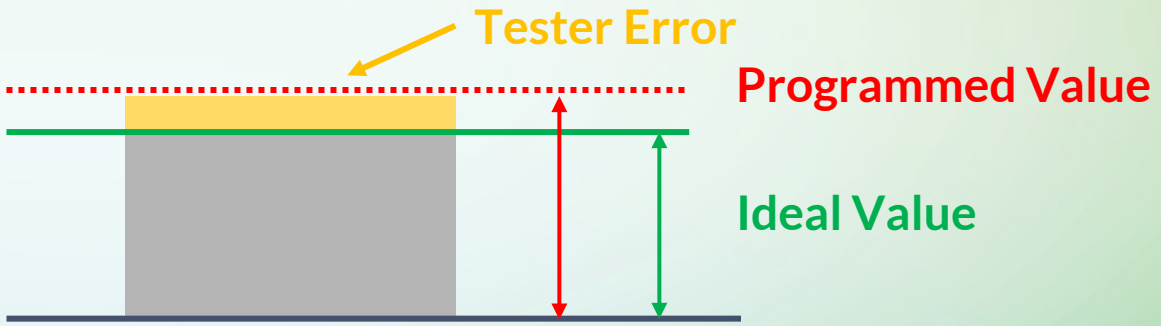
**DPS: High DC Accuracy (millivolts or less)**

**Ideal tester has perfect accuracy**



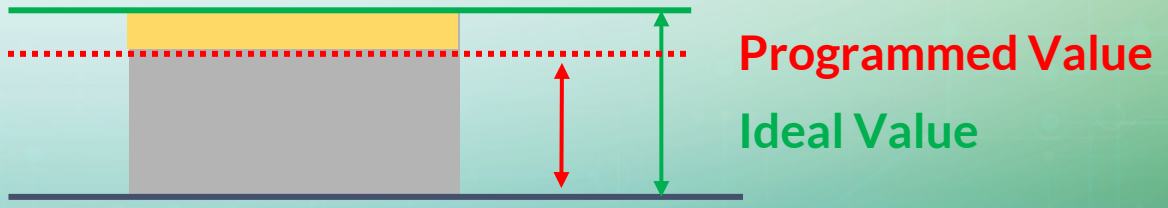

**Programmed to higher value to ensure yield**

- **Wastes power**
- **DUT runs hotter**
- **Might need to run slower scans**




**Programmed to lower value to ensure quality**

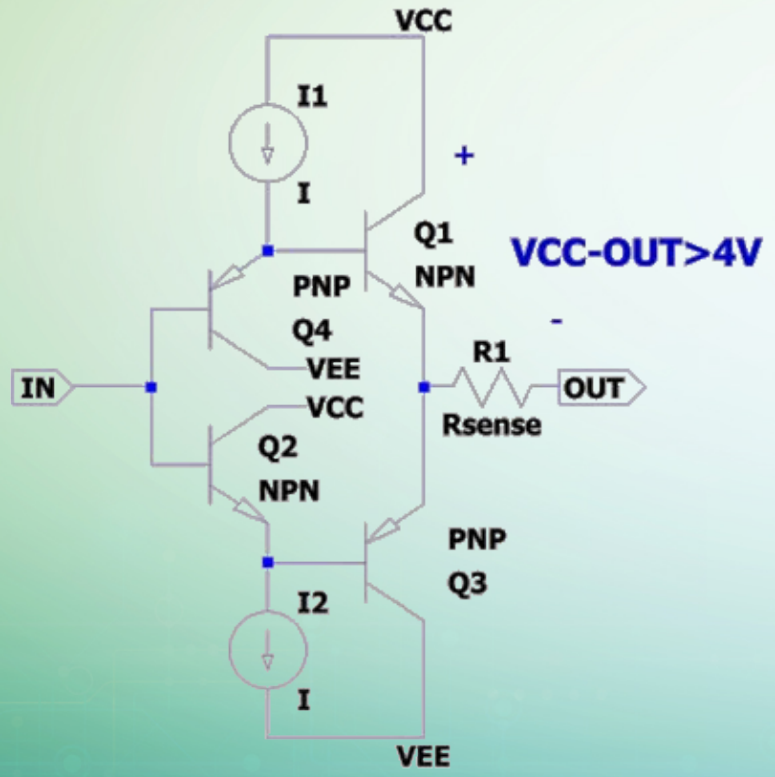
- **May reduce yield**



# Challenges of ≤ 5nm Process Nodes

## DPS: High Power Efficiency

### Common Linear Solution

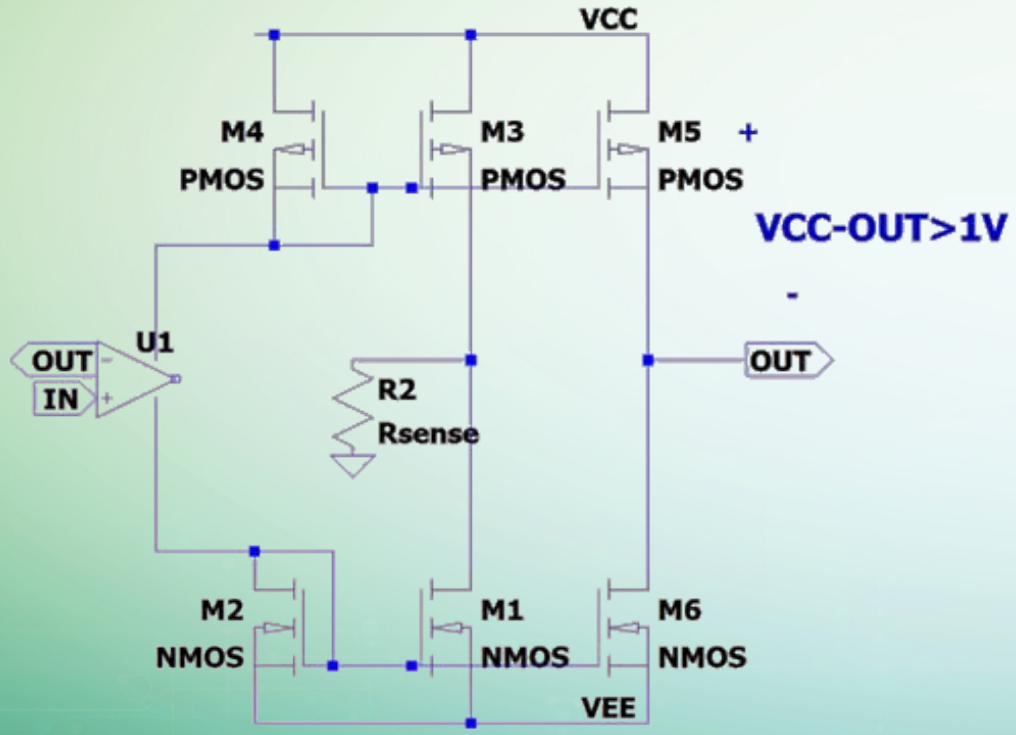



- This architecture requires large headroom: for $Vout = 1V$, $Vcc$ must be $\geq 5V$
- Poor Efficiency = $\frac{Pout}{Pin} = \frac{I * Vout}{I * Vin} = \frac{1V}{5V} = 20\%$
- For every 1W delivered to the load, 4W are wasted

# Challenges of ≤ 5nm Process Nodes

## DPS: High Power Efficiency

### Elevate's Linear Solution

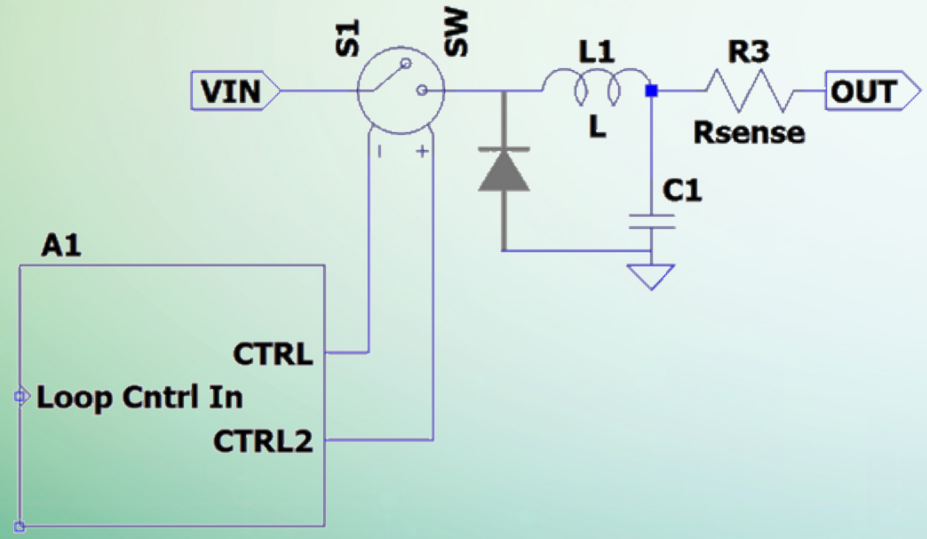



- **This architecture allows smaller headroom**:
  **for** $Vout = 1V$, $Vcc$ **must be** $\geq 2V$
- **Improved Efficiency =** $\frac{Pout}{Pin} = \frac{I * Vout}{I * Vin} = \frac{1V}{2V} = 50\%$
- **For** every 1W delivered to the load, only 1W is wasted

# Challenges of ≤ 5nm Process Nodes

## DPS: High Power Efficiency

### Elevate's Next-Gen Switch-Mode DPS

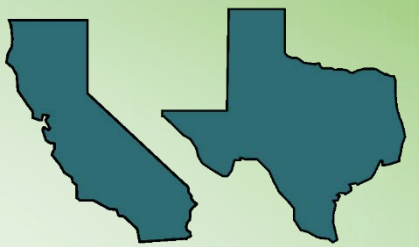



- Linear supplies are only power efficient when *Vcc* is optimized for *Vout*
- Switch-mode power supplies are efficient across a wide voltage range
- Power Efficiency = $\frac{Pout}{Pin} = \frac{Pout}{Pout + PD}$ = 75-90%

  where $P_D = P_L + P_{Conduction} + P_{Switching}$
- For every 1W delivered to the load, only 250mW is wasted (80% efficient)

# Elevate Semiconductor History and Product Focus

**The only major IC supplier whose sole focus is test**

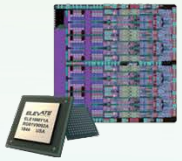


**Wafer Probe & Package Test**

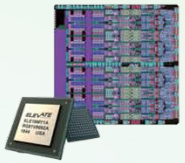
**Instrumentation**

## PE

Venus Family



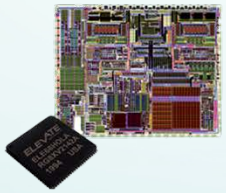
Custom PE & TG



Mystery

- First fully-integrated PE with DCL, DACs, PMUs & Deskews
- Product line has evolved to improve speed, density & power efficiency

## DPS



Jupiter

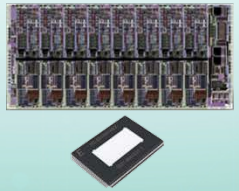
Vesuvius


Custom

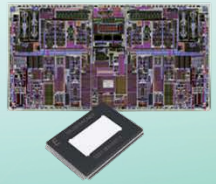
- First fully-integrated DPS with internal DACs
- Latest products have higher channel count, higher power efficiency & smaller footprint

## VI

Pluto



Triton



Saturn (hybrid)

- First fully-integrated octal VI with internal comparators & DACs
- Latest products have increased output voltages

# Elevate's New Solutions: DPS/PMU

**Kilauea**

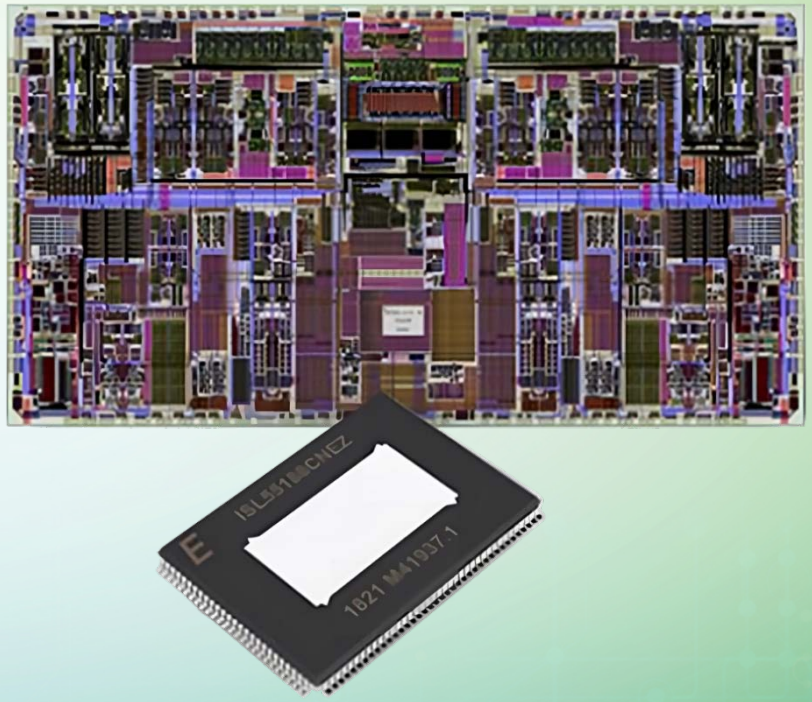
- Improved architecture, high efficiency quad DPS (34V/5A)
- 4 auto-selectable supplies to minimize headroom
- 100uV accuracy (target)
- Internal ganging up to 20A

**Shuksan**

- Switch-mode architecture DPS for max efficiency (75%)
- Chiplet add-on to provide envelope tracking for Kilauea
- High-density quad, 34V

**Whitney**

- Highest voltage dual fully-integrated DPS/PMU (+/- 64V)
- Integrated DACs, MI, monitors
- Applications in Automotive, PoE, PMIC Quick Charge, LED drivers



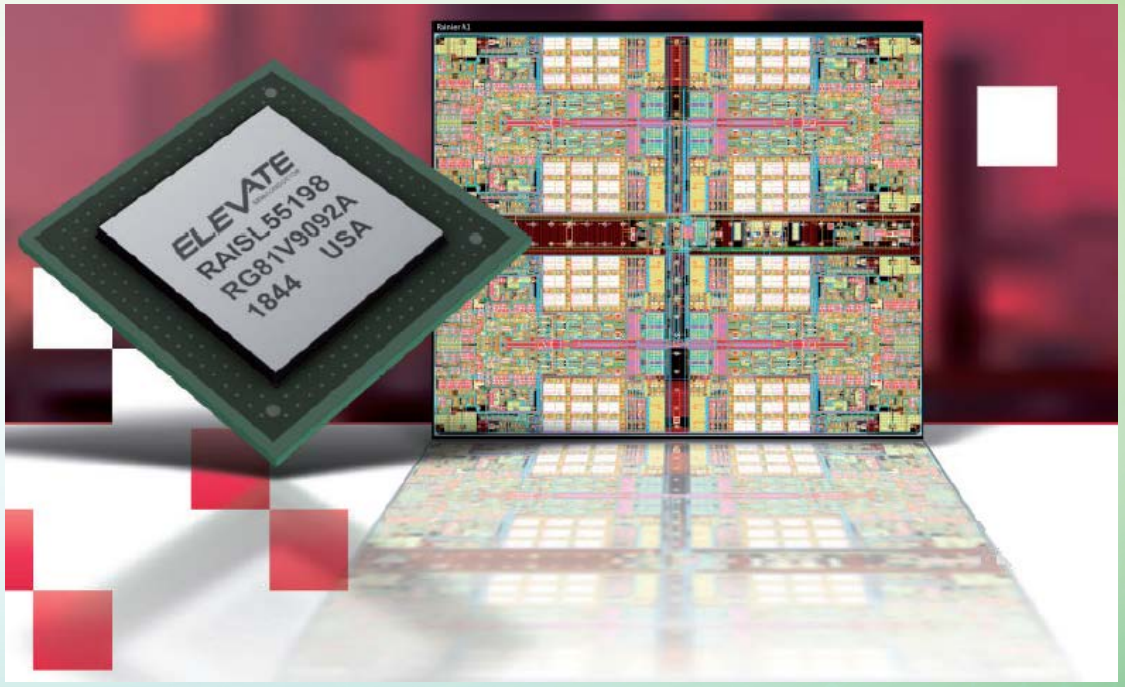
# Elevate's New Solutions:  Pin Electronics

**Rainier**

- Lowest power, fully-integrated 2Gbps octal PE
- High-density design includes integrated PPMU/DAC/Deskew/Load
- < 500mW/channel

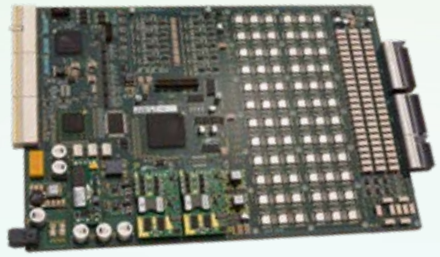
**Longs Peak**

- Octal 7.5Gbps PE
- < 1W/channel (target)
- Integrated timing generation

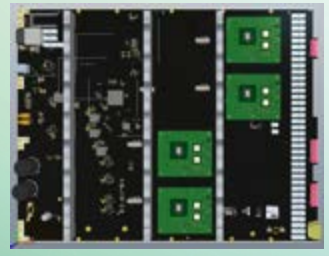


# Collaboration

## Instruments



HD VI based on Jupiter



IO core based on Mystery DPIN16 module, PXI: 32/64

HD PMU based on Neptune

## Custom & Semi-Custom Engagements

**We are flexible and value customer input as we develop solutions together**

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# Thank You


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