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SWTEST
PROBE TODAY, FOR TOMORROW
2023 CONFERENCE

# IMPORTANCE OF CERAMIC SUBSTRATES WITH LOW THERMAL EXPANSION COEFFICIENT IN SEMICONDUCTOR WAFER TESTING

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SEMCNS
Stand up with Electro Material Ceramic aNd Solution

## • Introduction

*STF : Space TransFormer

- SEMCNS provides a solution for large area STF* products using LTCC materials for semiconductor wafer inspection processes.

**History**

- 2023 • New factory in Osong
- 2022 • Became an enterprise of middle standing
- 2021 • Listed on KOSDAQ
- 2020 • Progress of national projects • $10 million Export Tower
- 2019 • Voted World Class Product of Korea • 10 billion won in overseas sales
- 2018 • ISO9001 certification • Selected as National Project (Advanced Technology Center)
- 2017 • New entry into Global IDM
- 2016 • Established SEMCNS Co.,Ltd.
- 2007 • Started to develop LTCC for probe card

**Main Product**

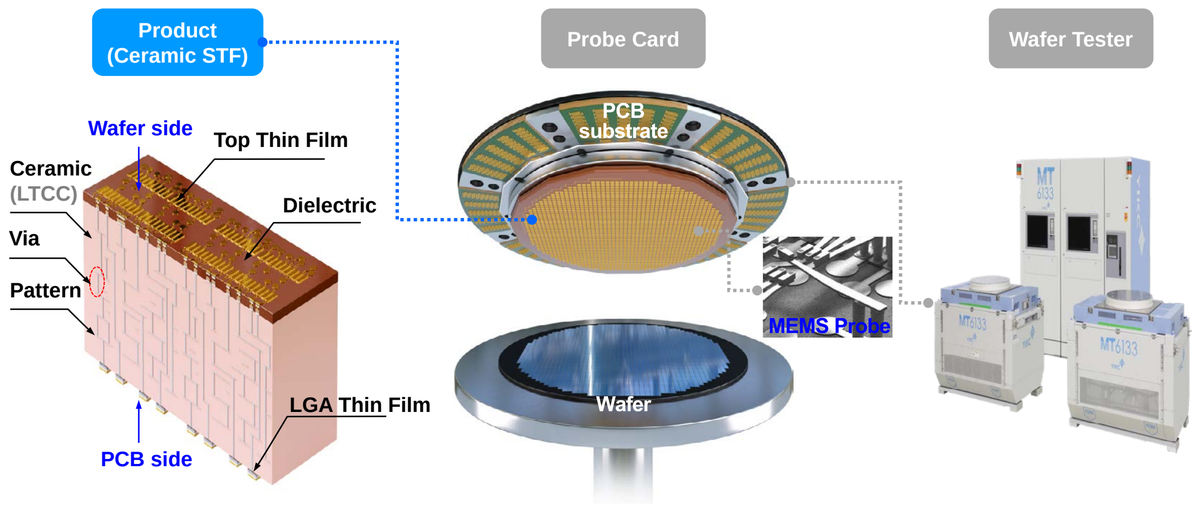
Ceramic STF for Semiconductor Wafer Inspection Process

**Key Technology**

100% in-house Continuous line manufacturing

| Ceramic Technology | Grinding Technology |
|---|---|
| The strength, electrical connectivity and position precision of ceramic STF | Adapt to high quality thin film, customer optimal shape implementation |
| **Thin Film Technology** | **Design Technology** |
| Development of multi-layered thin film technology suitable for customer's process | Suitable for customer's design requested by SEMCNS's own Design technology |

**Product Outline**

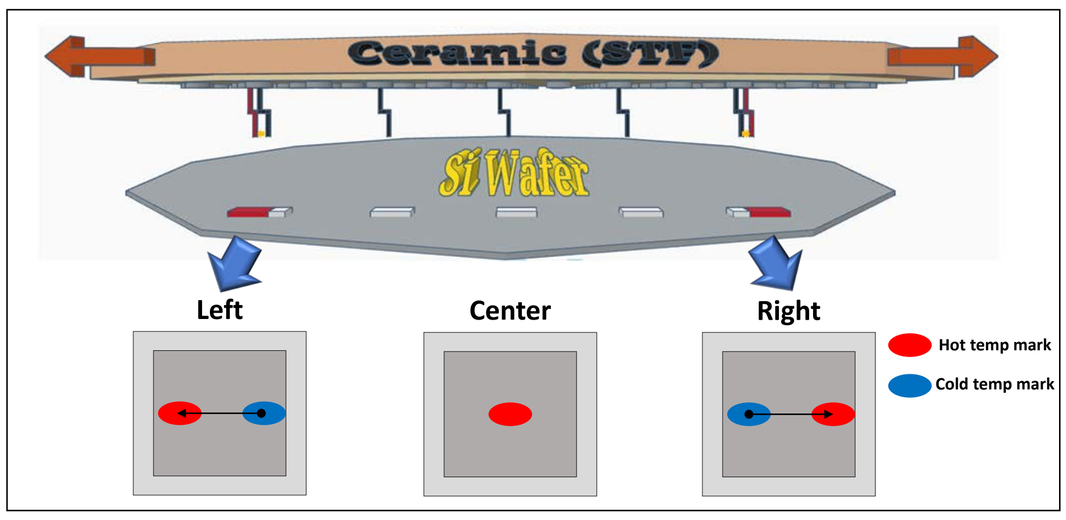



* CTE : Coefficient of Thermal Expansion

- Pin scrub occurs on the wafer pad during the wafer testing, which is caused by the difference in CTE* of wafer and STF.
- Recently, precise control of pin scrub is required and market trend needs a Low CTE material.
- There are three reasons why Low CTE material is needed for semiconductor Probe Cards.

1) There are increasing adoptions of automotive parts and environmental temperature is increasing.

| Test Temperature | Normal | Automotive |
|---|---|---|
| Cold Temp.(℃) | -25 | -50 |
| Hot Temp. (℃) | +95 | +125 |

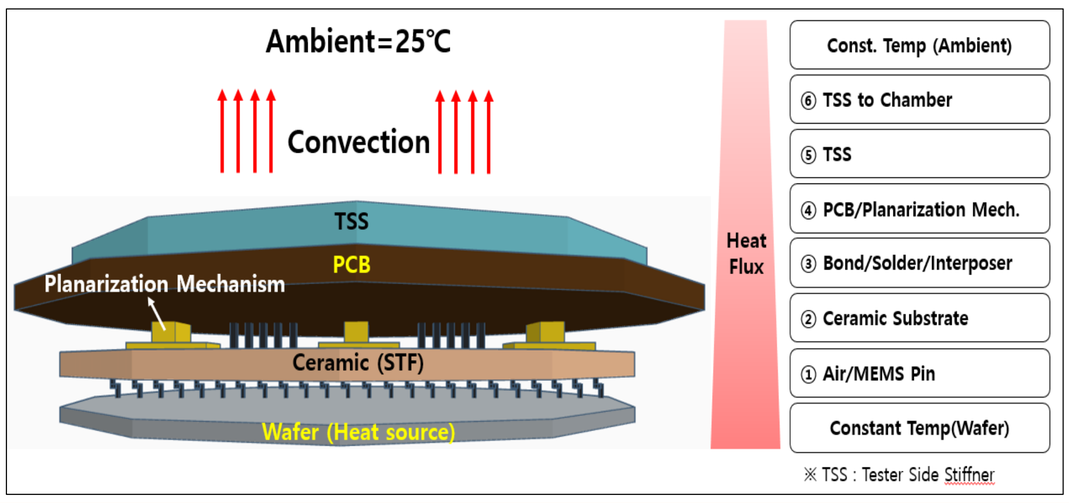



2) The # of Probe Pins is increasing due to an increase in the Parallelism of wafers.

| Pins | Normal | High Density |
|---|---|---|
| # of Pins (K) | 1x | 2x ~ 3x |

3) The pad size for semiconductors is reducing.

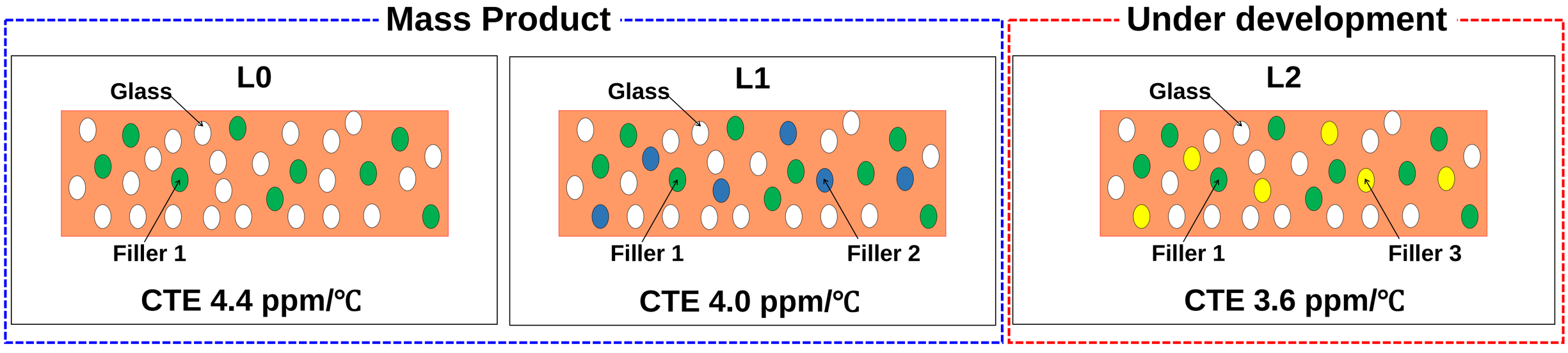
| Pad | Present | Near future |
|---|---|---|
| Pad Size (㎛) | 62.5 x 60 | 50 x 50 |




## • Approach

- Producing and developing STF using LTCC materials with three different CTE values.

- L0 : Crystallization Glass + Filler 1 → CTE 4.4 ppm/℃ (Mass-production)
- L1 : Crystallization Glass + Filler 1 + Filler 2 (Low CTE) → CTE 4.0 ppm/℃ (Mass-production)
- L2 : Crystallization Glass + Filler 1 + Filler 3 (Low CTE) → CTE 3.6 ppm/℃ (Under Development, ~2024)



- **Results**
  - The characteristics of the LTCC material on mass-production are as belows.

| | CTE at 25~100℃ (ppm/℃) | Dielectric Constant at @1MHz | Dielectric Loss at @1MHz | Modulus (MPa) | Thermal Conductivity (W/m·K) | Specific Heat (J/g·K) |
|---|---|---|---|---|---|---|
| L0 | 4.4 | 7.73 | 0.0019 | 117 | 2.28 | 0.749 |
| L1 | 4.0 | 7.40 | 0.0025 | 118 | 1.97 | 0.748 |

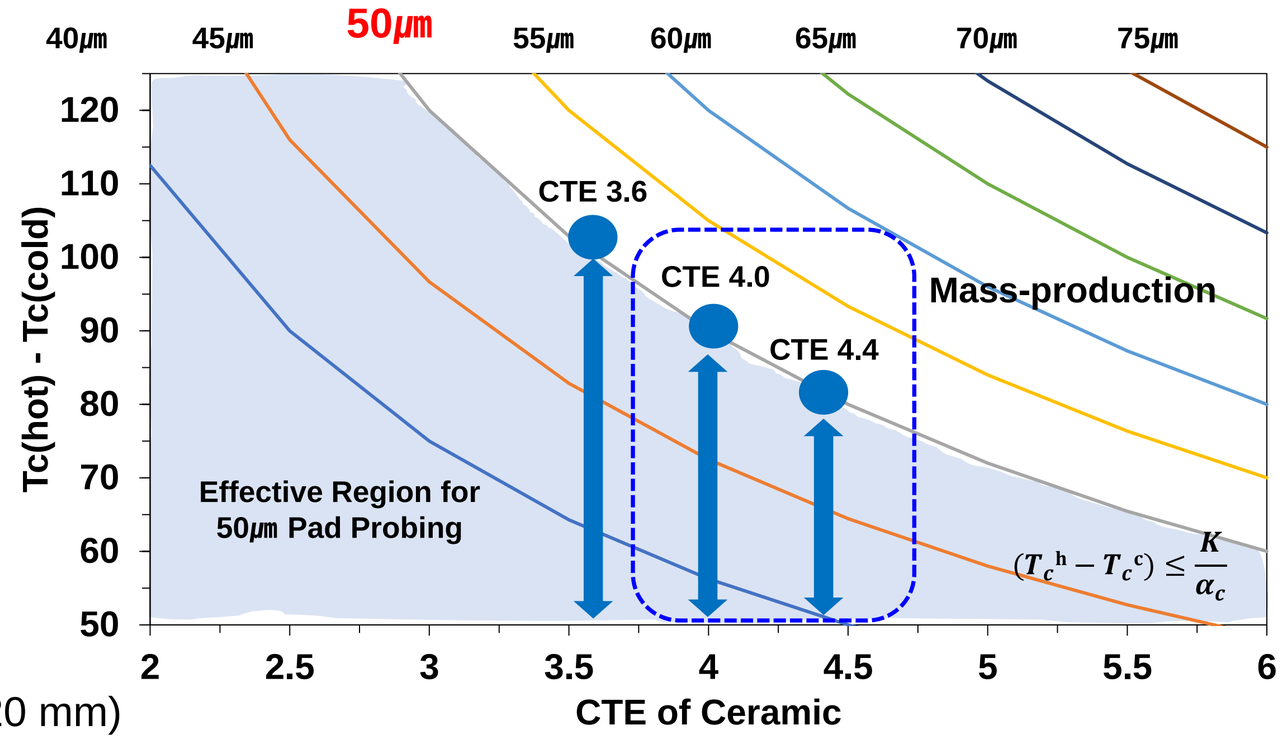
※ The CTE value was measured on a 12-inch STF using 3D vision measurement. (25~100℃)

  - Using the L1 materials, it can provide a CTE of 3.87ppm/℃ at 25℃~100℃ and CTE of 3.60ppm/℃ at -40℃~140℃.

* TMA : **T**hermo**M**echanical **A**nalysis

| Temp. Range (℃) | TMA* CTE (ppm/℃) | |
|---|---|---|
| | SEMCNS LTCC | |
| | L0 | L1 |
| 25~100 | 4.36 | 3.87 |
| -40~120 | 4.19 | 3.49 |
| -40~140 | 4.27 | 3.60 |

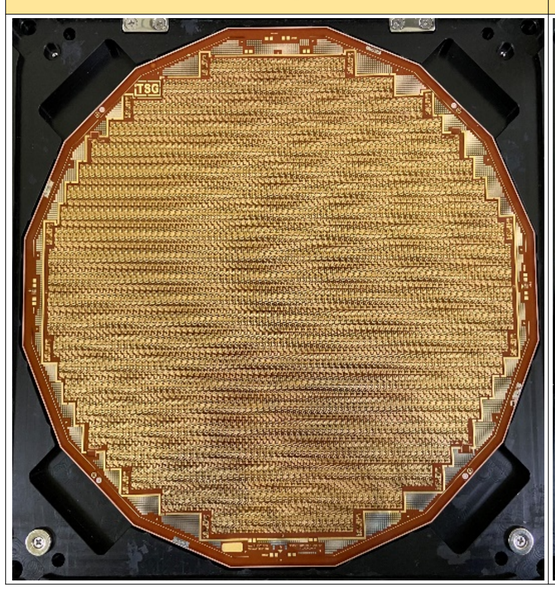
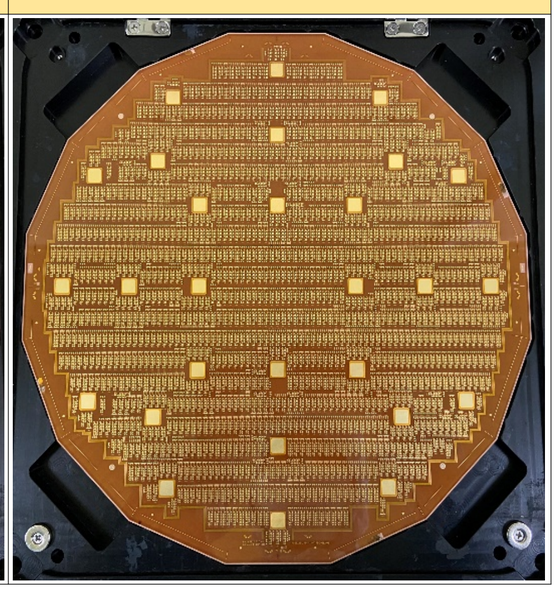
※ The CTE value was measured by TMA (5 x 5 x 20 mm)

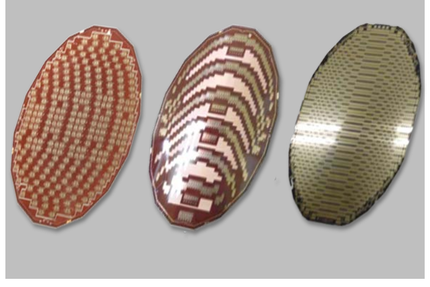
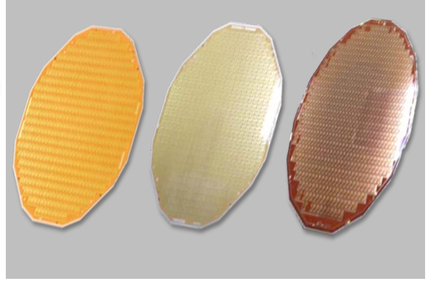
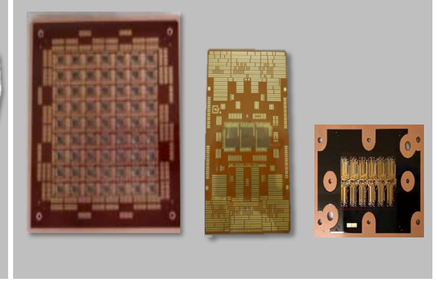



※ Credit : 2013 SWTW by Y.H.Park

  - Producing a variety of product using L0 and L1 materials.
  - As the CTE is decreasing, it is being developed to respond to high-spec and diverse products.

*CIS : CMOS Image Sensor

| Top | Bottom |
|---|---|
|  |  |

| 12" DRAM | 12" NAND | CIS * / Parametric |
|---|---|---|
| Total Pin : 60K ~ 100K<br>Ceramic Inner Layer : 15 ~ 35<br>Thin film Layer : 5 | Total Pin : 10K ~ 63K<br>Ceramic Inner Layer : 10 ~ 43<br>Thin film Layer : 2 | Total Pin : 30K ~ 40K<br>Ceramic Inner Layer : 40 ~ 80<br>Thin Film Layer : 2 |
| Mass Production | Mass Production | On-Going Development |
|  |  |  |

- **Conclusion**
  - Develop Low CTE materials (L1) about CTE 4.0ppm/℃.
  - Improved pin scrub using L1 materials.
  - CTE 4.4 and 4.0ppm/℃ are currently in mass production.
  - CTE 3.6ppm/℃ is under development. (~2024)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