SWTEST

PROBE TODAY, FOR TOMORROW

2023 CONFERENCE

High Speed Probe Card Architecture for High End Devices

AMD

Xin Reng Foo – AMD Singapore
Chee Hoe Lin – AMD Singapore
Raffaele Vallauri –Technoprobe Italy
Alberto Berizzi – Technoprobe Italy

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Overview

- Introduction
- Challenges
- High End Probe Card Requirements
- Probe Head Design Optimization
- Simulation Data
- Characterization Data

Data Intensive Markets

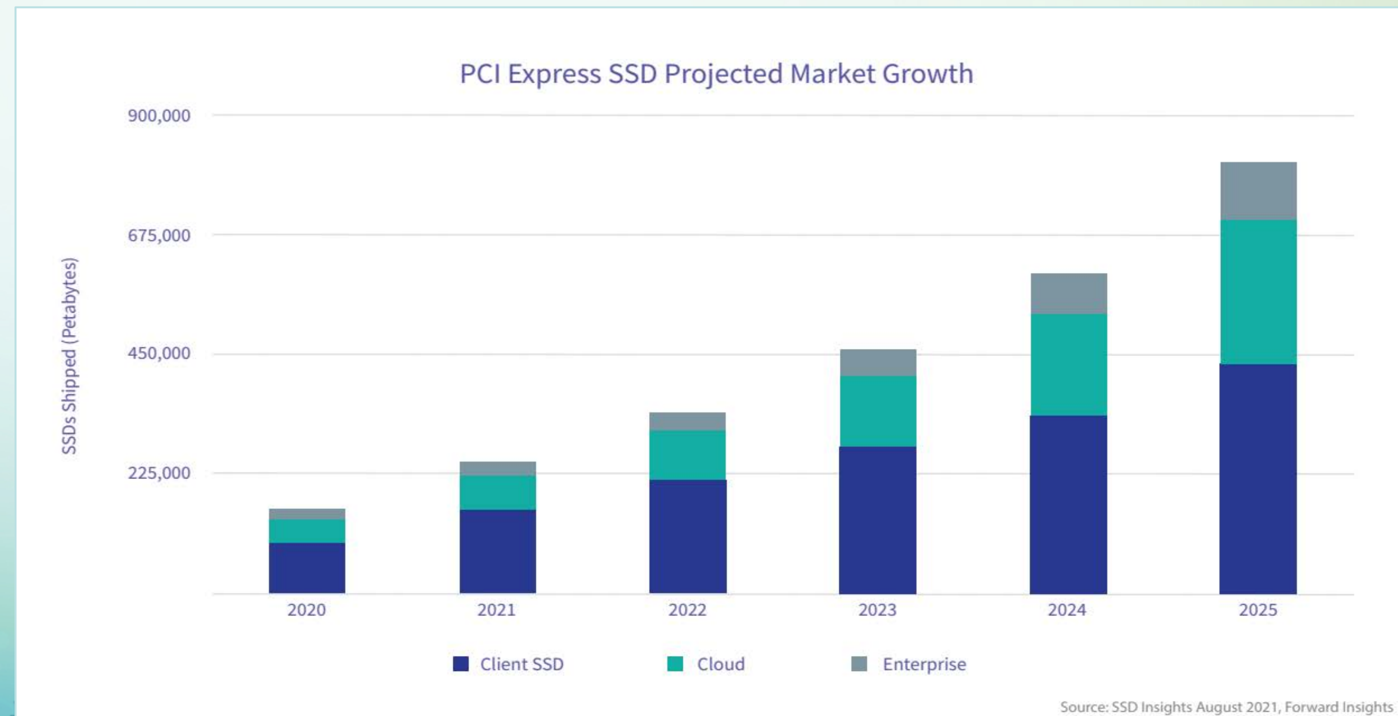
High Performance Computing (HPC)

Automotive

Military and Aerospace

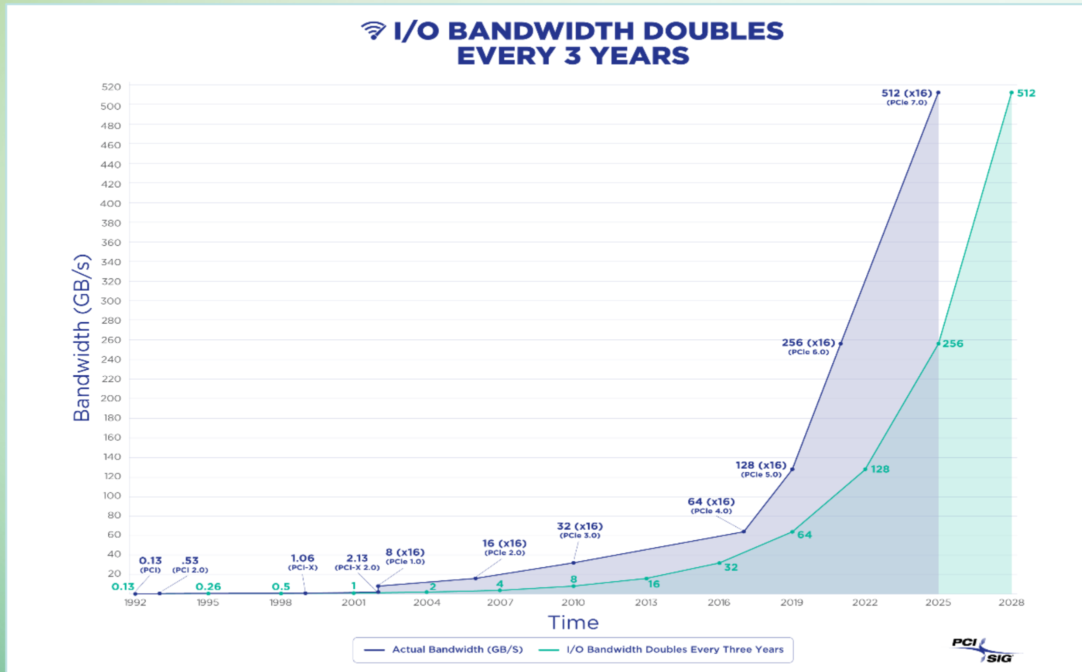
Artificial Intelligence (AI) and Machine Learning (ML)

Data Centre



Data Rate Explosion

- PCIe specification doubles the I/O bandwidth every three years to meet industry demand



Specifications	Lanes x1	x2	x4	x8	x16
2.5 GT/s (PCIe 1.x +)	500 MB/S	1 GB/S	2 GB/S	4 GB/S	8 GB/S
5.0 GT/s (PCIe 2.x +)	1 GB/S	2 GB/S	4 GB/S	8 GB/S	16 GB/S
8.0 GT/s (PCIe 3.x +)	2 GB/S	4 GB/S	8 GB/S	16 GB/S	32 GB/S
16.0 GT/s (PCIe 4.x +)	4 GB/S	8 GB/S	16 GB/S	32 GB/S	64 GB/S
32.0 GT/s (PCIe 5.x +)	8 GB/S	16 GB/S	32 GB/S	64 GB/S	128 GB/S
64.0 GT/s (PCIe 6.x +)	16 GB/S	32 GB/S	64 GB/S	128 GB/S	256 GB/S
128.0 GT/s (PCIe 7.x +)	32 GB/S	64 GB/S	128 GB/S	256 GB/S	512 GB/S

Source: PCI -SIG

- Demand for a reliable, high-speed, low latency I/O interconnect for data-intensive applications and markets, (Artificial Intelligence and Machine Learning (AI/ML), High Performance Computing (HPC), Quantum Computing, Hyperscale Data Centers and Cloud)

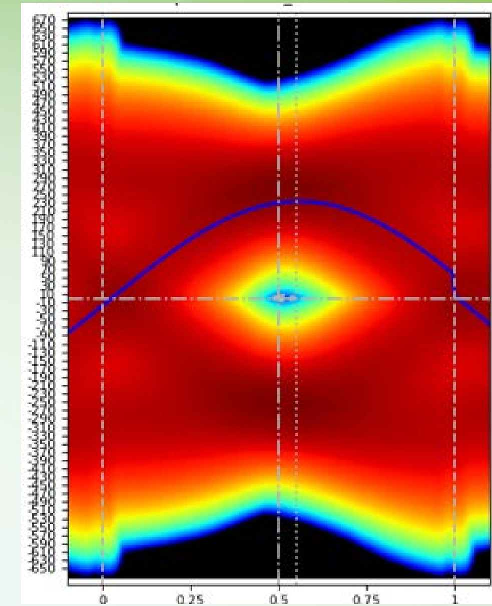
Challenges

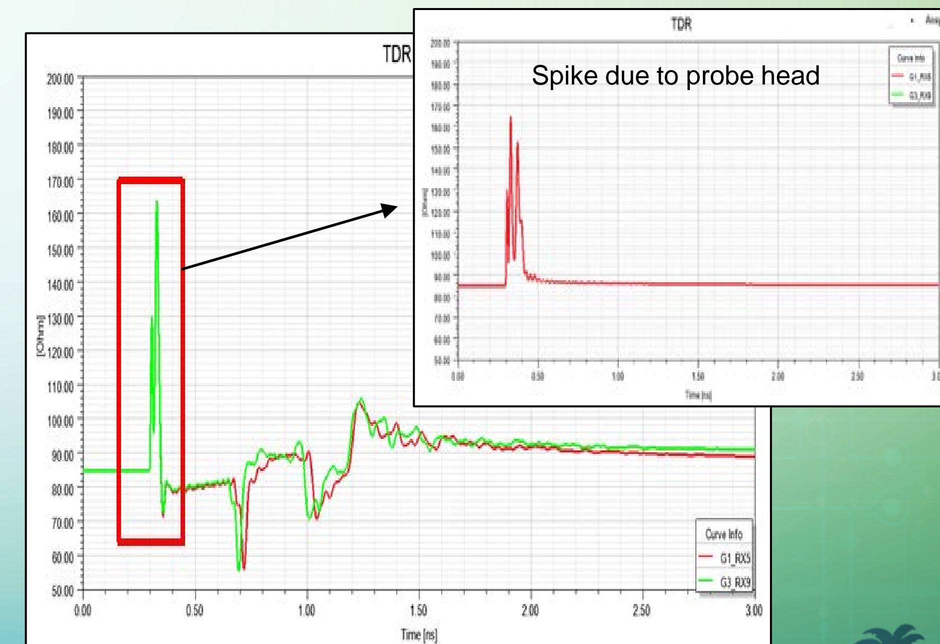
- **Bump pattern is not optimized for probe solution Signal Integrity**
  - ➢ **Probe impedance is strongly dependent on bump pattern**
  - ➢ **Crosstalk is strongly dependent on Signal/Ground ratio**

- **Existing probe solution is a closed eye at NRZ 25GT/s**
  - ➢ **Impedance mismatches at probe head to probe card**

- **Standard probe card solution in the market does not offer high speed, high current carrying capacity and high lifetime at the same time**

- **Unable to support full external loopback coverage at Sort in the early stages of product test**



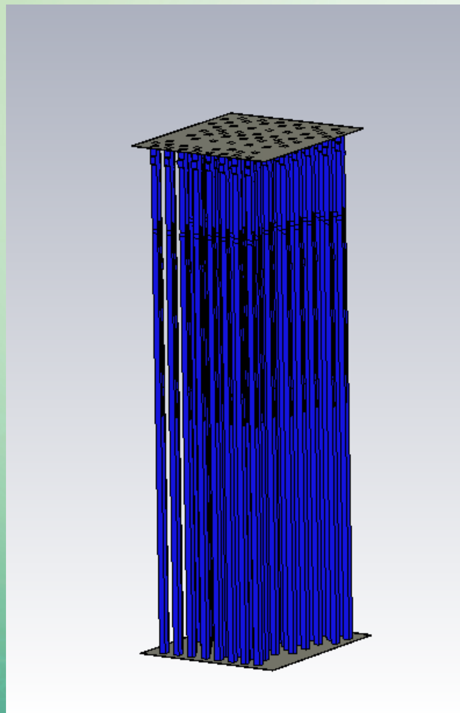


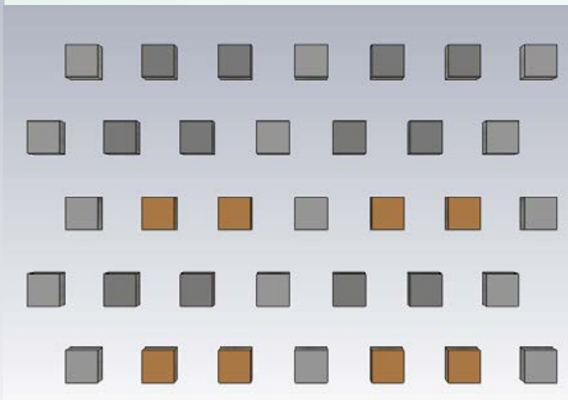
High End Probe Card Requirements

- High Current Carrying Capacity
- Multi site parallelism capability
- High probe count capability up till 35K
- High probe lifespan of more than 1.5 M
- Stable /Low Contact Resistance
- Low Mean Time Before Failure
- Ability to handle dual temperature testing
- HSIO routings need to meet
  - differential / single ended impedance target for overall path (includes loopback through direct trace, relays, bias-T, and high-speed routes to ATE tester)
  - high-speed end-to-end requirement for HSIO loopback path (up to 32GT/s NRZ)
- Meeting all supplies IR drop (50mv) and Site-Site IR drop delta requirement (10%)

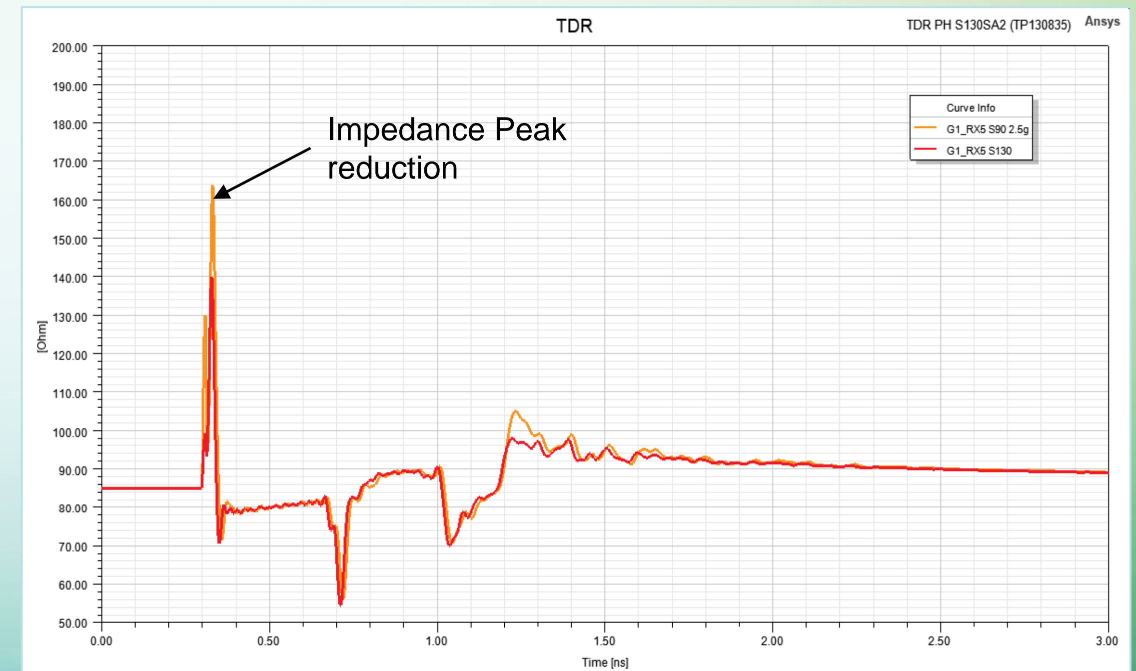
Probe Characteristics – Optimization Strategy

- Optimization of the probe dimension to reduce impedance peak
- Lower the probe impedance spike by optimizing the cross section of the probe in relation with the signal to ground pitch
- Adoption of Hybrid Probe solution allows more degrees of freedom to improve the impedance peak





Min pitch considered 130um with “chess” layout



Probe Simulation - Optimizing Probe Cross Section

TDR (CS Standard)

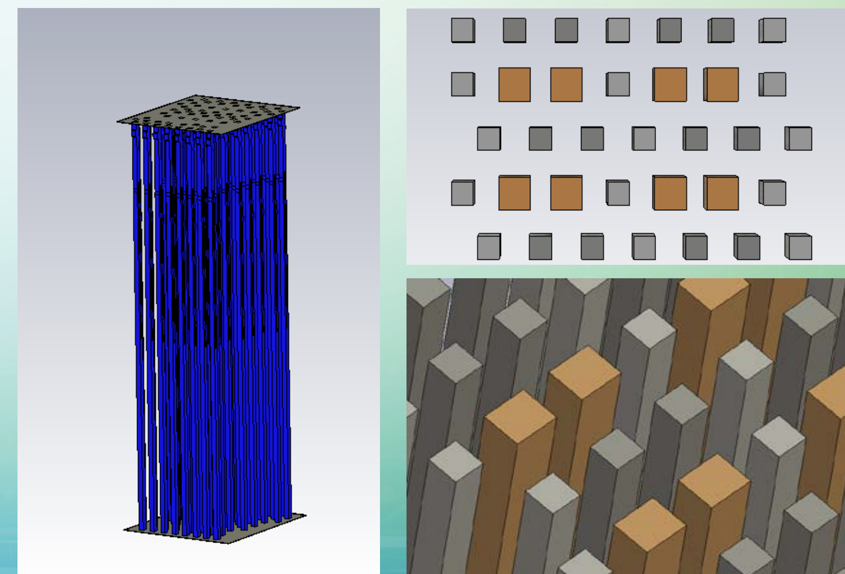
TDR (CS + 20%)

TDR (CS + 40%)

TDR (CS + 70%)

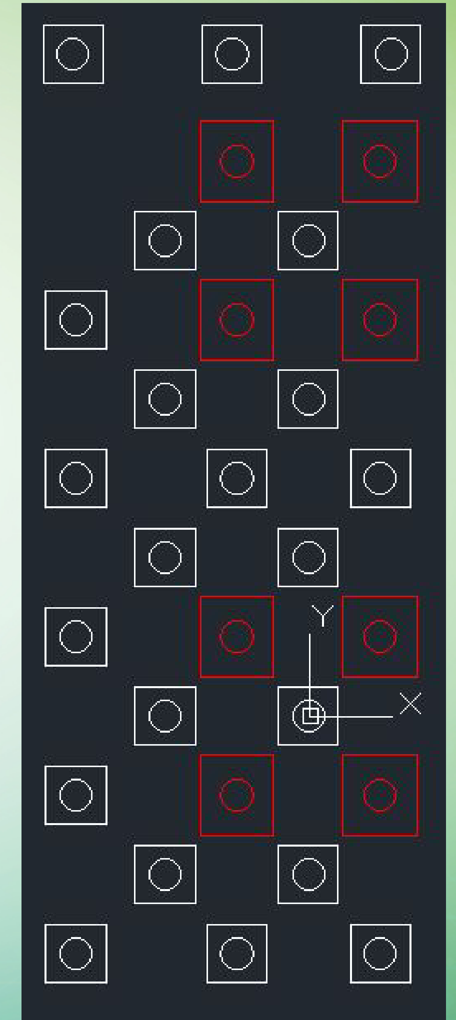
TDR (CS + 100%)

- **Simulations give best results using probes for loopback signals enlarged at +20/+40 % cross section**

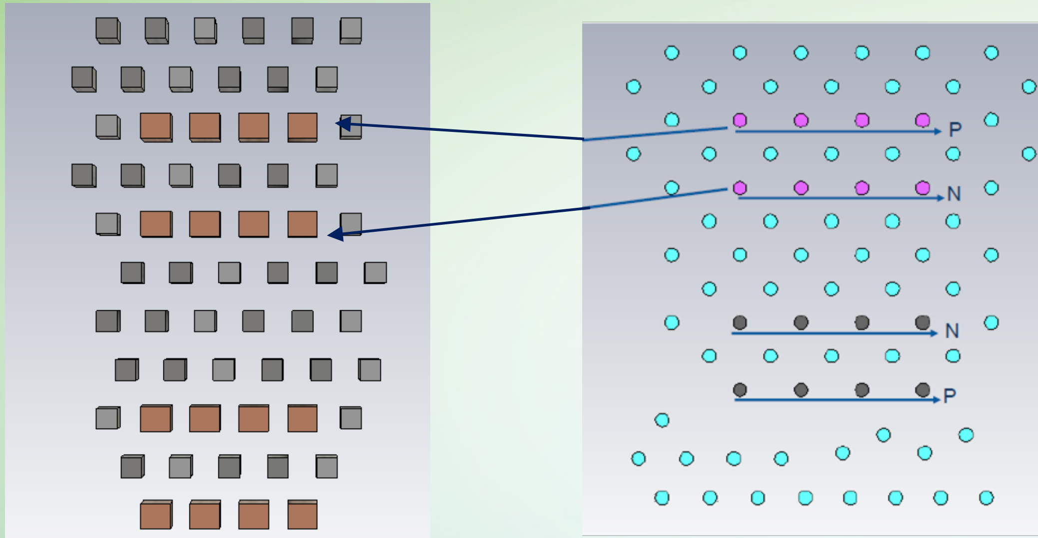


Probe Characterization - Physical Constraints for Probe Placement

- Each probe is inserted in a placeholder (*holes* in the ceramic plates)
- Increasing probes cross section results in holes dimension increase
- Hole clearance between closest probes must be compliant with design rules for structural integrity of the probe head
- Based on layout/pattern of 133um pitch
  - Red are placeholders for larger probes
  - White are placeholders for thinner probes
- Characterisation of W +20% cross section probe is still meeting the design specification
- Any further cross section increasing will impact the structural integrity of the probe head



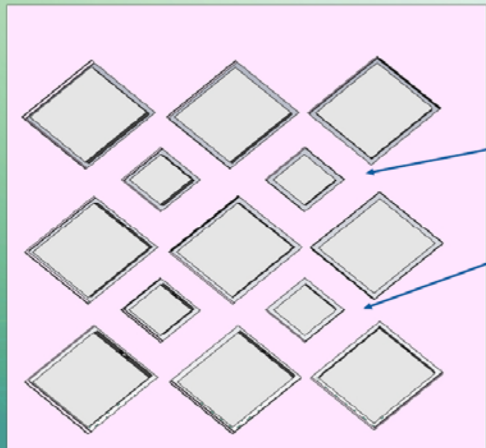
Probe Characterization - Optimizing Crosstalk Performance

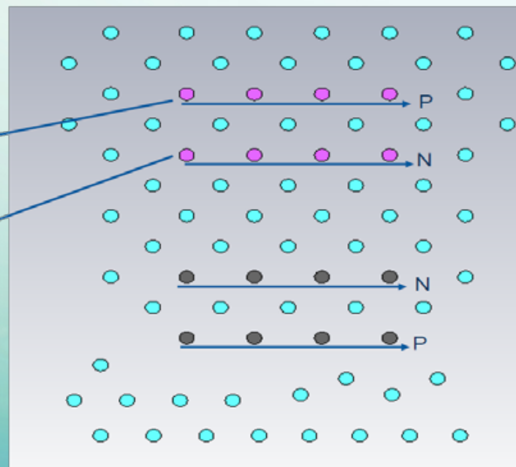


Probe signals enlarged at +20% cross section caused

- Increase of Return Loss and Insertion Loss compared to standard.
- Decrease of Xtalk performance compared to standard.

To get an increase of both RL and IL and Xtalk performance we worked on placement and rotation





Strategy 1: "Inversion" Probe placement concept:

- Small signal pins, larger GND pins

Strategy 2: Rotated concept for probes placement at 45° (Coaxial) ("Faraday's cage"):

- Fields within a conductor cancel out with any external fields (electric field within a conductor is zero)

Probe Card Design – End to End

EXTERNAL LOOPBACK CHANNEL MODEL

85 Ω
TX Die
Probe Pin
PCS
WS PLB Loopback
PCS
Probe Pin
RX Die
85 Ω

TX DUT pad
RX DUT pad
ProbeHead
PCS
PCB

head_
MLO
ProbeHead
wafer
tip_

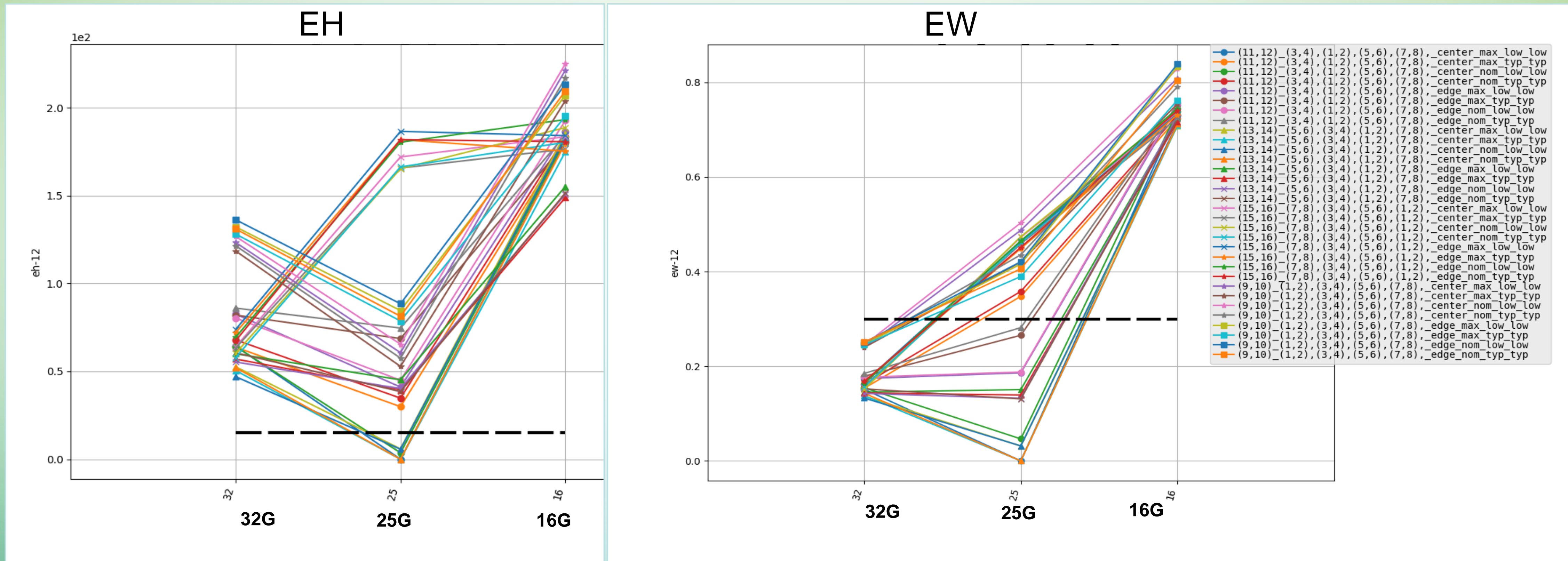
Source: Wikipedia-Merlion

Co-Develop with Technoprobe for the next generation *Merlion* Probes series to meet AMD HSIO test requirement

Merlion: Official mascot of Singapore. A mythical creature with the head of a lion and the body of a fish like a hybrid probe solution

Channel Simulation - Optimizing Probe Dimension

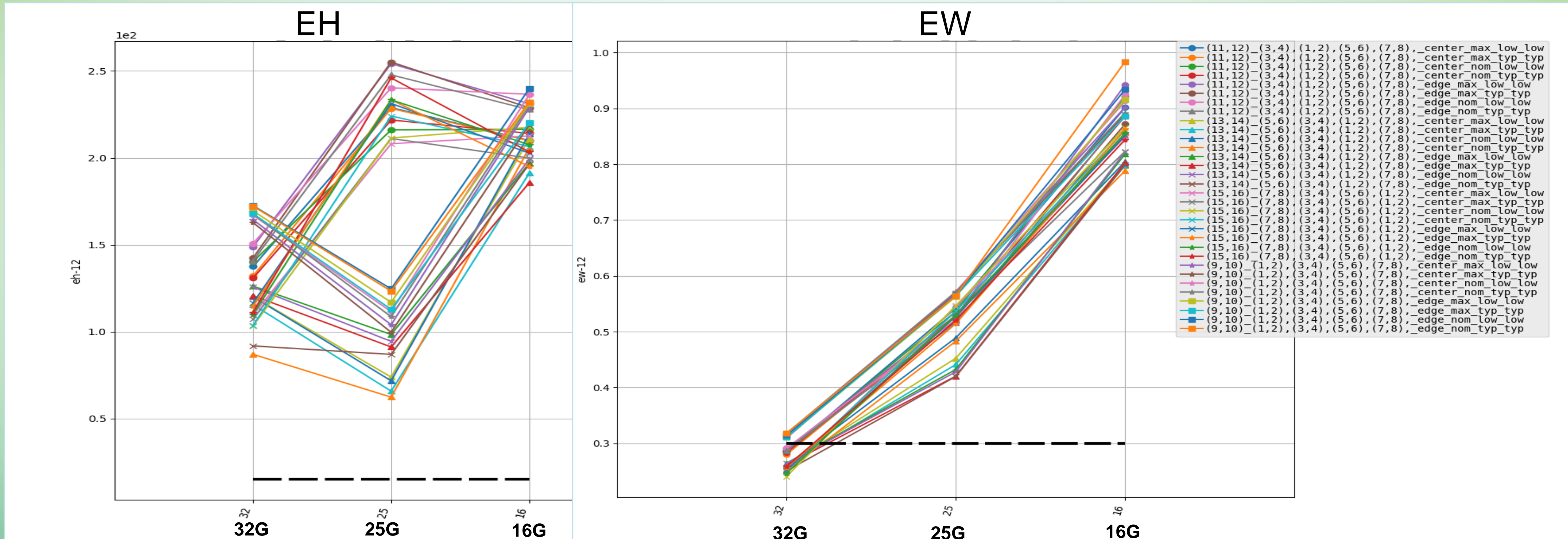
Probe Needle	Probe Length	Probe Dimension	Rotation	Probe Intrinsic Resonant
Merlion 1	REF	CS + 20 %	0°	25GHz



- Loopback @ 32GT/s. Sufficient margin for Eye Height, but Eye Width not meeting UI target
- Considering channel margin and manufacturing variation, it is not possible for loopback test to meet 32G requirement

Channel Simulation - Optimizing Probe Dimension

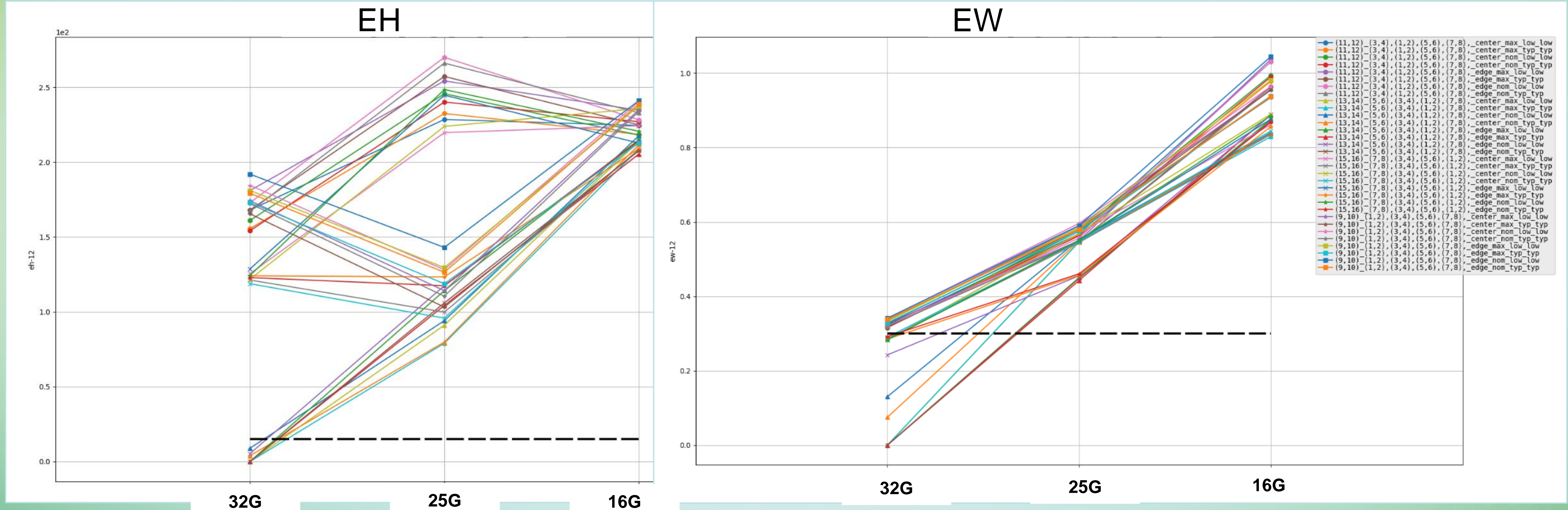
Probe Needle	Probe Length	Probe Dimension	Rotation	Probe Intrinsic Resonant
Merlion 2	L – 25%	CS + 20 %	0°	30GHz



- Loopback @ 32GT/s. Nominal channel design and HVM corners meeting Eye Height but not Eye Width target. No margin for EW
- Loopback @ 25GT/s. Meeting EH and EW targets with margins

Channel Simulation - Optimizing Probe Dimension

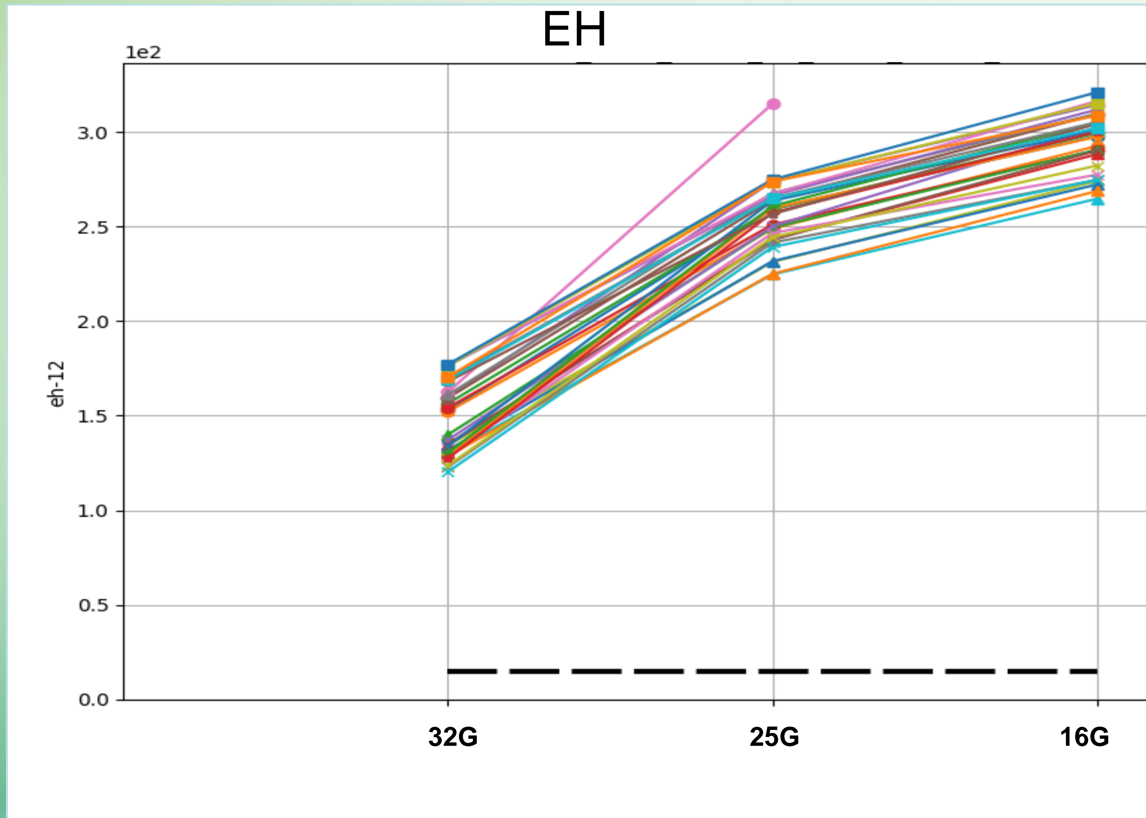
Probe Needle	Probe Length	Probe Dimension	Rotation	Probe Intrinsic Resonant
Merlion 3	L – 40%	CS + 20 %	0°	40GHz

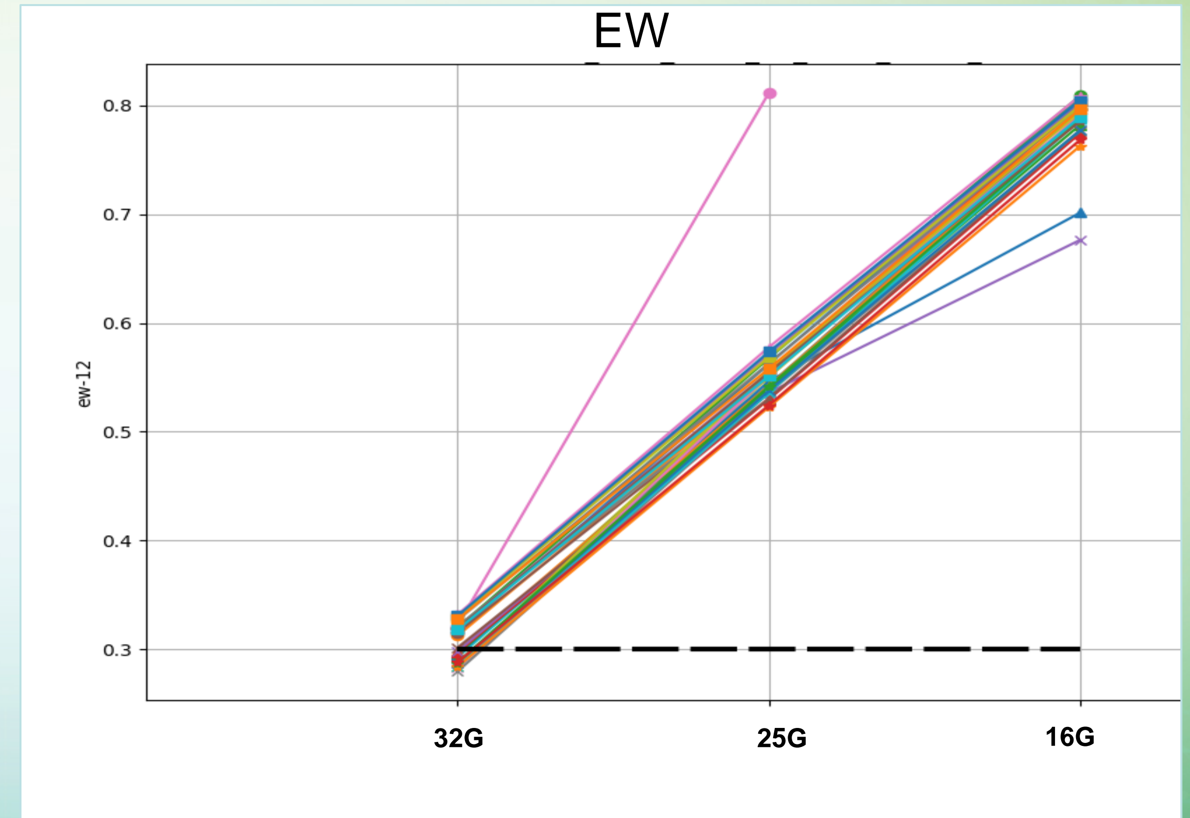


- Loopback @ 32GT/s. Nominal channel design and most HVM corners meeting EH and EW targets
- Loopback @ 25GT/s. Meeting Eye Height and Eye Width targets with margins
- Some HVM corners are not meeting 32GT/s, improvement in probe head design is needed for more margin

Channel Simulation - Optimizing Probe Dimension and Placement

Probe Needle	Probe Length	Probe Dimension	Rotation	Probe Intrinsic Resonant
Merlion 4	REF	Optimized	45°	27GHz

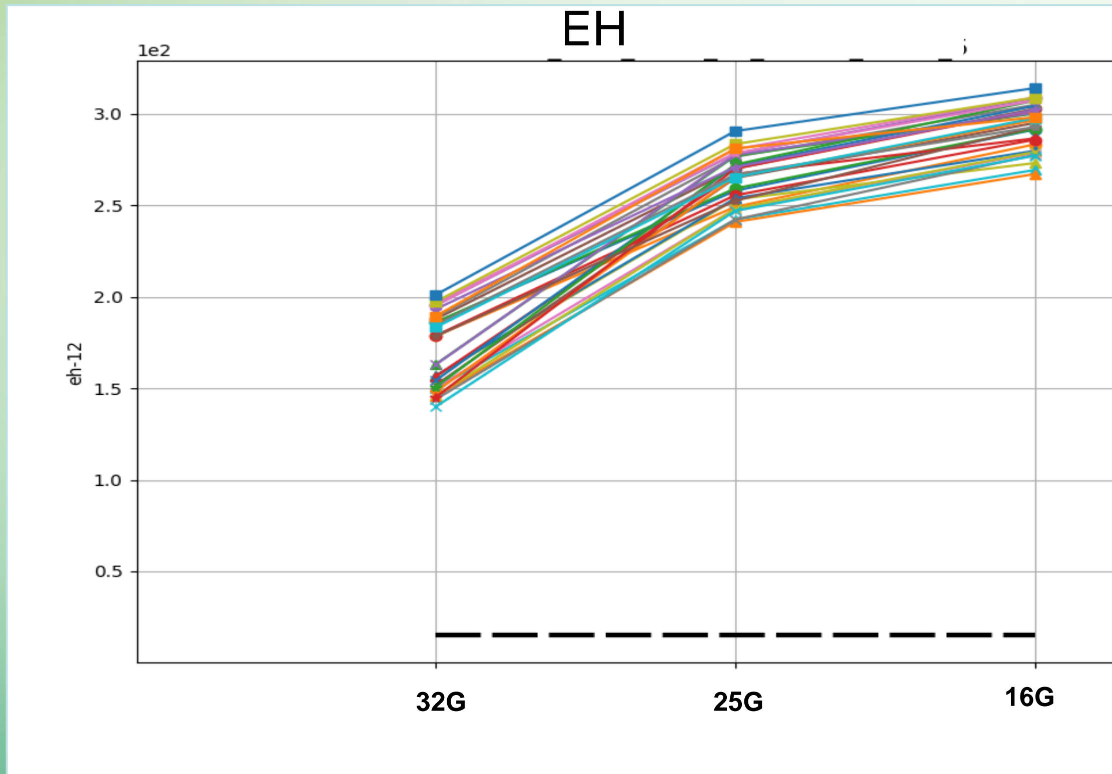


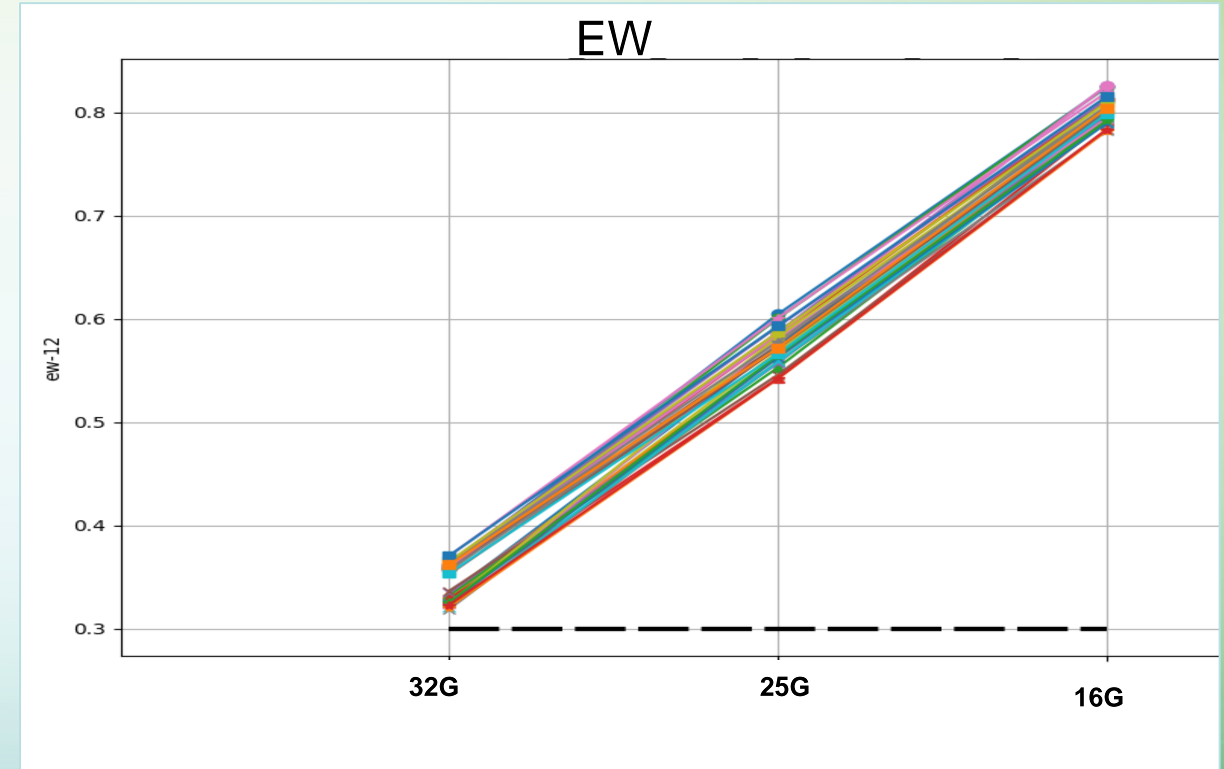


- **Loopback @ 32GT/s Meeting EH but EW has no margin**

Channel Simulation - Optimizing Probe Dimension and Placement

Probe Needle	Probe Length	Probe Dimension	Rotation	Probe Intrinsic Resonant
Merlion 5	L – 25%	Optimized	45°	34GHz

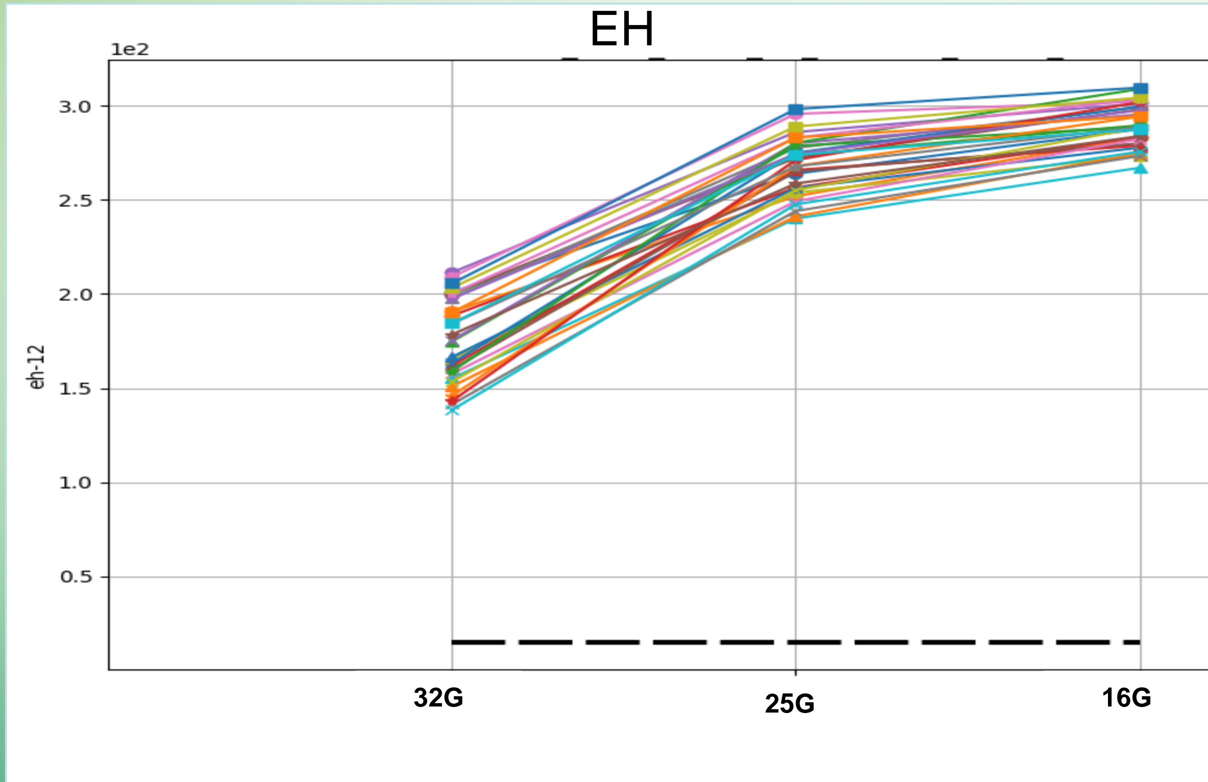


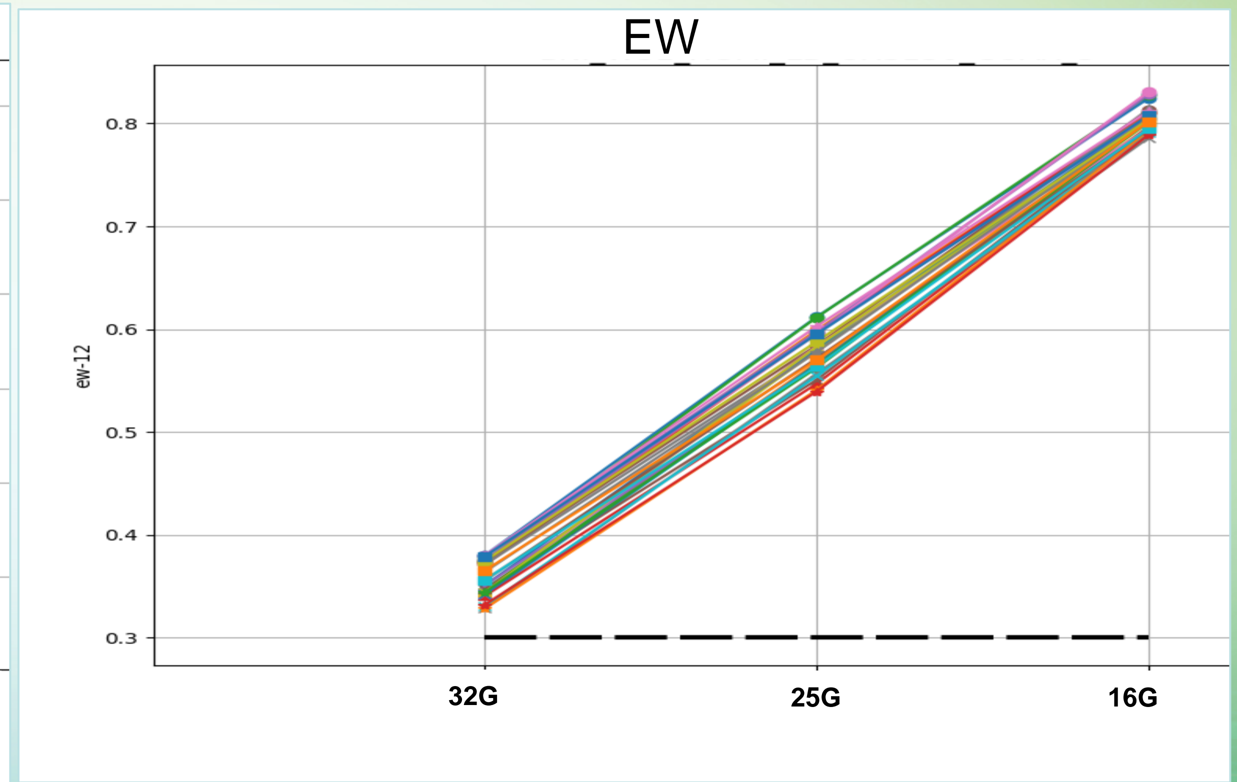


- Loopback @ 32GT/s. Meeting both EH and EW with margins

Channel Simulation - Optimizing Probe Dimension and Placement

Probe Needle	Probe Length	Probe Dimension	Rotation	Probe Intrinsic Resonant
Merlion 6	L – 40%	Optimized	45°	40GHz





- Loopback @ 32GT/s. Meeting both EH and EW with best margins

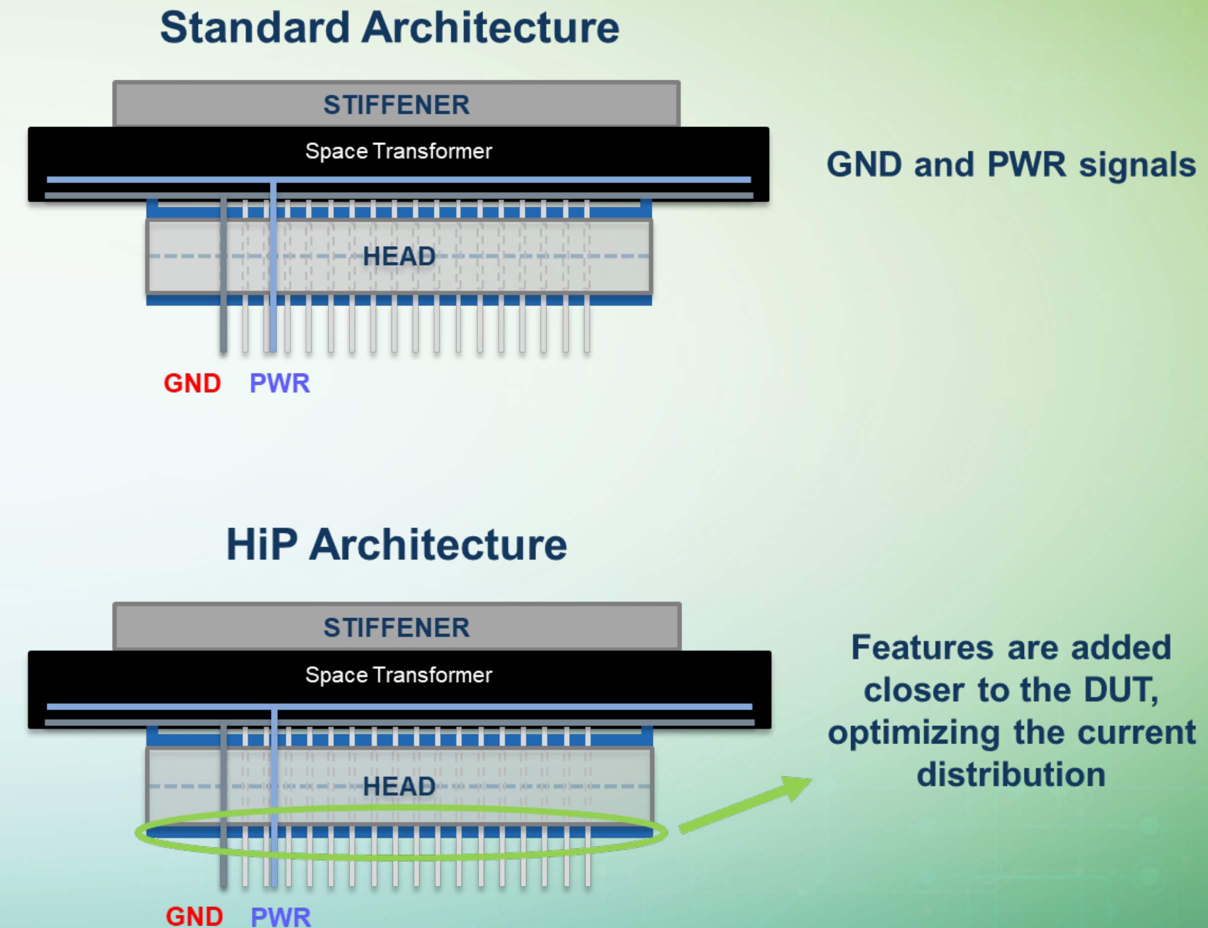
Probe Selection Summary

Probe Needle (Hybrid)	Probe Length	Probe Dimension	Rotation	Probe Intrinsic Resonant	Insertion to Crosstalk Ratio (ICR)	Nominal Channel Eye Width and Height
Merlion 1	REF	CS + 20%	0°	25GHz	20dB	120mV , 0.25UI
Merlion 2	REF – 25%	CS + 20%	0°	30GHz	26dB	130mV , 0.28UI
Merlion 3	REF – 40%	CS + 20%	0°	40GHz	26dB	150mV , 0.31UI
Merlion 4	REF	Optimized	45°	27GHz	28dB	169mV , 0.32UI
Merlion 5	REF – 25%	Optimized	45°	34GHz	26dB	184mV,0.36 UI
Merlion 6	REF – 40%	Optimized	45°	40GHz	25dB	184mV,0.36 UI

- Hybrid probing with coaxial structure design improves the probe needle SI performance significantly
- For coaxial design approach, probe impedance is highly influence by the C4 bump S/G pattern
- Hybrid probe needle Merlion 6 can meet external loopback requirement @ 32GT/s NRZ. It is the best SI performance probing solution and could potentially extend the reach to 64GT/s NRZ

HiP PH Architecture

- Technoprobe Patented solution
- HiP architecture
  - additional features are inserted in the PH with the aim of distributing the current more evenly at PWR and GND level
- This results in an increased CCC of probes, when those are combined with HiP architecture



Merlion 6 Probe Head – Main features

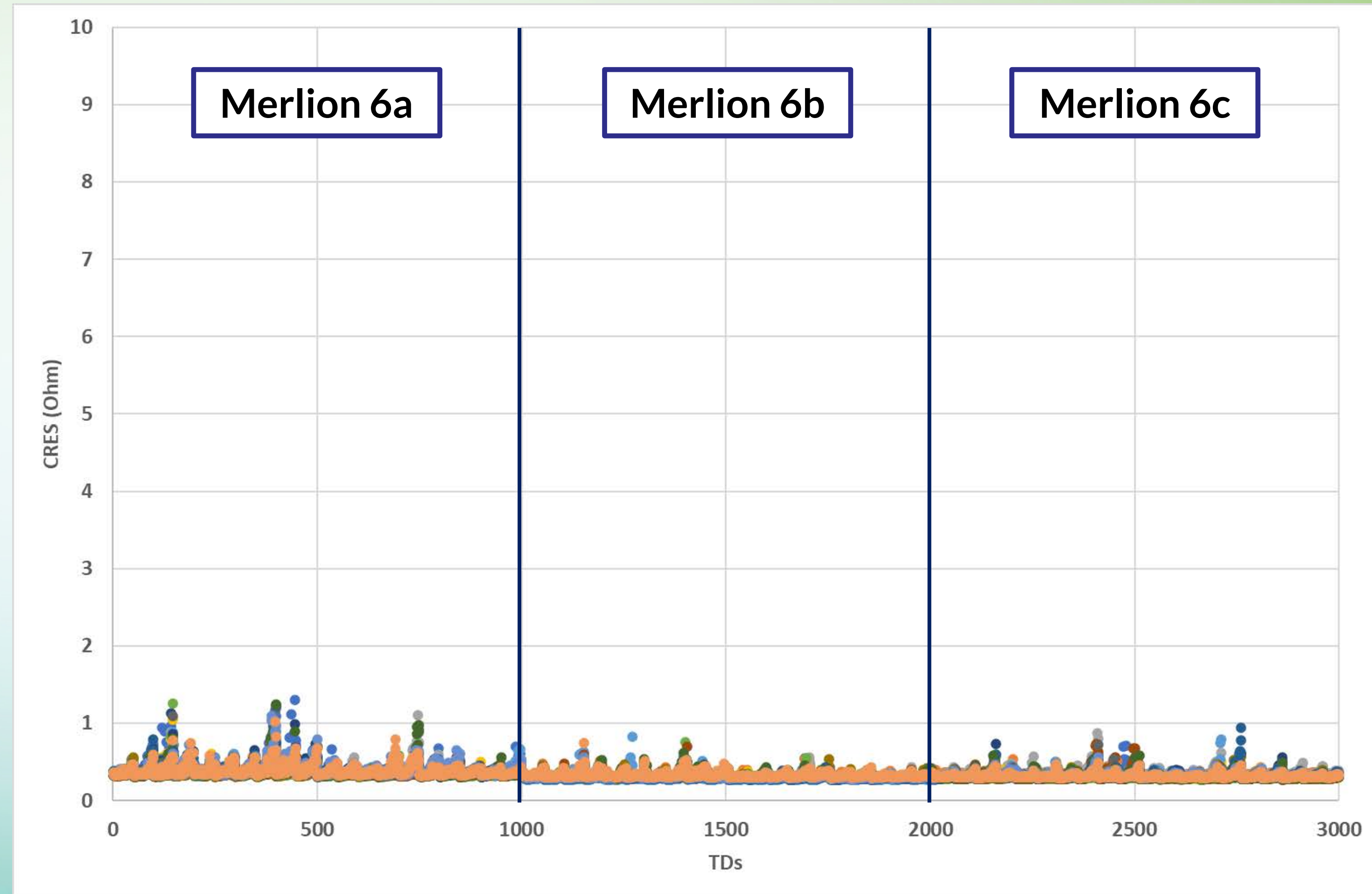
- Hybrid Probe head
  - 3 different probe designs to optimize CCC/MAC and high speed performances
- HiP (High Power PH) architecture
  - Minimize probe burnt and maximize MTBF

Technology name	Merlion 6a	Merlion 6b	Merlion 6c
Tip	Flat	Flat	Flat
XLT	YES	YES	YES
Radial alignment [µm]	8	8	8
Z planarity [µm]	Δ = 20	Δ = 20	Δ = 20
Min pitch: Linear	90 µm	100 µm	120 µm
Min pitch: Full array regular	90 µm	115 µm	150 µm
Min pitch: Full array any angle	110 µm	135 µm	170 µm
CCC/MAC [mA]	1450/1300 HiP: 2700/2400	1500/1400 HiP: 2800/2500	1900/1700 HiP: 3000/2700
Force (at 75 um OT)	1.8 g	2.3 g	3.2 g
Temperature range	-45 to +175 °C	-45 to +175 °C	-45 to +175 °C
Probe alloy	SA2	SA2	SA2
Max working OD	100 µm	100 µm	100 µm

Merlion 6 – CRES Characterization

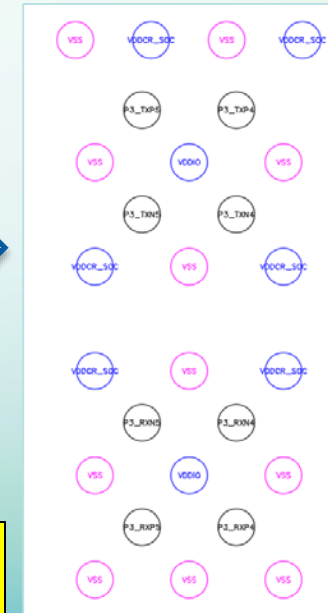
- CRES tests on bumped wafer at RT
  - Cleaning (XY=60): 5TDs @50um OT on 3M-3µm pink every 50TDs on wafer
- Summary results table

Subtech	CRES avg [Ohm]	CRES st.dev [Ohm]
Merlion 6a	0.31	0.09
Merlion 6b	0.32	0.07
Merlion 6c	0.38	0.08



Merlion 6 Test Fixture

- Validate the frequency performances in terms of S parameter and impedance matching of the Merlion 6 Probe Heads with simulations
- Customized test fixture designed to “sandwich” the Probe Head between 50-ohm impedance-controlled traces at each end to allow VNA interface
- Test PH with 27 Needles (8 RF Loopback and 19 GND Needles);
- Total of 16 2.92mm Connectors (8 Head side + 8 Tip side), to allow a 4 simultaneous ports measurement



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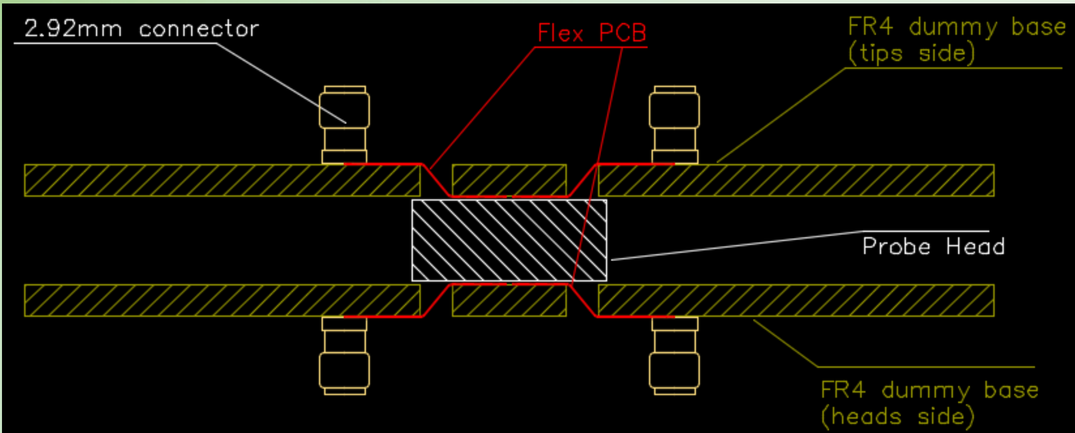
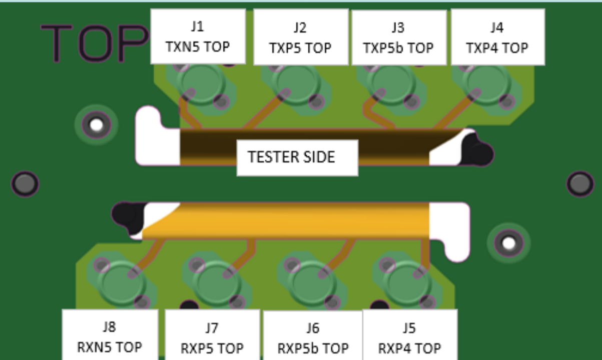
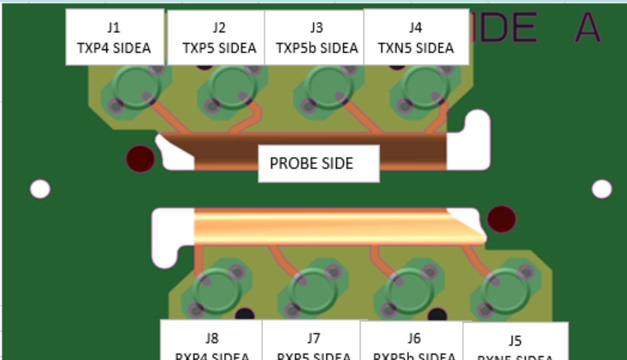
Test Fixture



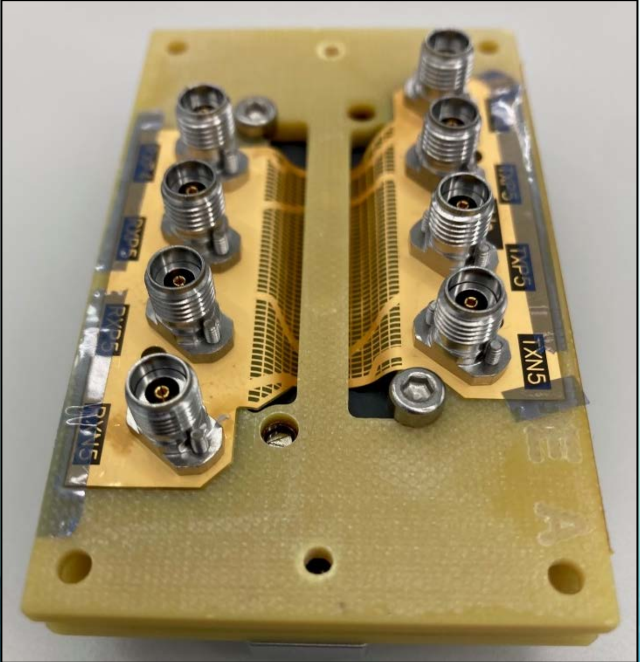
Needle Head Side



Needle Tip Side

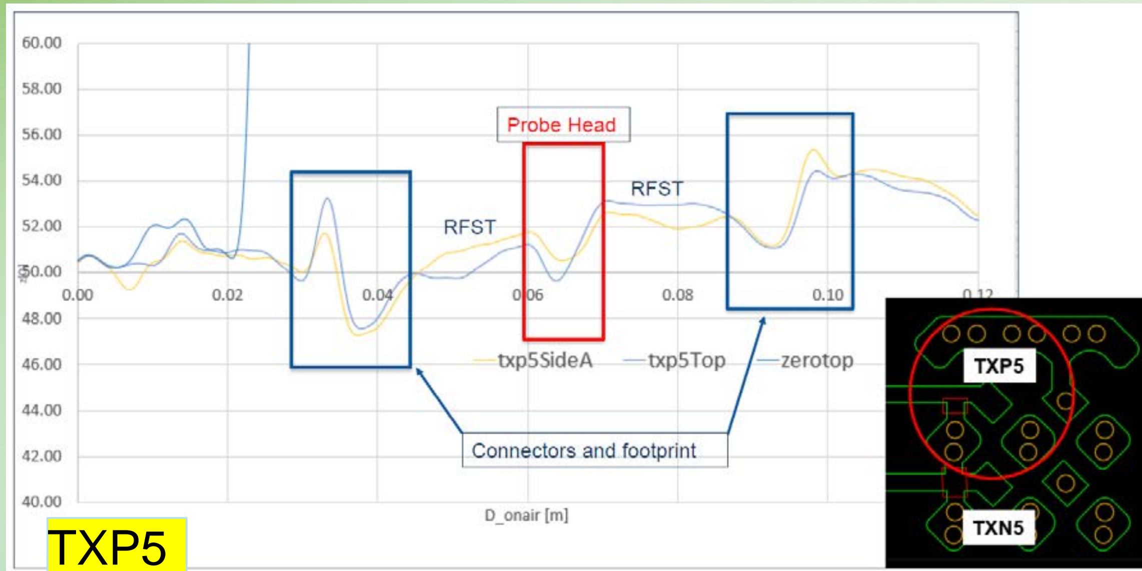


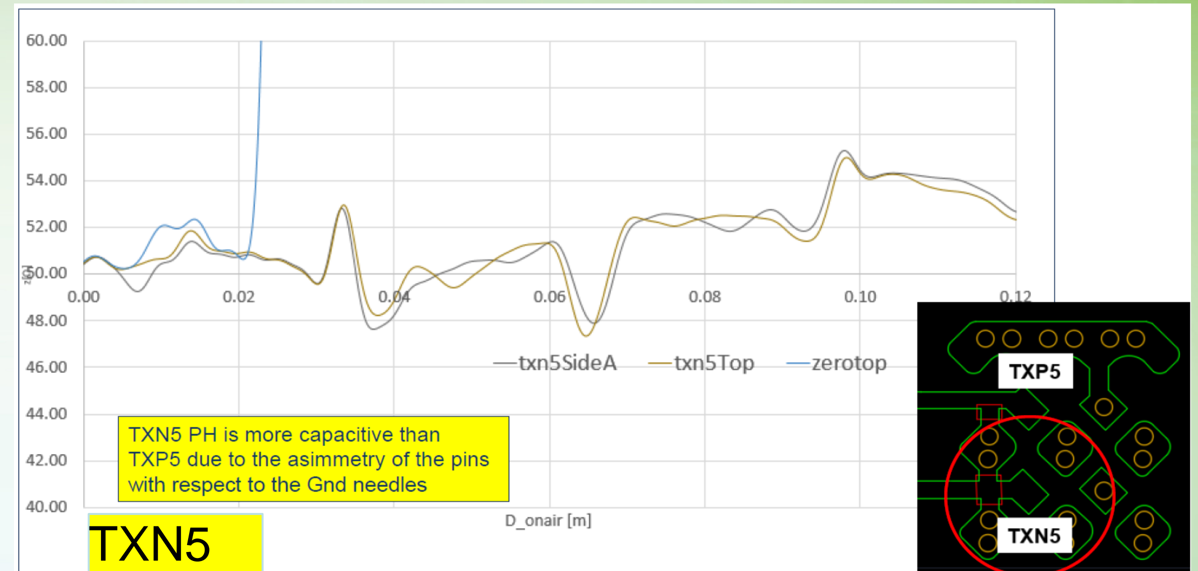
Needle Tip Side

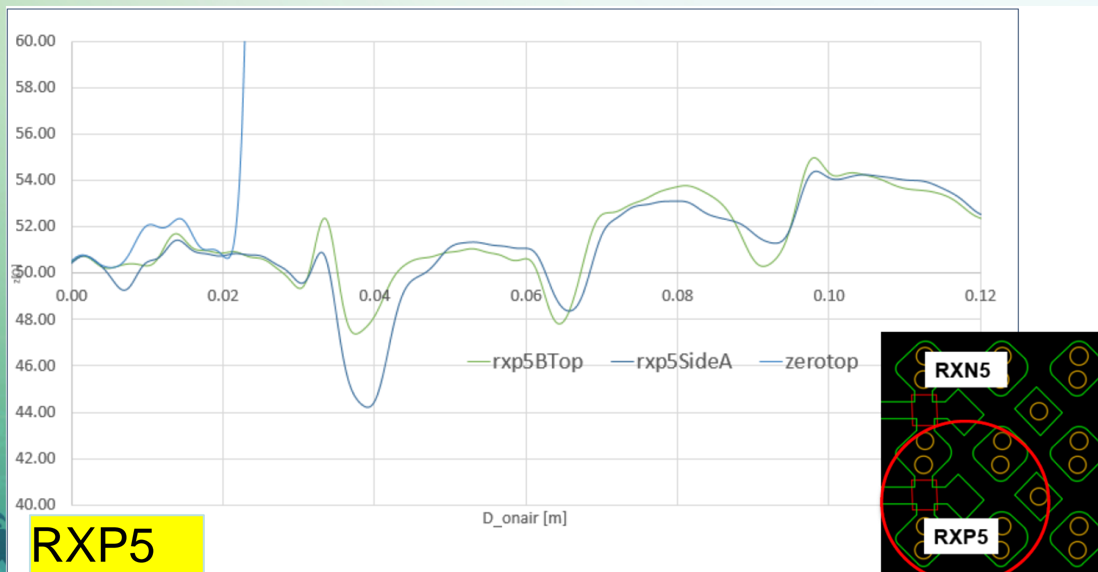


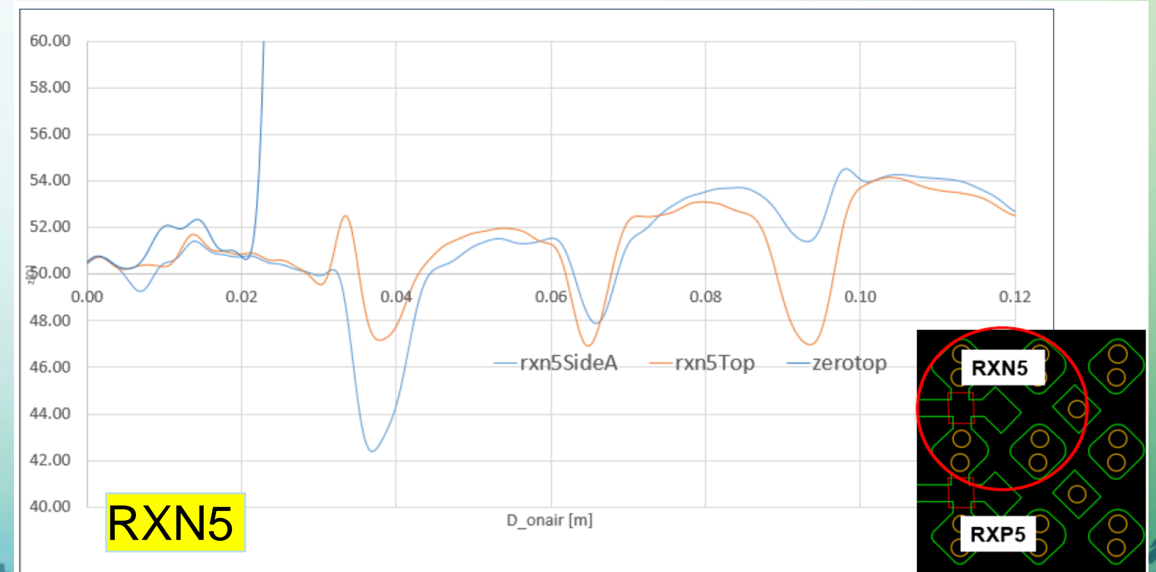
Needle Head Side

Test Fixture - SE TDR Measurement

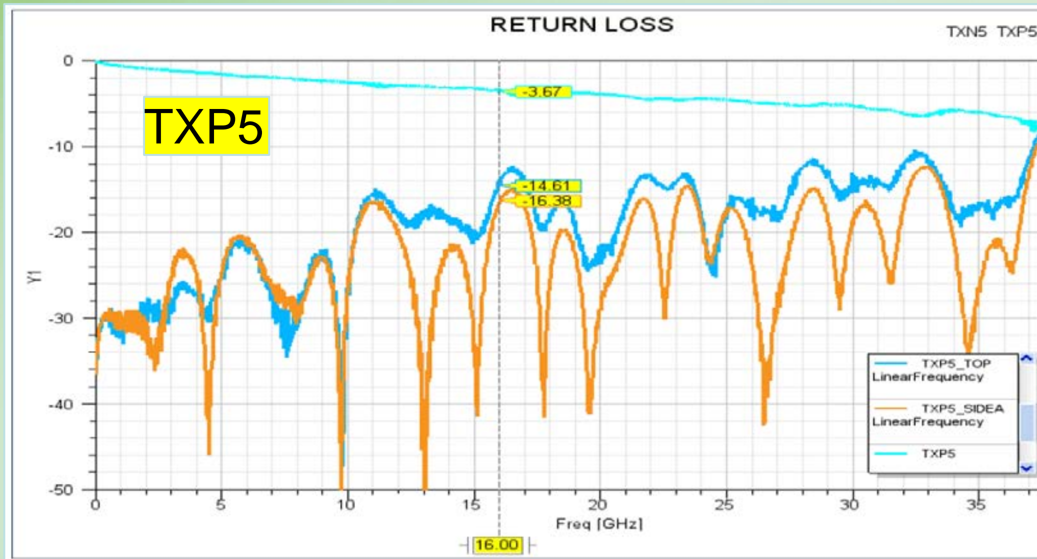


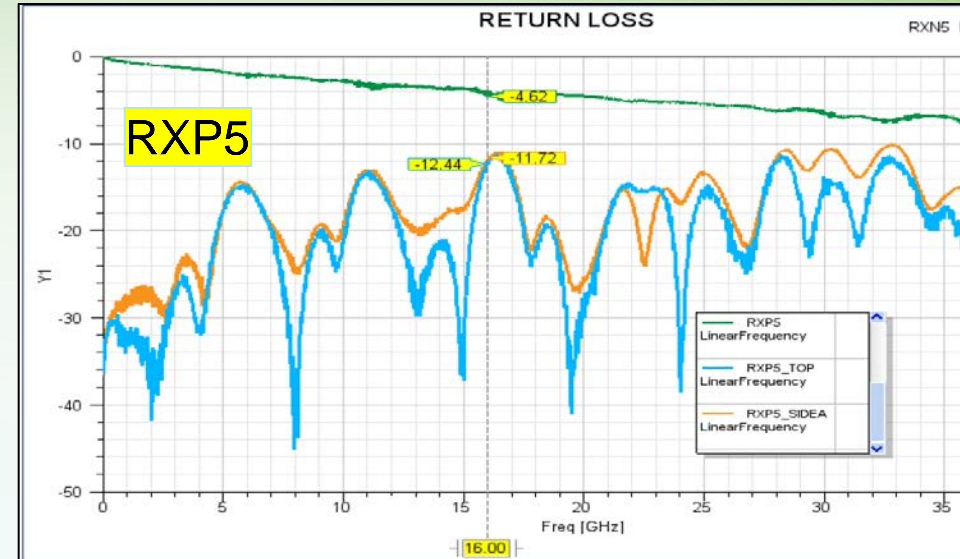


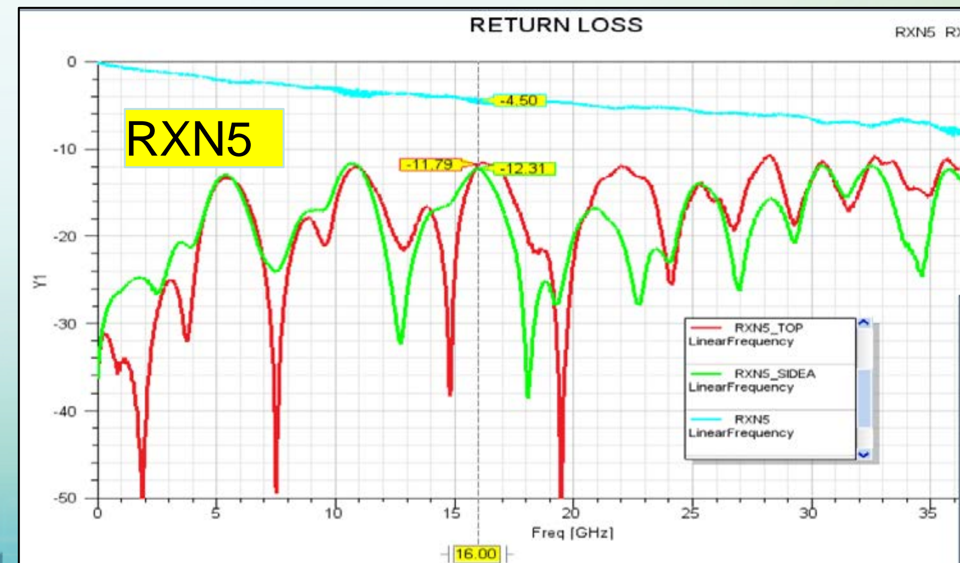




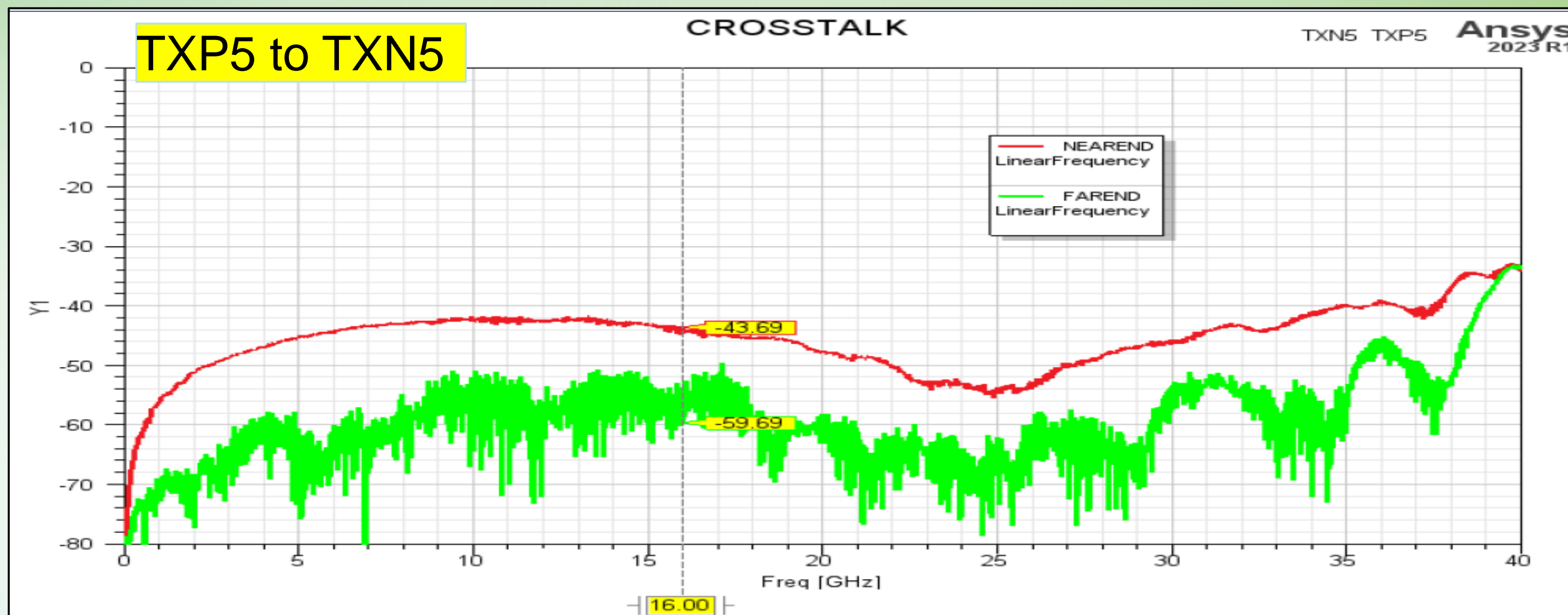
Test Fixture - SE S Parameters Measurement

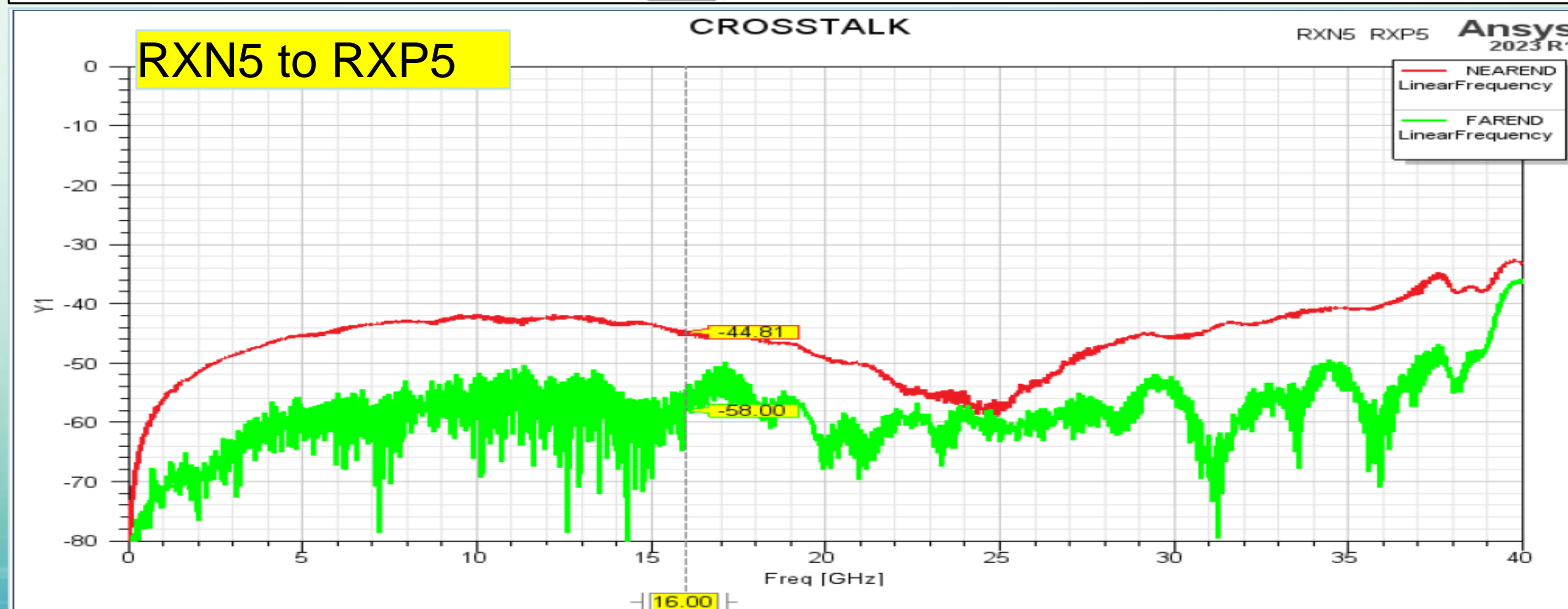




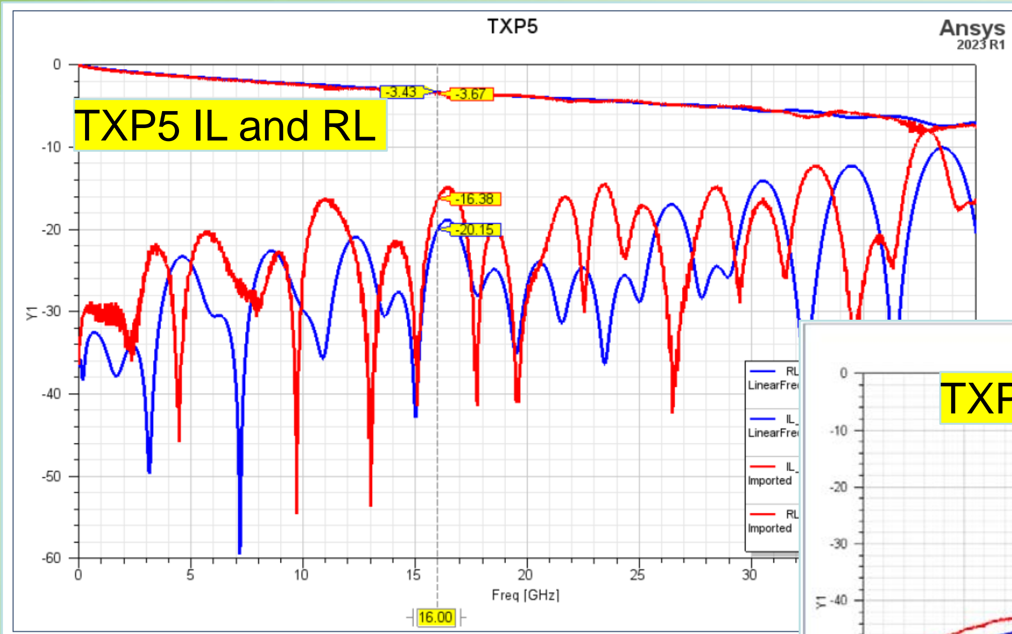


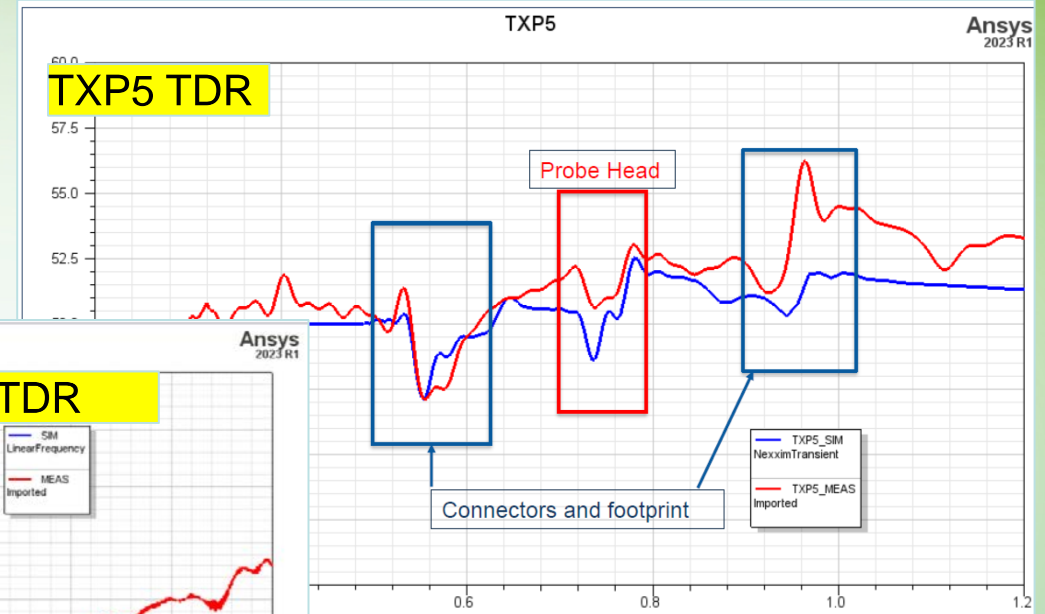
Test Fixture – SE Crosstalk Measurement

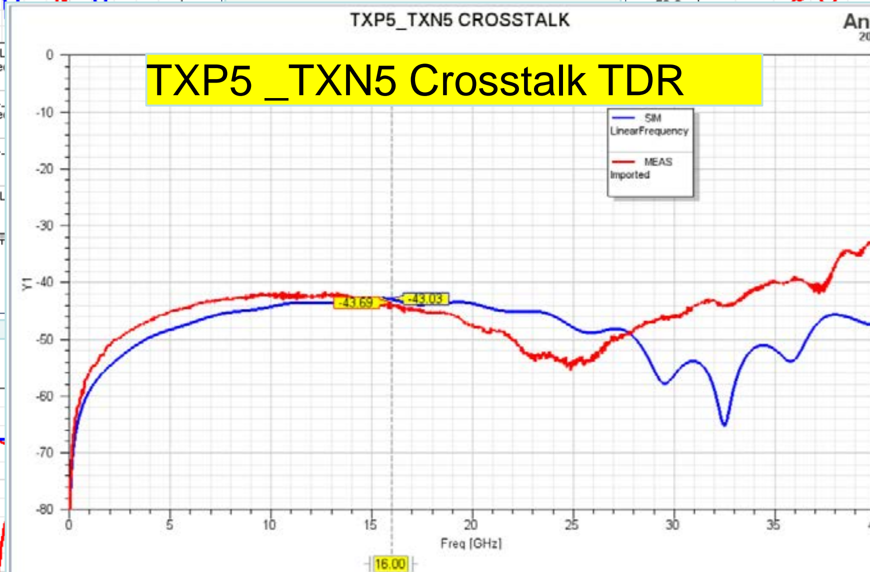


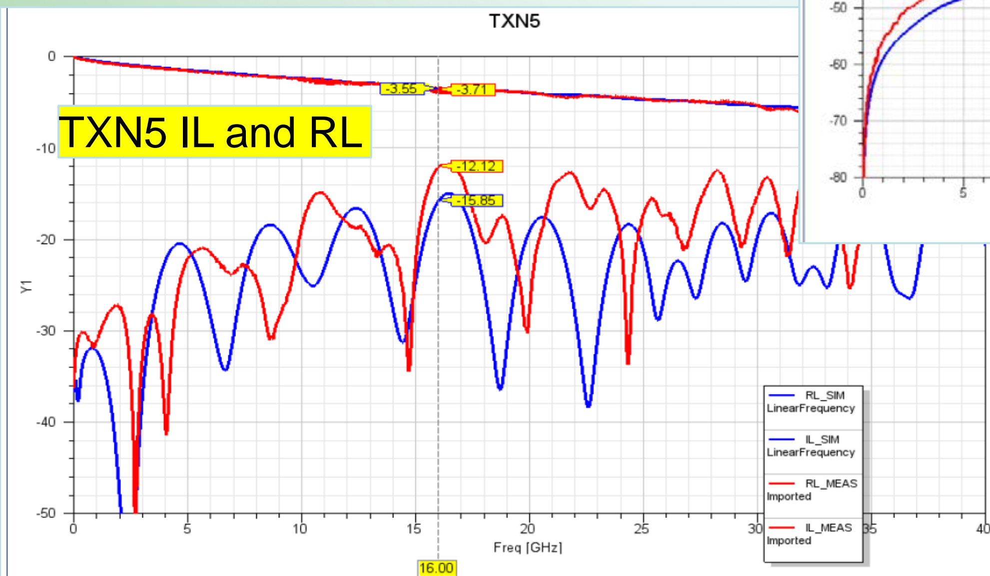


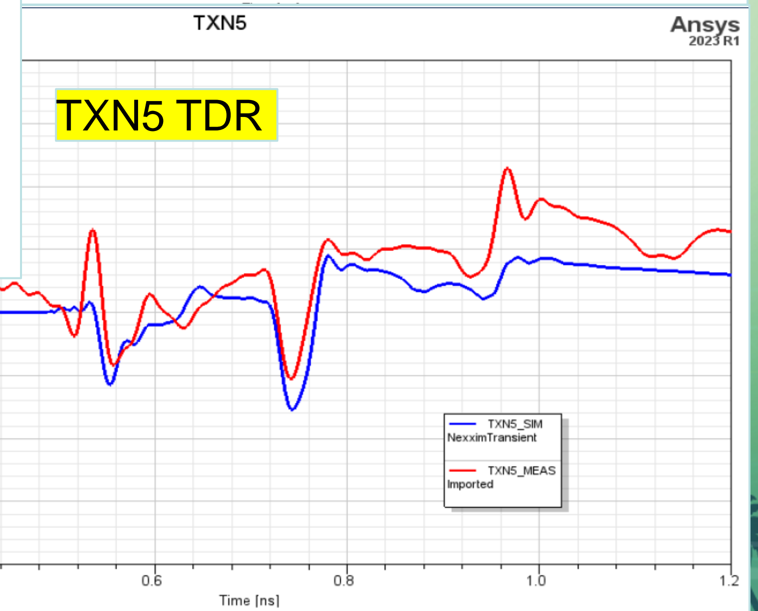
Test Fixture- SE S Parameters Simulation vs. Measurement



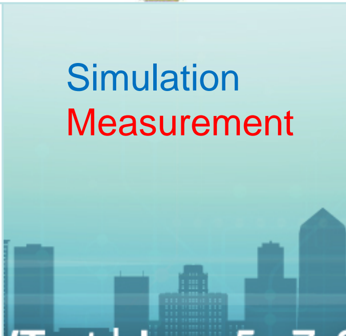




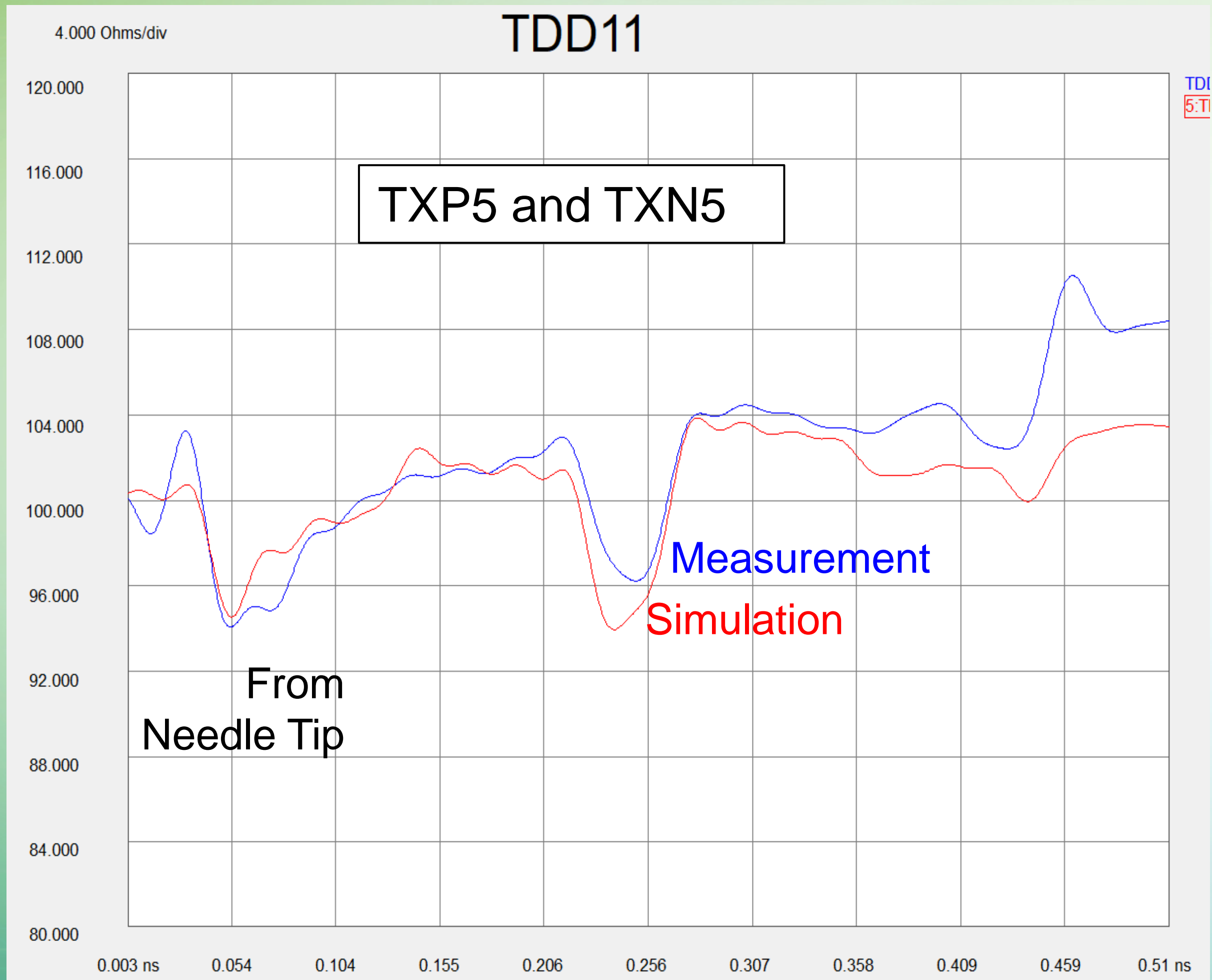


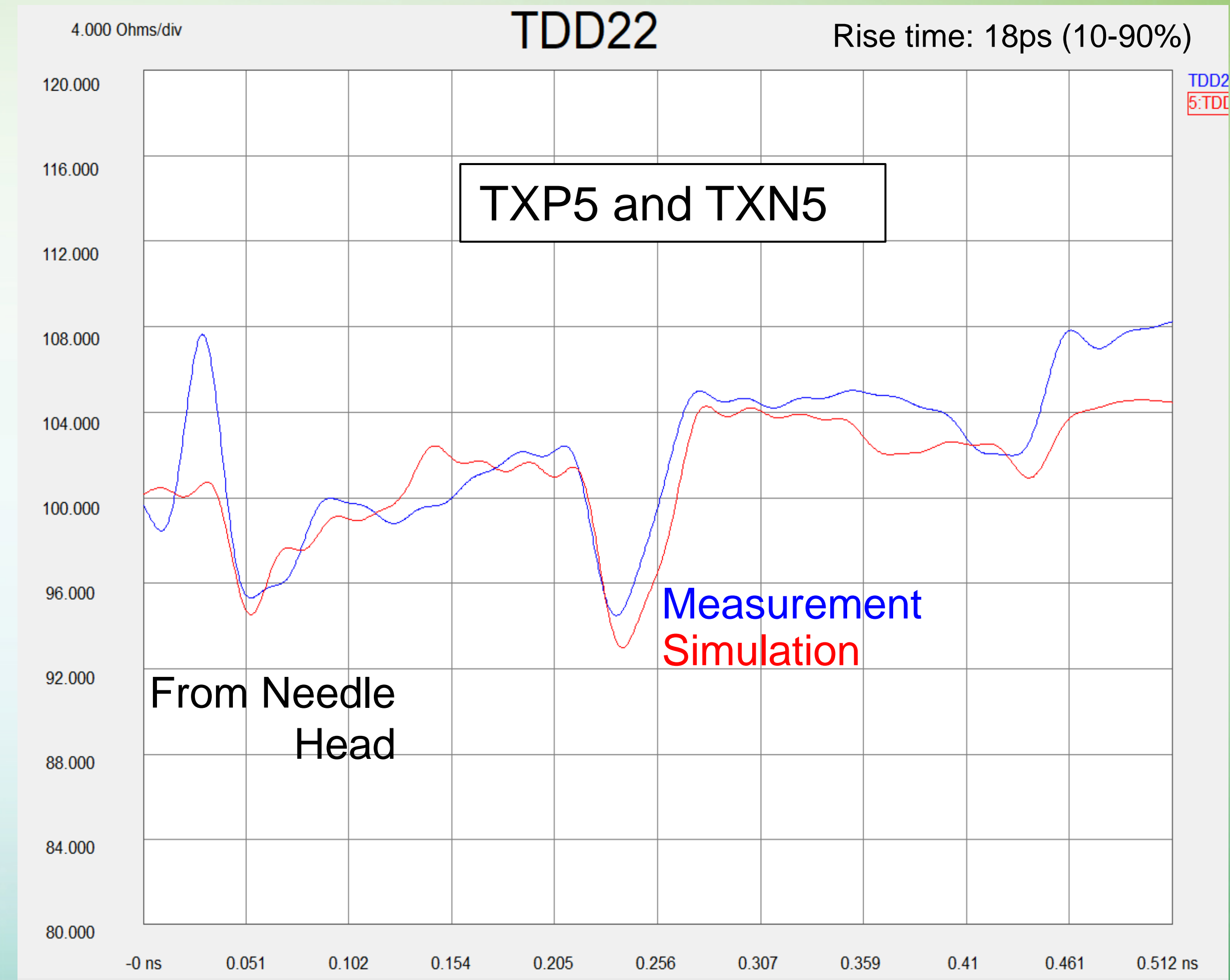


Simulation
Measurement

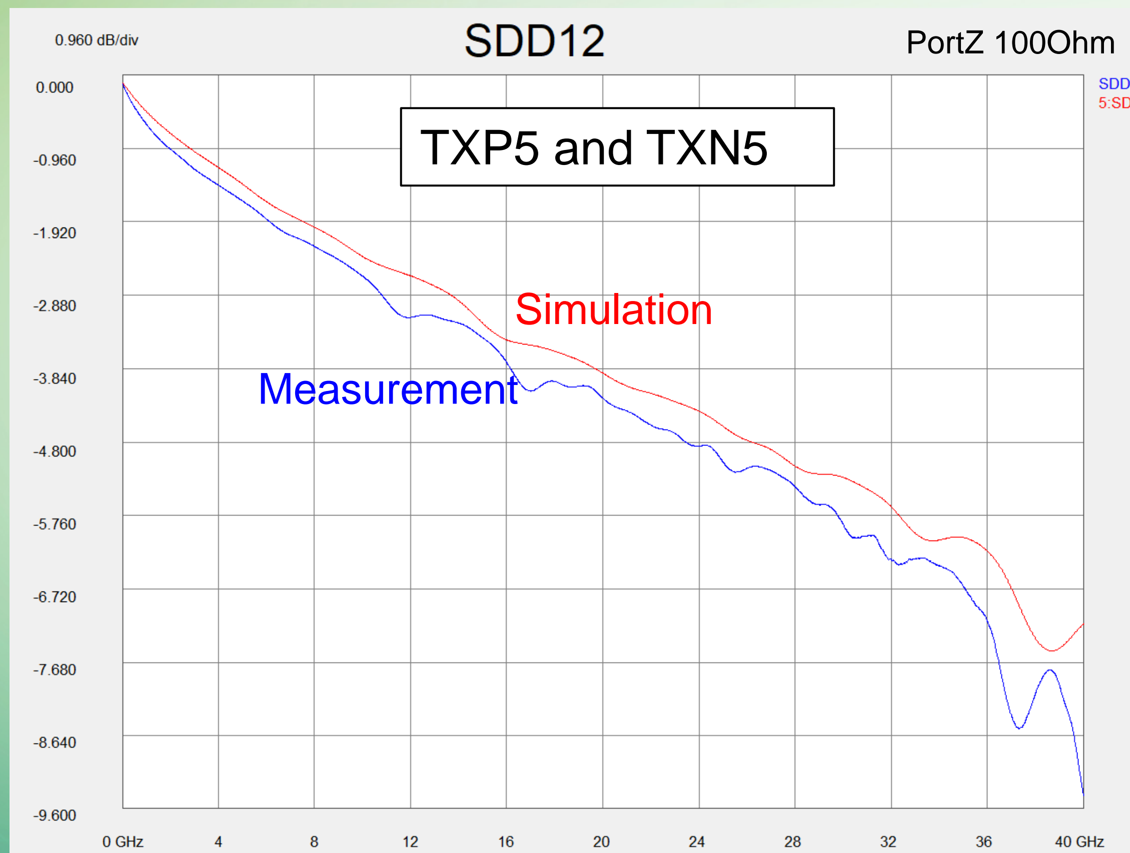


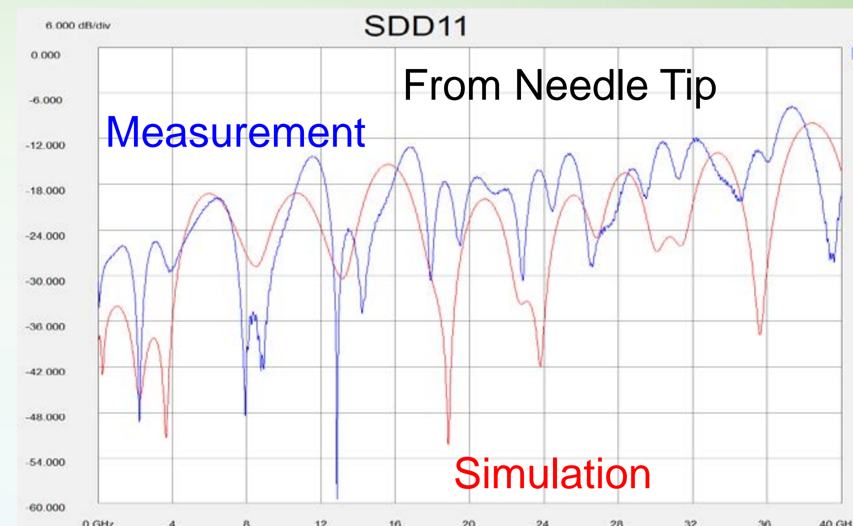
Test Fixture- DIFF TDR Simulation vs Measurement

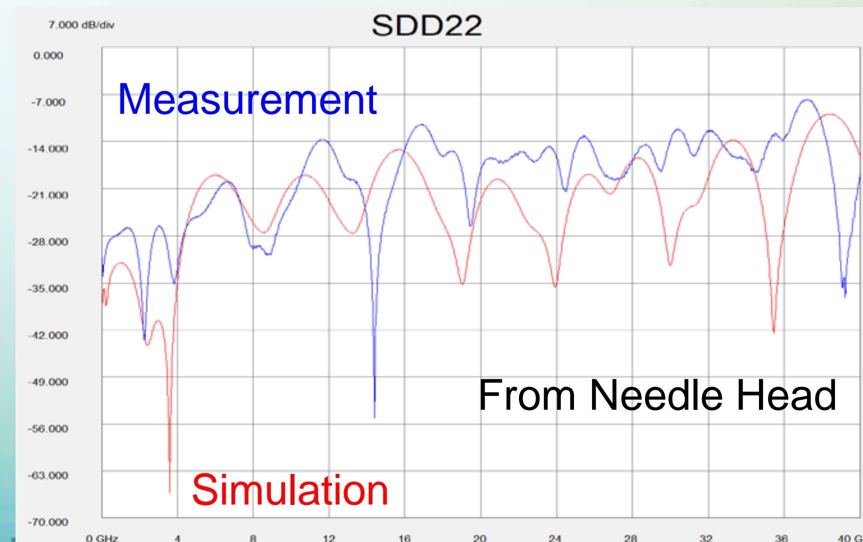




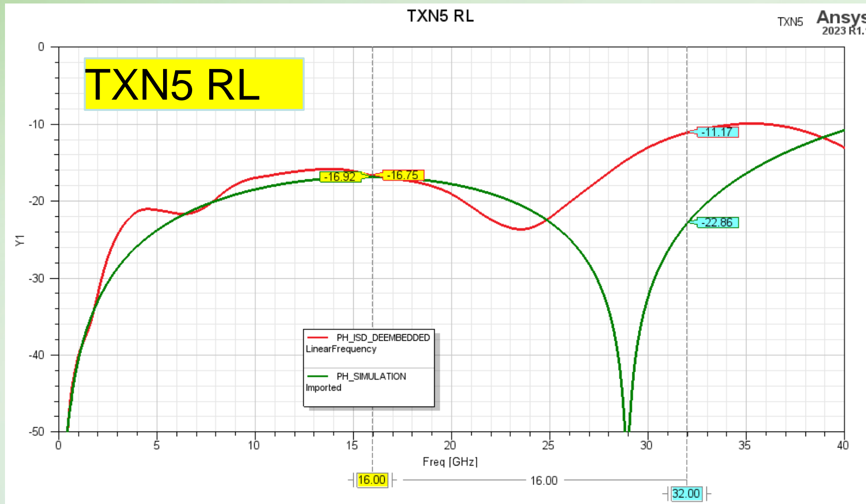
Test Fixture- DIFF S Parameters Simulation vs Measurement

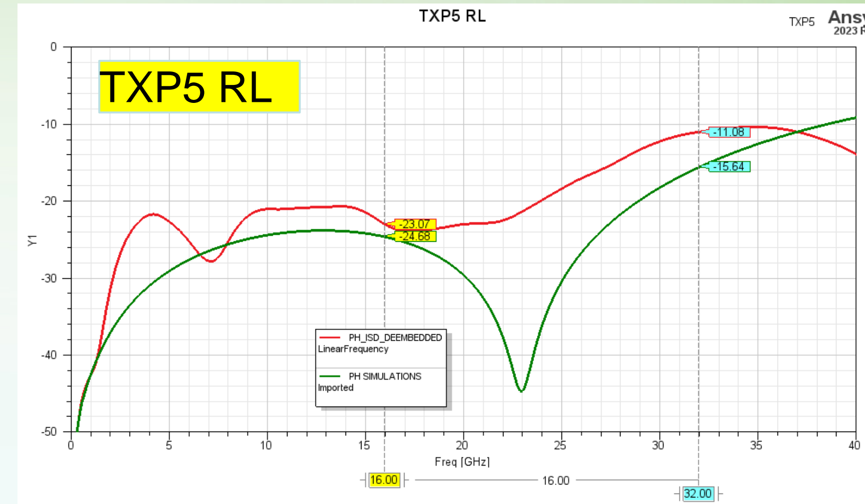


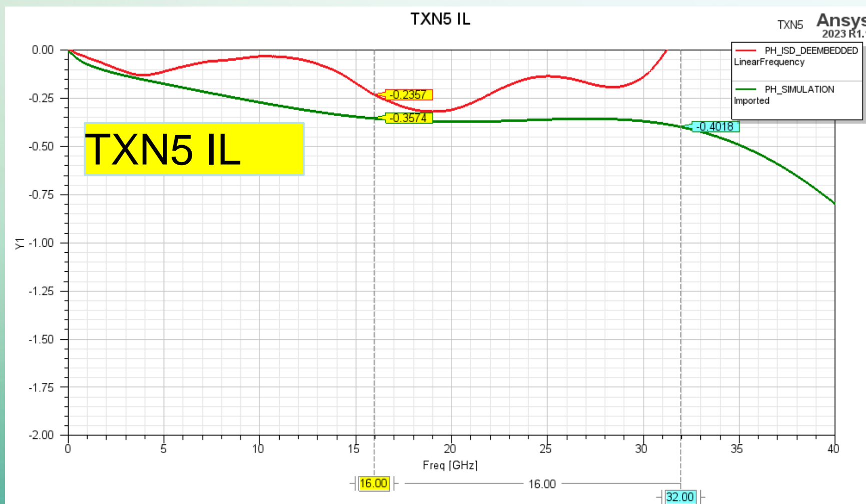


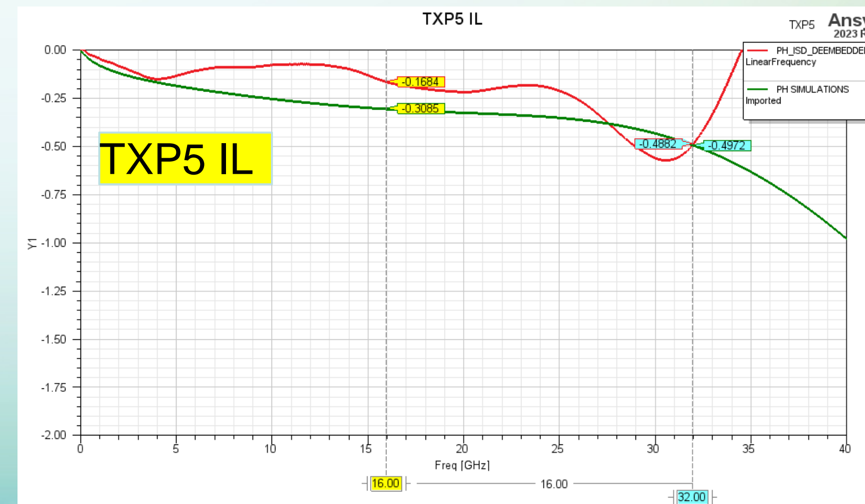


De-embedded Needle S Parameters Measurement vs Simulation









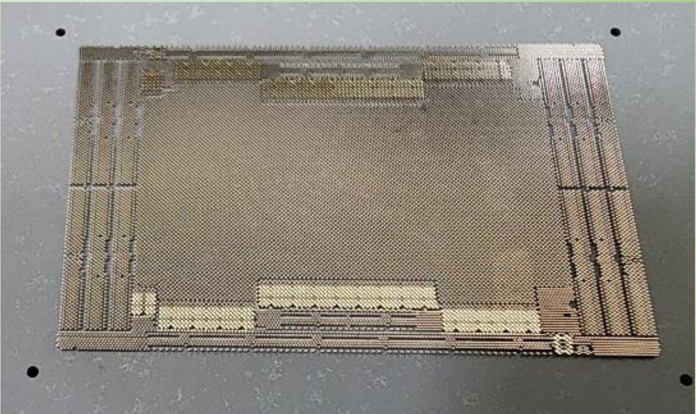
De-embedded Measurement

Simulation

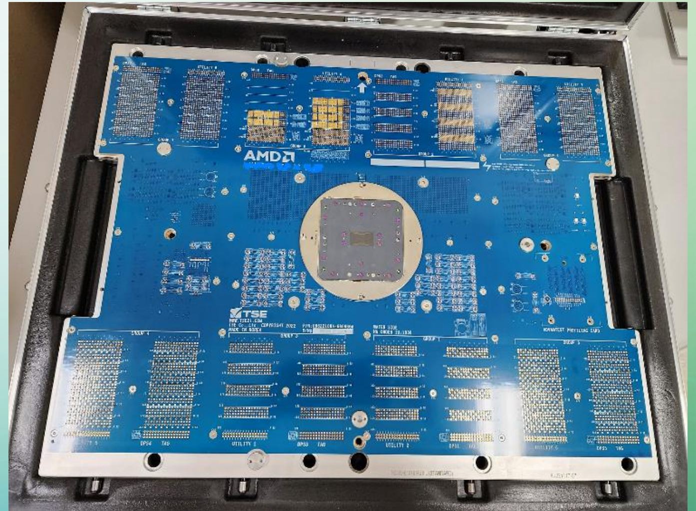
Test Fixture Measurement Conclusion

- Insertion loss and return loss show high degree of variability due to RF Space Transformer microstrip manufacturing tolerance, impedance mismatches between SMA connector to trace and mechanical assembly
- Single ended crosstalk simulation of probe needle matches the measurement
- TDR measurement shows good agreement in predicting probe head impedance profile
- De-embedding is performed on test points with best impedance profile. De-embedded S-parameters measurement shows good IL and RL correlation with simulation

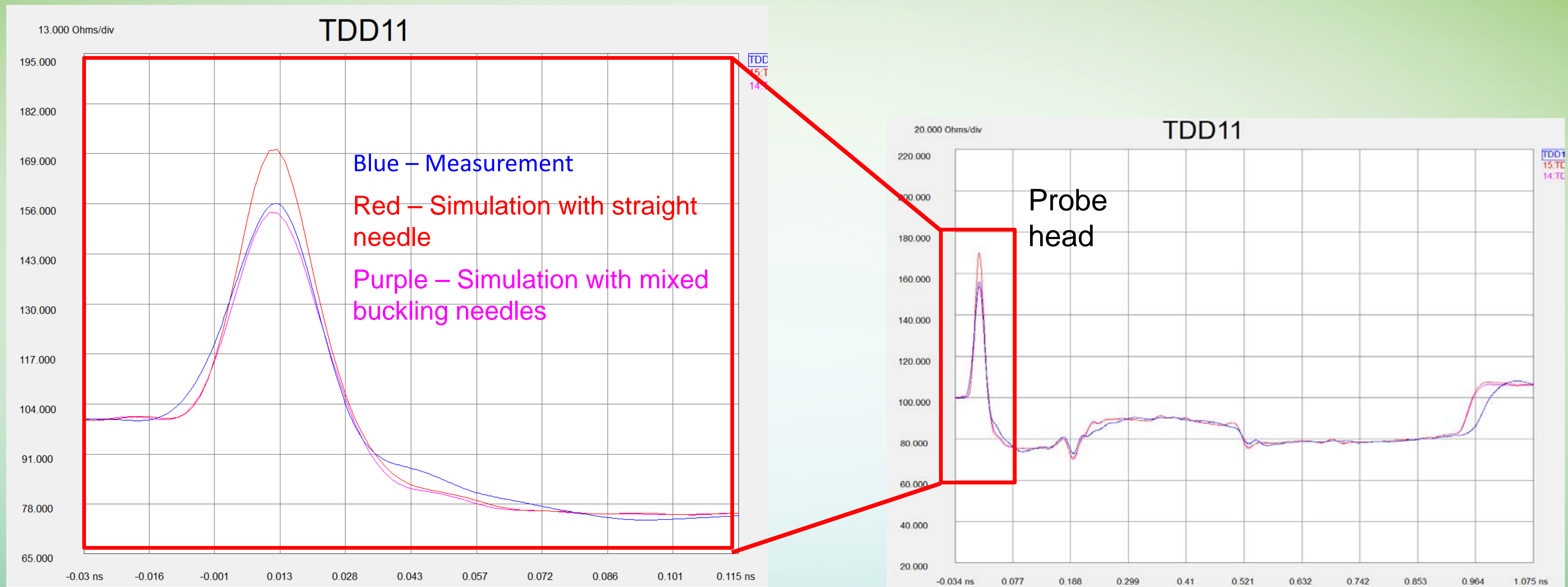
Probe card External Loopback End to End measurement



PCB + PCS+PH



End to End - DIFF TDR Simulation vs Measurement



- Microprobing VNA measurement directly on probe needle tip is not recommended
- Without proper connection on all probe GND on the tip side, the return current is forced through only the microprobe GND pin thus causing higher loop inductance and hence higher measured impedance

Conclusion

- Merlion 6 hybrid probe solution not only can meet the AMD high-speed test requirement and provide high current carrying capacity for test
- Probe solution also provided low and stable CRES with high strength & conductivity
- HiP (High Power PH) architecture minimize probe burnt and maximize MTBF in production
- Simulation (TDR measurement) shows good agreement in predicting probe head impedance profile
- De-embedded S-parameters measurement shows good IL and RL correlation with simulation

Special Thanks

- Ng Hui Ying – Sr Packaging Engineer at AMD
- Ivan Giudiceandrea - Product & Design Development Engineer at Technoprobe

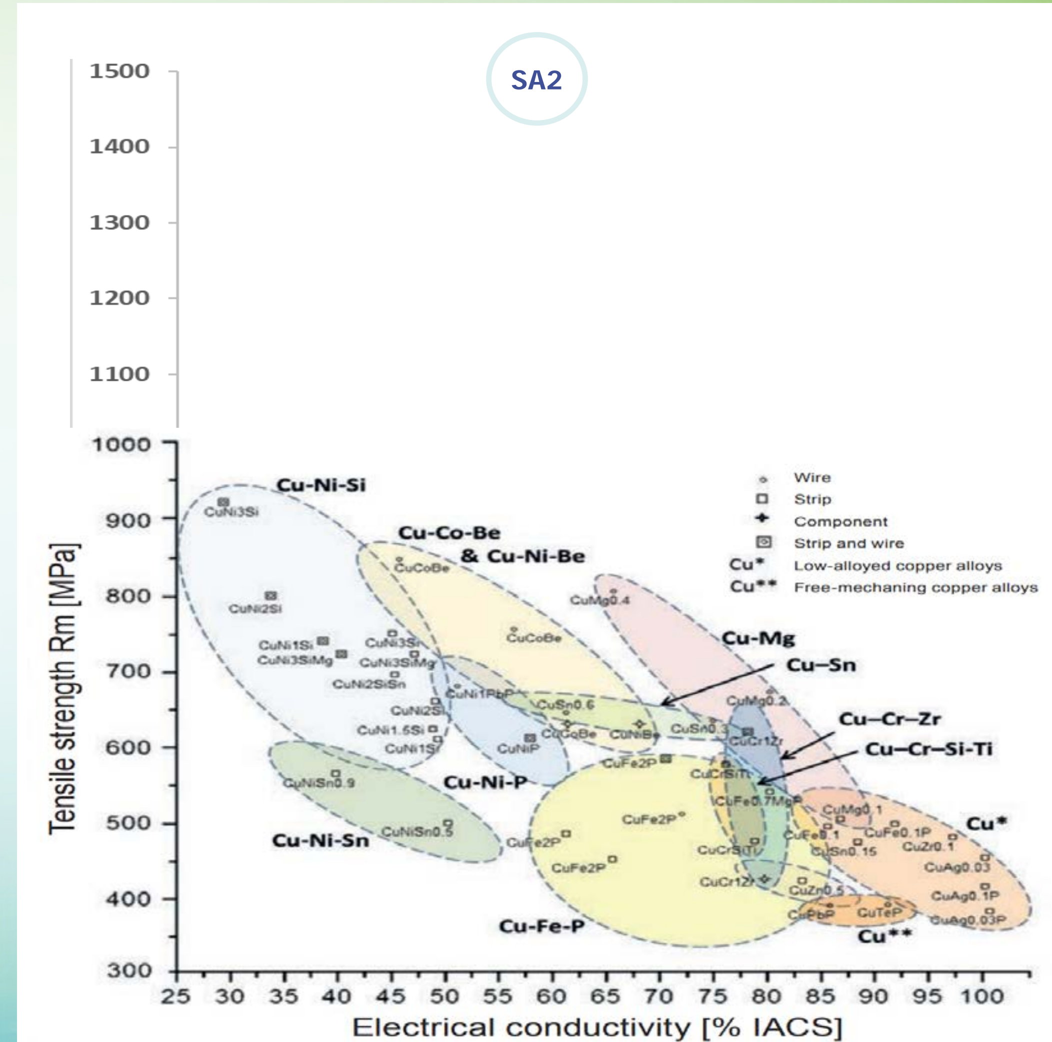
Back Up

SA2 Probe Alloy

- Materials development is continuous to support arising challenging probing applications

- Key parameters are
  - Maximize Electrical Conductivity
  - Maximize Strength (Yield strength/hardness)
  - Minimize Electrical Contact Resistance (CRES)
  - Maximize High temperature stability of mechanical performances

- SAx alloys internally developed with unprecedented performances
  - High strength & conductivity
  - Low and stable CRES
  - Stress relaxation at high T



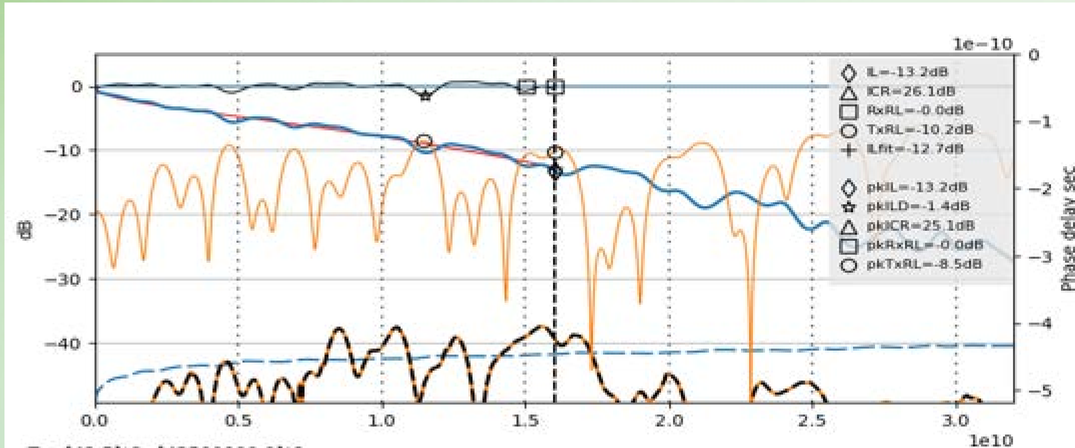
HiP PH Architecture – Key Values

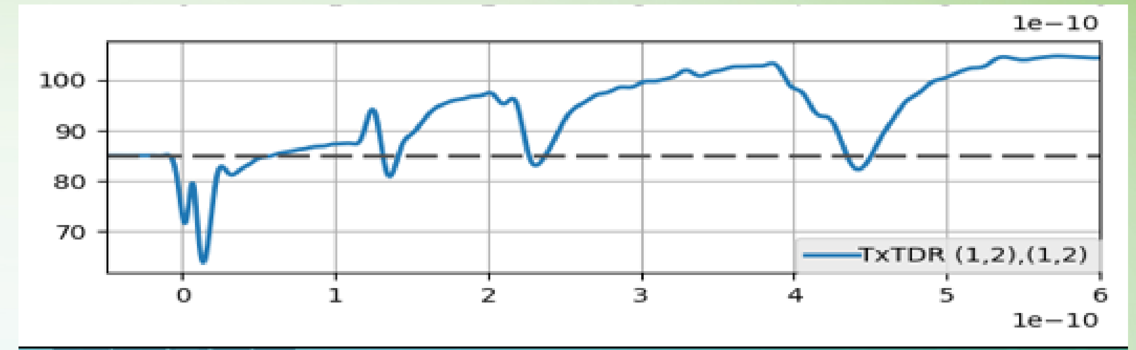
HiP, combined with High Current Probes and Hybrid configuration is today the state-of-the art in PCs technology, widely adopted by any top-tier semiconductor Company.

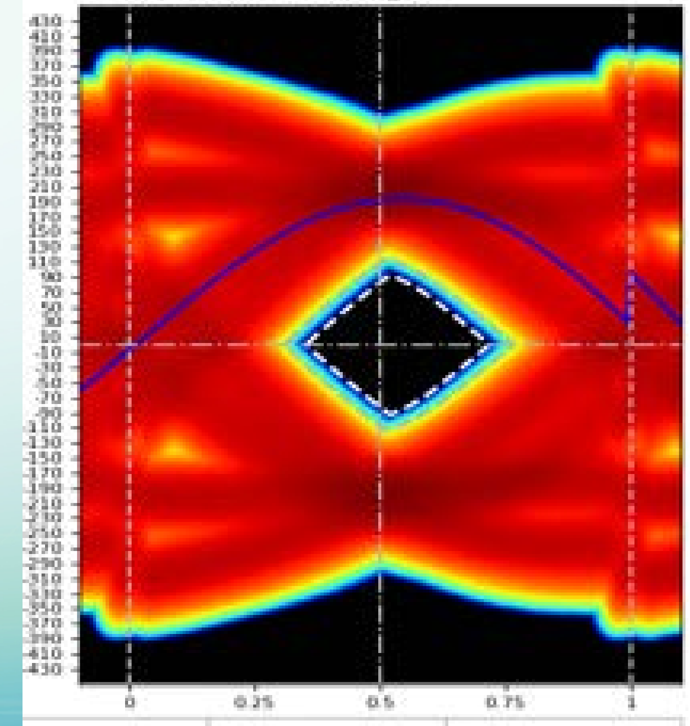
Lithographic process (semicon-like)

High layout complexity:
high holes density of several power planes can be routed in same layers or multiple layers

Probe Card Channel Simulation







- **Merlion 6 channel simulation data, S-parameters, TDR and Crosstalk**

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