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PROBE TODAY, FOR TOMORROW

2023 CONFERENCE

Maximizing CCC and the March to an Unburnable Probe

FormFactor™

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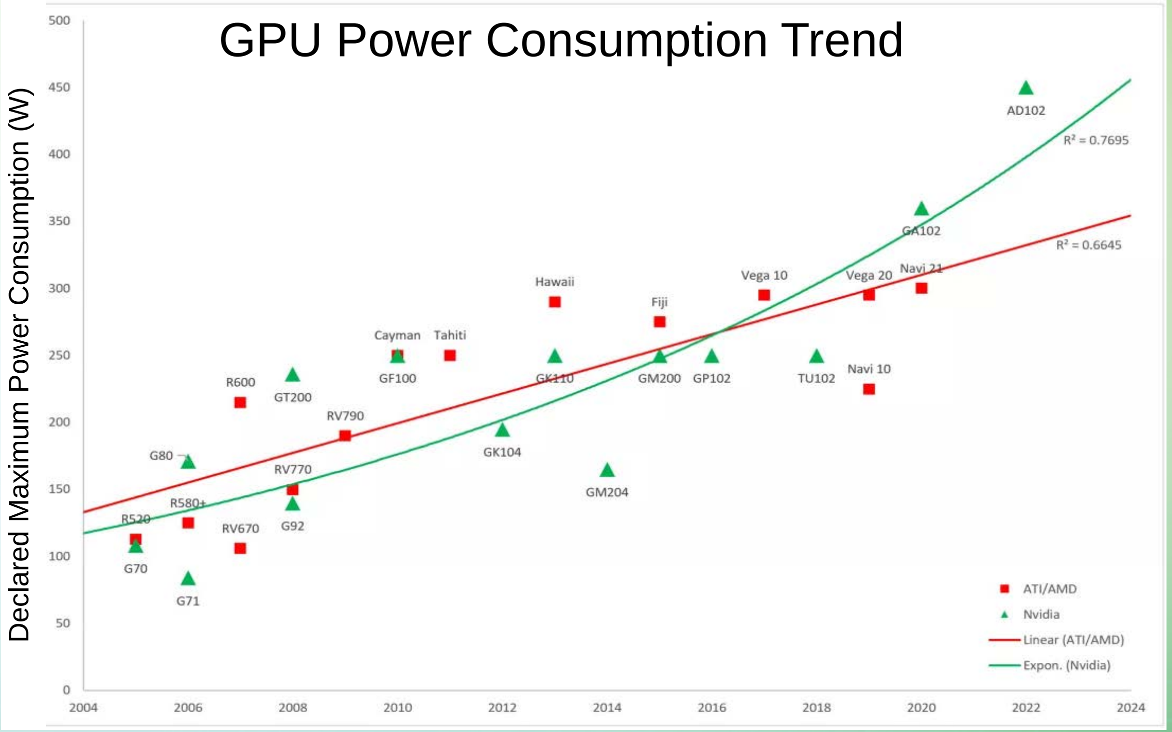
Agenda

- Why Does CCC matter?
- Hybrid Probe Review
- Next Generation Probe Review
- Metallized Guide Plate Review
- Maximized CCC Conclusion

Industry Trends

- High Performance Compute and GPU applications are marching to 1kW devices (1,000A at 1V)
  - Shipping 400A devices today (400W at 1V)
  - Newest HPC devices have >50 Billion Transistors
- New nodes and technology advancements are creating downward pressure on yield
  - Yield drop with each node transition
  - Transitions to more complex digital coms (PAM4) decrease yield
  - Larger die for HPC and GPU applications are lowering wafer yield
- As yields decrease and as device power increases Probe Card capability and CCC must increase



https://www.techspot.com/article/2540-rise-of-power/

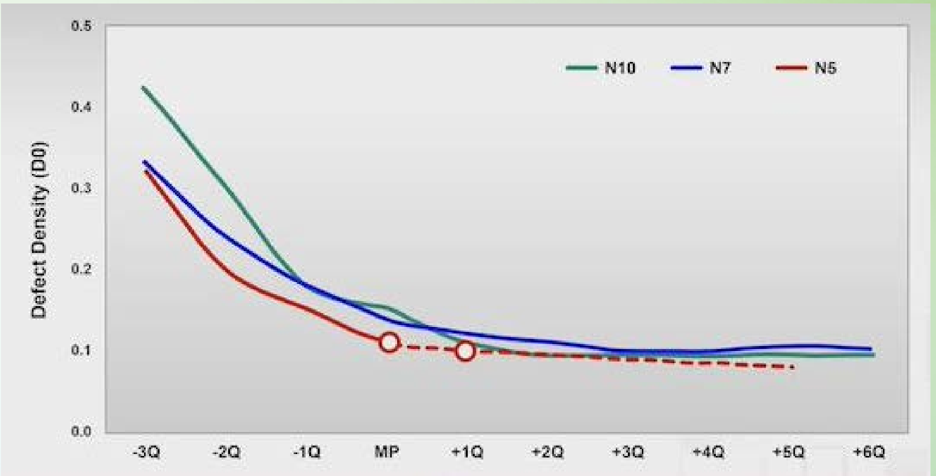
CCC Terminology

- Current Carrying Capability
  - The amount of current that a probe or spring can withstand before burning or damage occurs
- ISMI CCC
  - Current applied where a 20% lower force is observed in a probe (spring)
- MAC (Maximum Allowable Current)
  - Current applied where a change in probe force or planarity is first observed
- ECCC (Effective Current Carrying Capability)
  - An averaging of total current that a group of probes can withstand before burning occurs

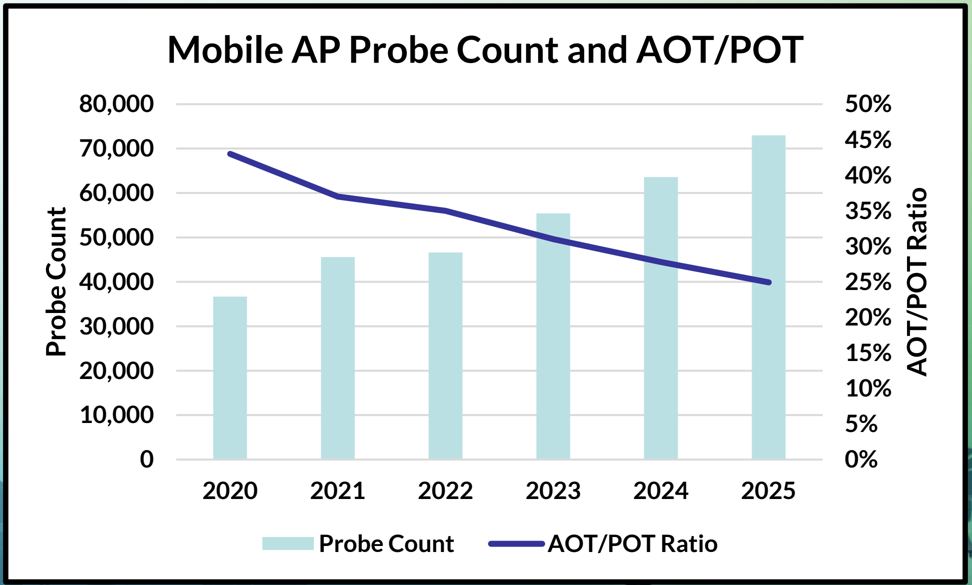
Why Does CCC Matter?

- Probe Current Carrying Capability prevents probe burning when something goes wrong during wafer testing
  - Shorts in the DUT
  - Unstable contact between the DUT and Probe card
- High CCC Probes improves uptime and MTBF as the probe card becomes more robust and resistant to probe burning

Defect Density over Time by Node

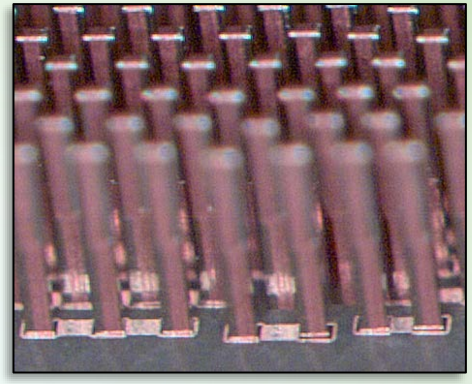


https://www.anandtech.com/show/16028/better-yield-on-5nm-than-7nm-tsmc-update-on-defect-rates-for-n5

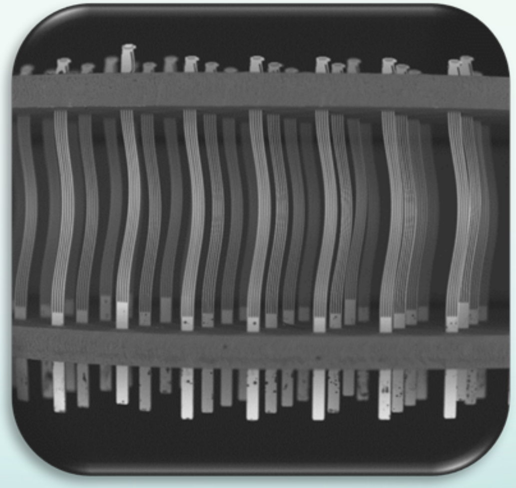


Methods for Improving CCC

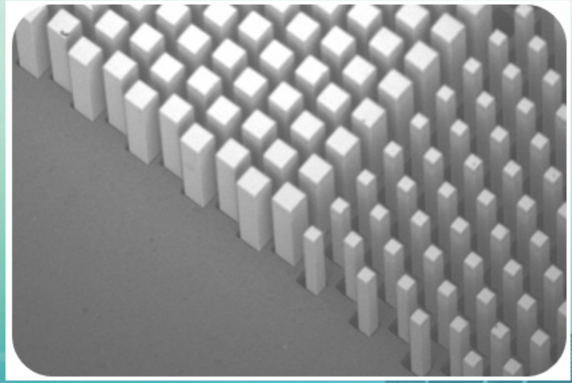
Metallized Guide Plates



Next Generation Probes



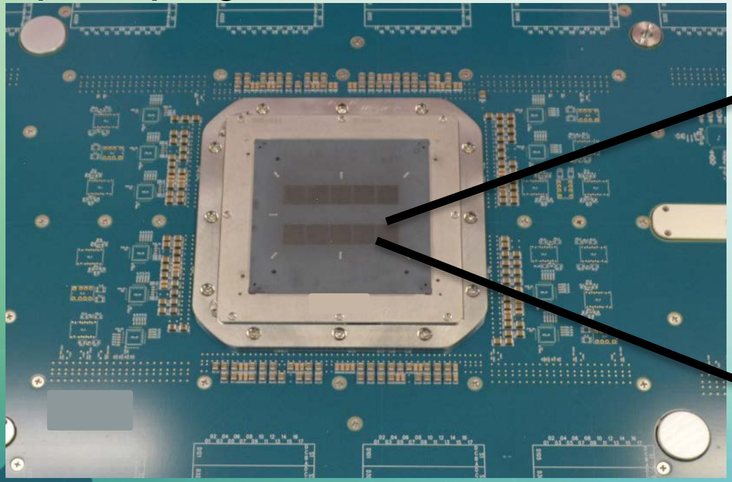
Hybrid Probes



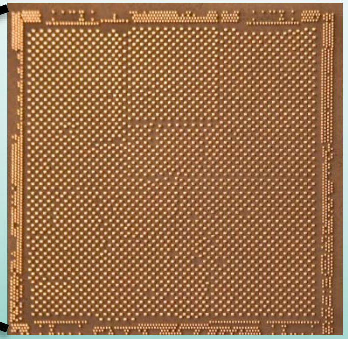
Hybrid Architecture

- SOCs have PWR/GND in the middle of the Device and I/O in the periphery of the Device
  - PWR/GND typically at ≥150um pitch
    - Can use wider, high CCC probes
  - I/O typically at ≤90um pitch
    - Can use smaller, lower CCC probes
- By combining probe types in the Probe Card the Effective CCC is increased

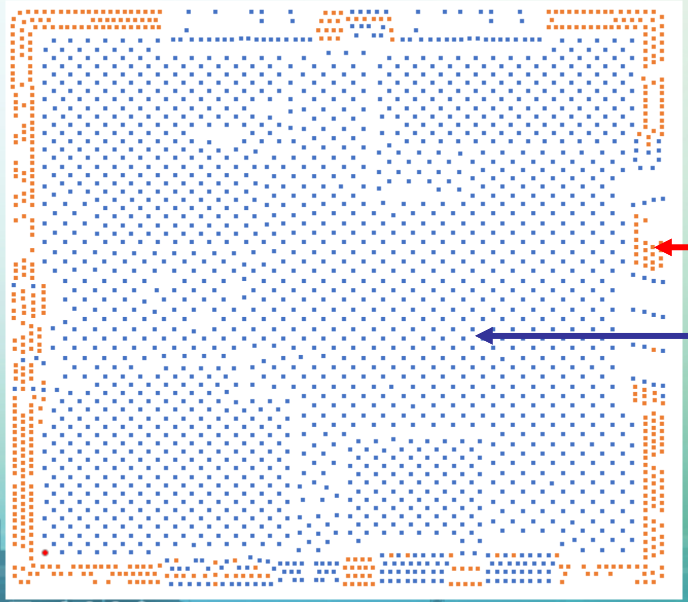
Hybrid Spring Head Probe Card – V93K DD



DUT Zoomed In



Single DUT Layout by Probe Type



Tighter Pitch Probes with lower CCC

Wider Pitch Probes with Higher CCC

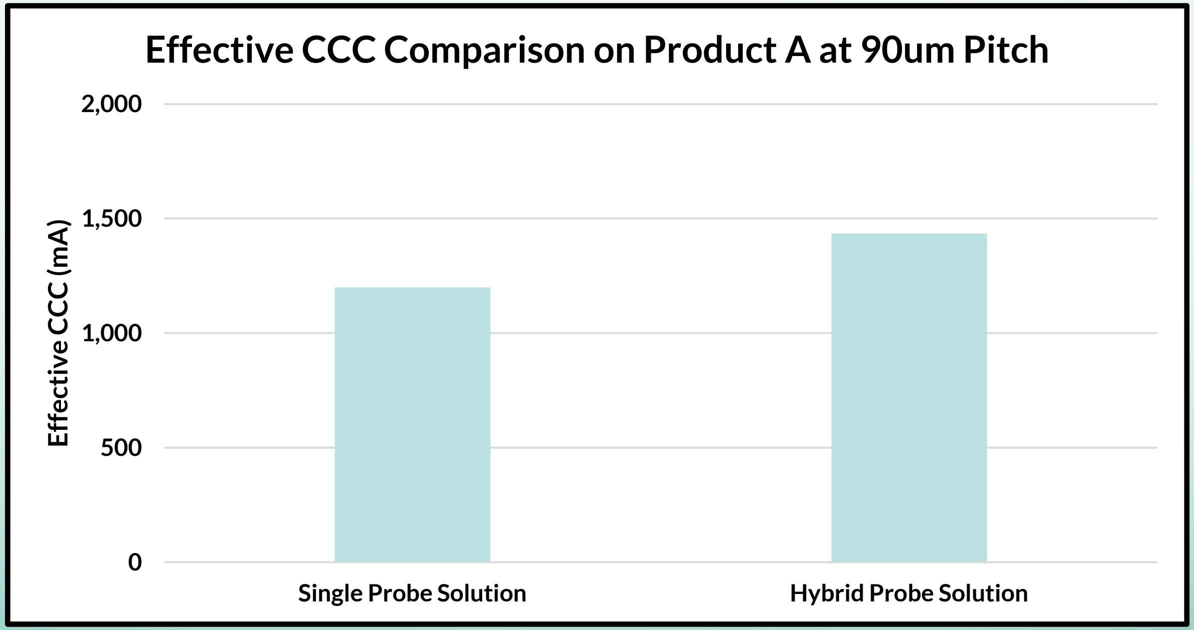
Hybrid Increasing Available CCC

- FFI Hybrid probe technology increases probe card available CCC
  - combining tight pitch low CCC probes and wide pitch High CCC probes in the same design
- Product A as a test case
  - Min Pitch = 90um
  - Requires MF100F for 90um pitch with CCC of 1,200 mA
  - If hybrid is used available CCC can be improved by 20% to 1,435 when using MF130/MF100

Product A x8 Hybrid Available CCC Example		
Hybrid Probe Type	MF100F	MF130F
CCC (mA)	1,200	1,500
Probe Count	4,216	15,248
Total CCC (mA)	5,059,200	22,872,000
Total Probe Card Available CCC (mA)	1,435	
% Improvement over Single Probe (MF100)	20%	

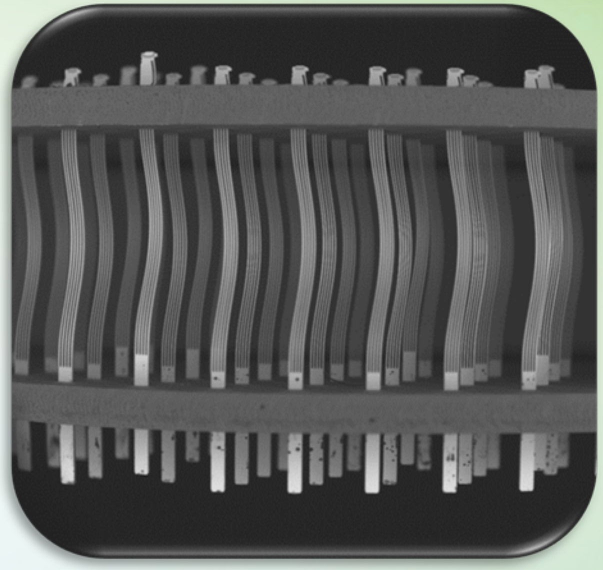
Maximizing Effective CCC

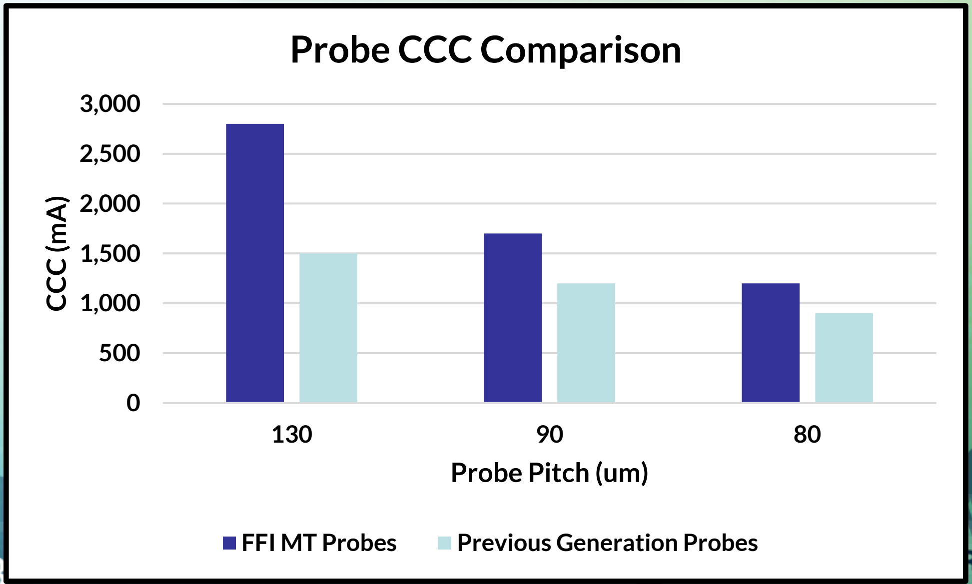
- Hybrid probes provide 20% higher effective CCC relative to single probe solutions



FFI MT Probe

- MT next generation probes provide >50% improved CCC over current gen. MEMS probes
- Higher speed performance with shorter probe length.
- Hybrid compatible MT probe family to further enhance CCC and high-speed capability.
- Metallized Guide Plate can further increase effective CCC to >3A





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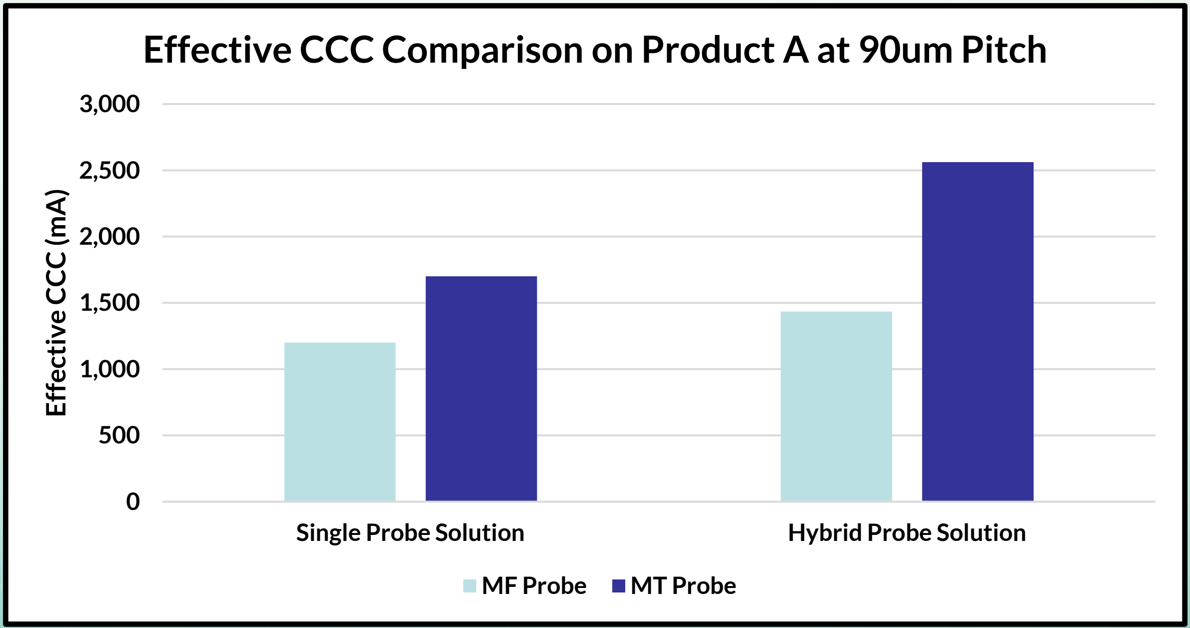
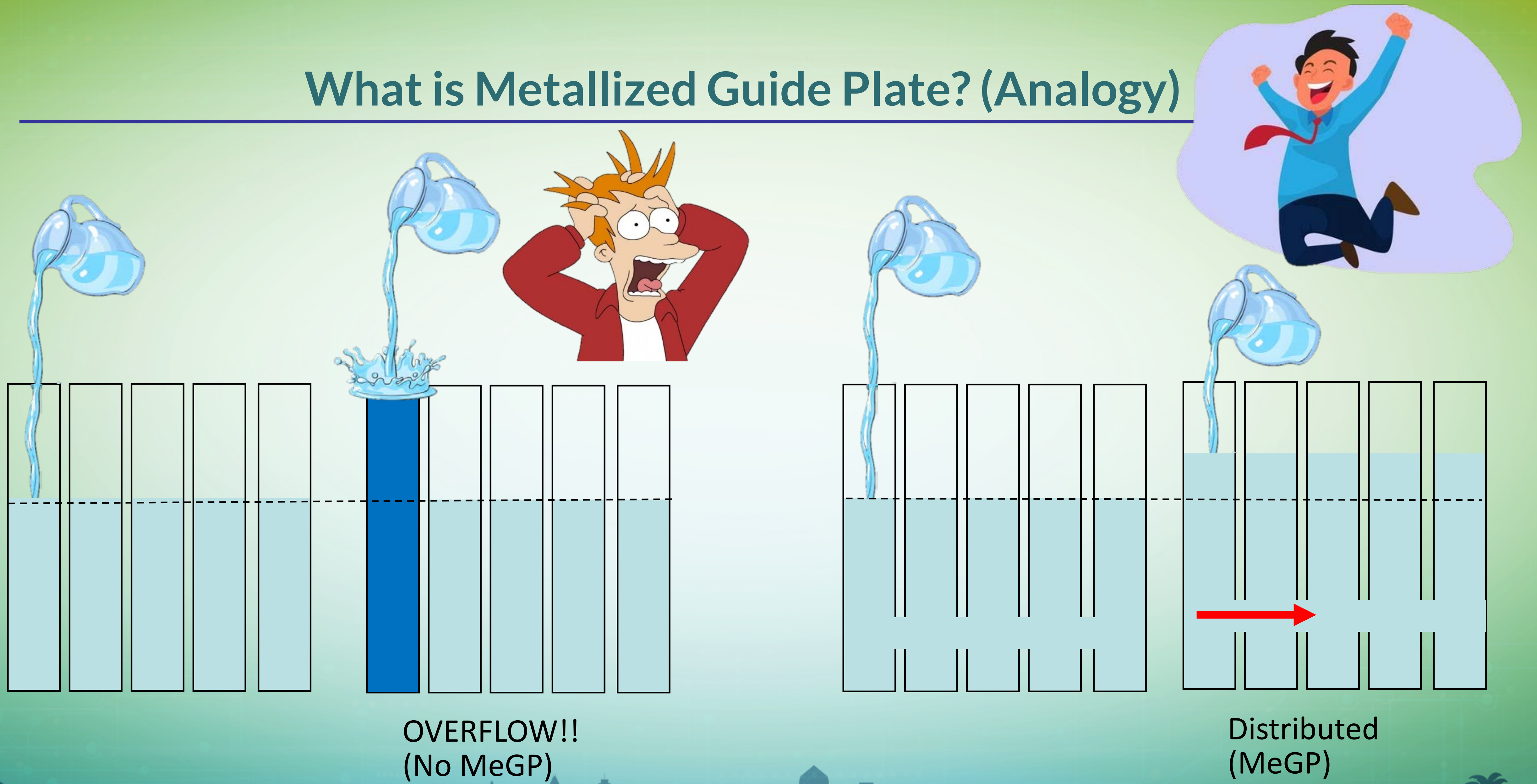
Maximizing Effective CCC

- Hybrid probes provide 20% higher effective CCC relative to single probe solutions
- MT Probes provide 42% higher CCC relative to last generation probes
  - 78% improvement when combined with Hybrid



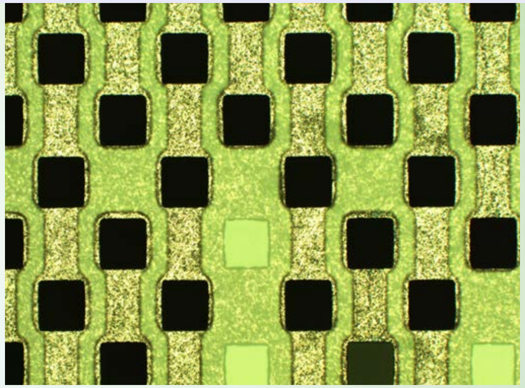
What is Metallized Guide Plate? (Analogy)



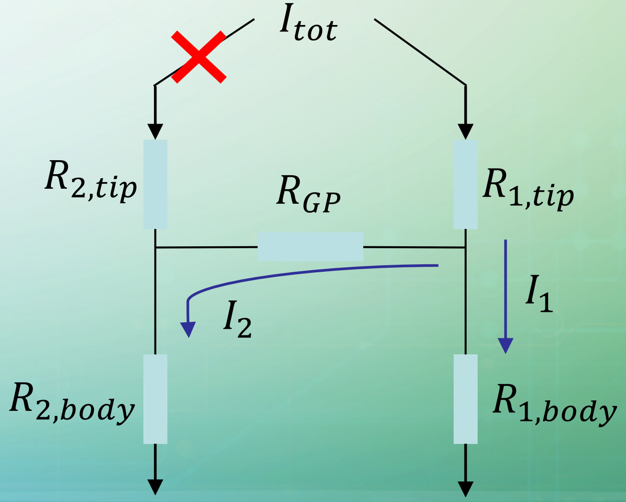
What is Metallized Guide Plate?

- Metallized Guide Plates (MeGP) connect VDD and GND nets together through metal patterns on the Guide Plate
  - Provides alternative current path when overcurrent events occur
  - Enables Improved Contact with the DUT through alternative current paths

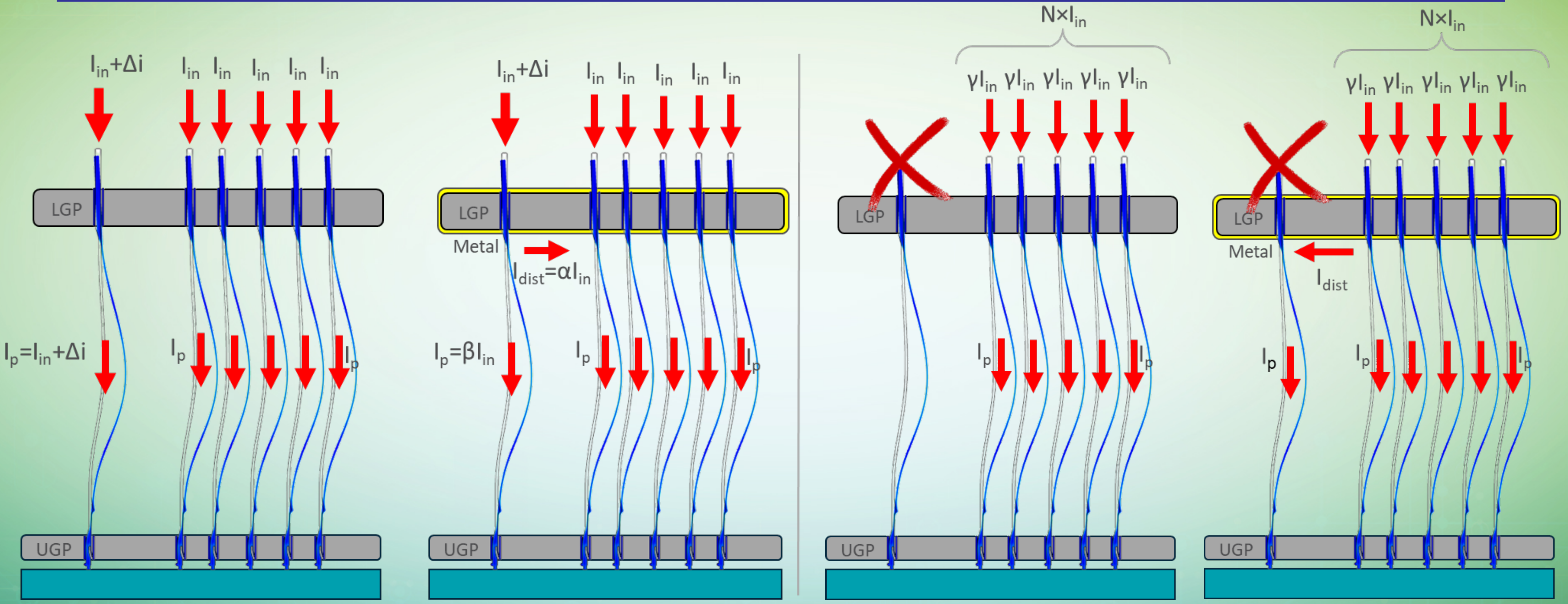
Metallization High Magnification



Metallization 2-Probe Circuit



Examples of how MeGP can help



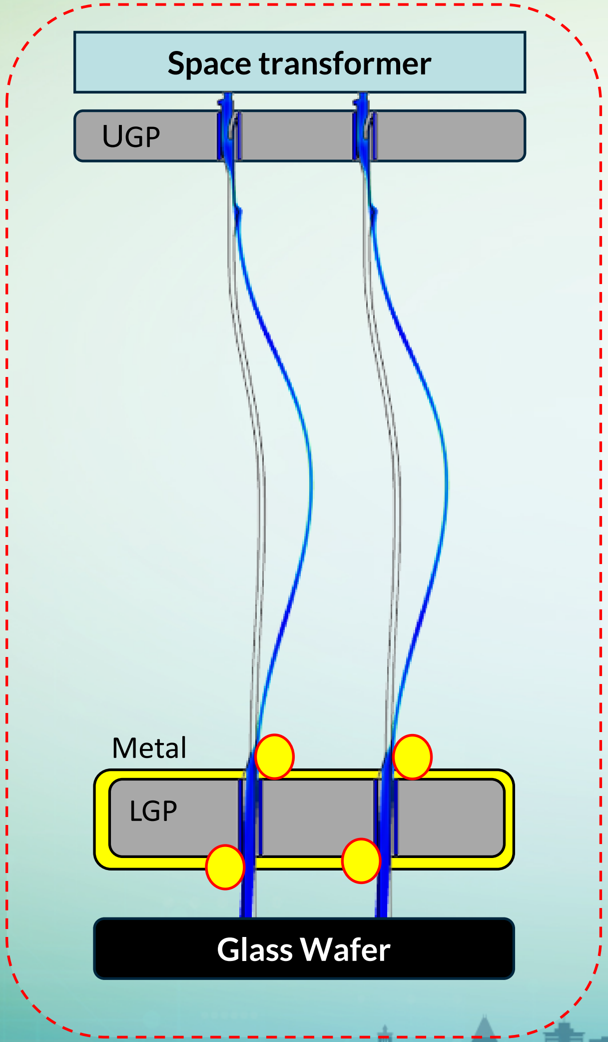
No MeGP

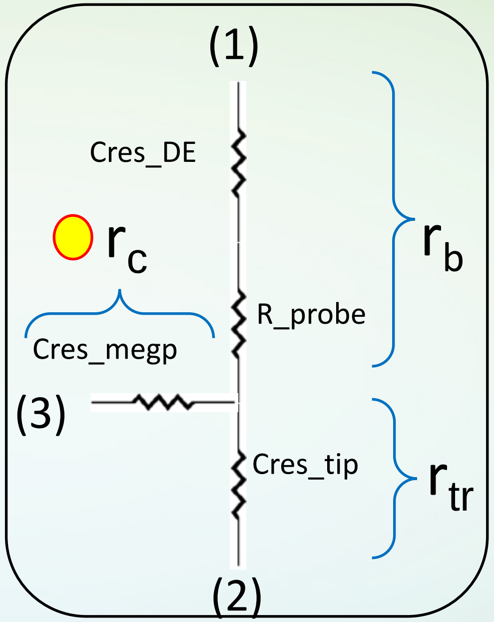
Current Spikes are re-distributed in MeGP case

No MeGP

Poor contact or disconnect

MeGP Technical Terminology



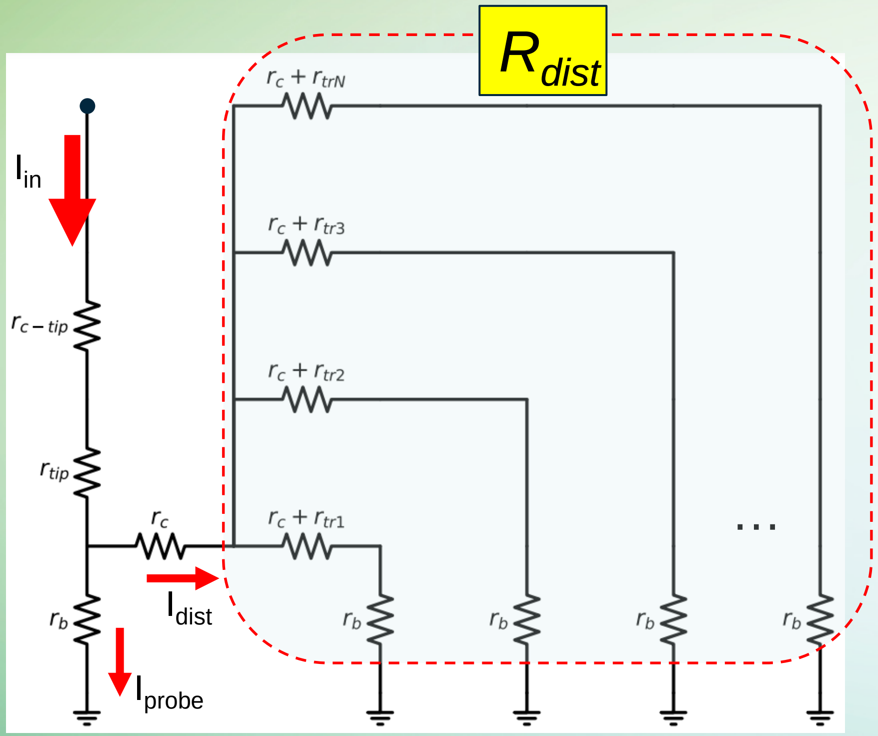


r_b: Probe body + DE Cres

r_c : Tip-MeGP Contact resistance

r_{tr}: Trace resistance

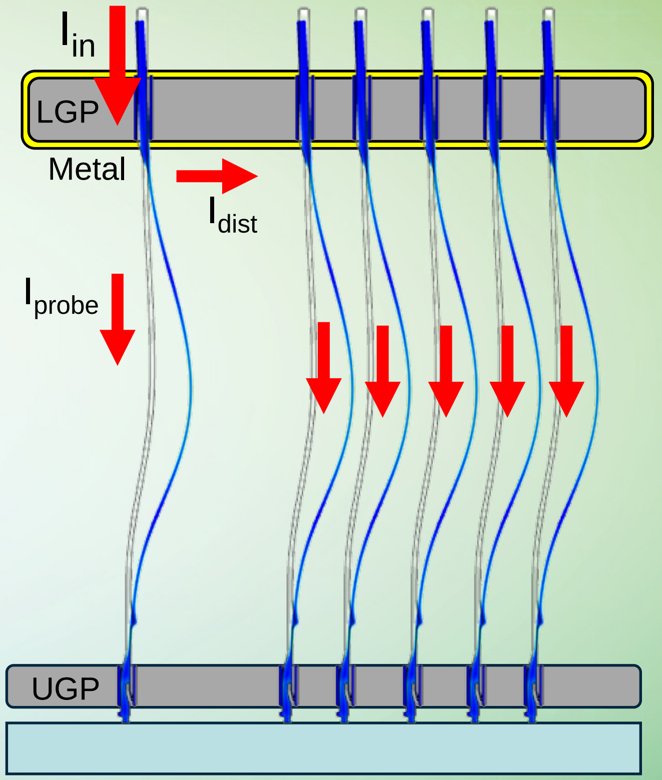
Generalized MeGP Effective CCC model (building block)



$$R_{dist} = \left(\sum_{n=1}^{N} \frac{1}{r_c + r_{tr(n)} + r_b} \right)^{-1}$$

Effective CCC

$$ECCC = I_{probe} \underbrace{\left(1 + \frac{r_b}{r_c + R_{dist}} \right)}_{\text{amplification factor}}$$



- r_b: Probe body + DE Cres
- r_c : Tip-MeGP Contact resistance
- r_{tr}: Trace resistance
- N: Number of probes
- R_{dist}: resistance of distributed network

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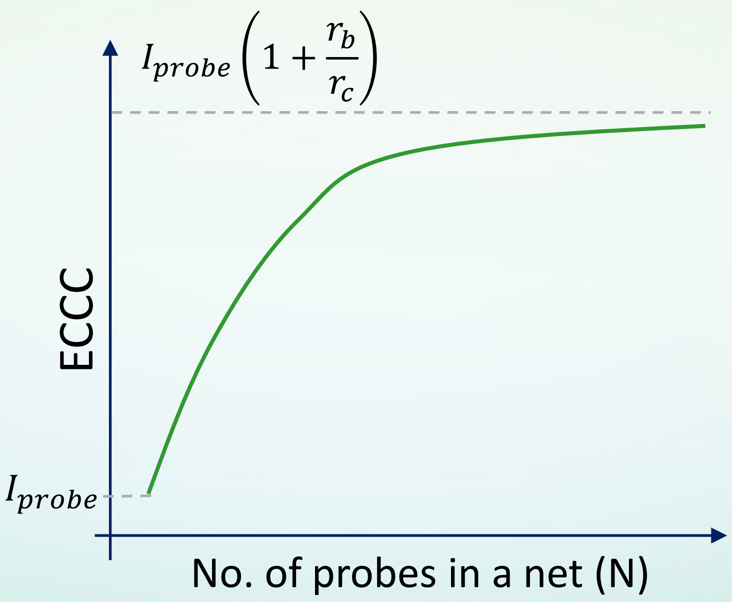
Effect of trace resistance and number of probes

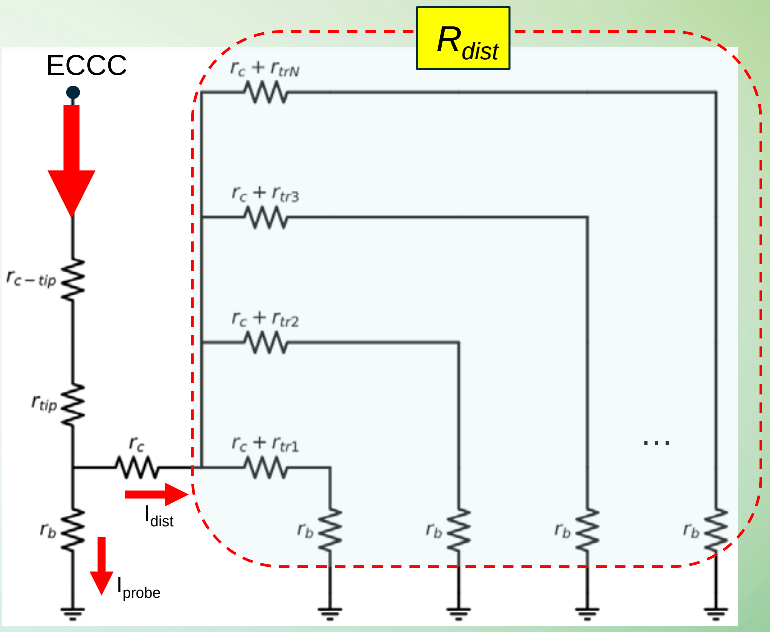
(1) If r_{tr} << $r_c + r_b$, the CCC will be layout independent, and the general equation reduces to:

$$ECCC_1 = I_{probe}\left(1 + \frac{r_b}{r_c + \frac{r_c + r_b}{N}}\right)$$

(2) For large gang numbers, N, the equation reduces to:

$$ECCC_2 = I_{probe}\left(1 + \frac{r_b}{r_c}\right)$$

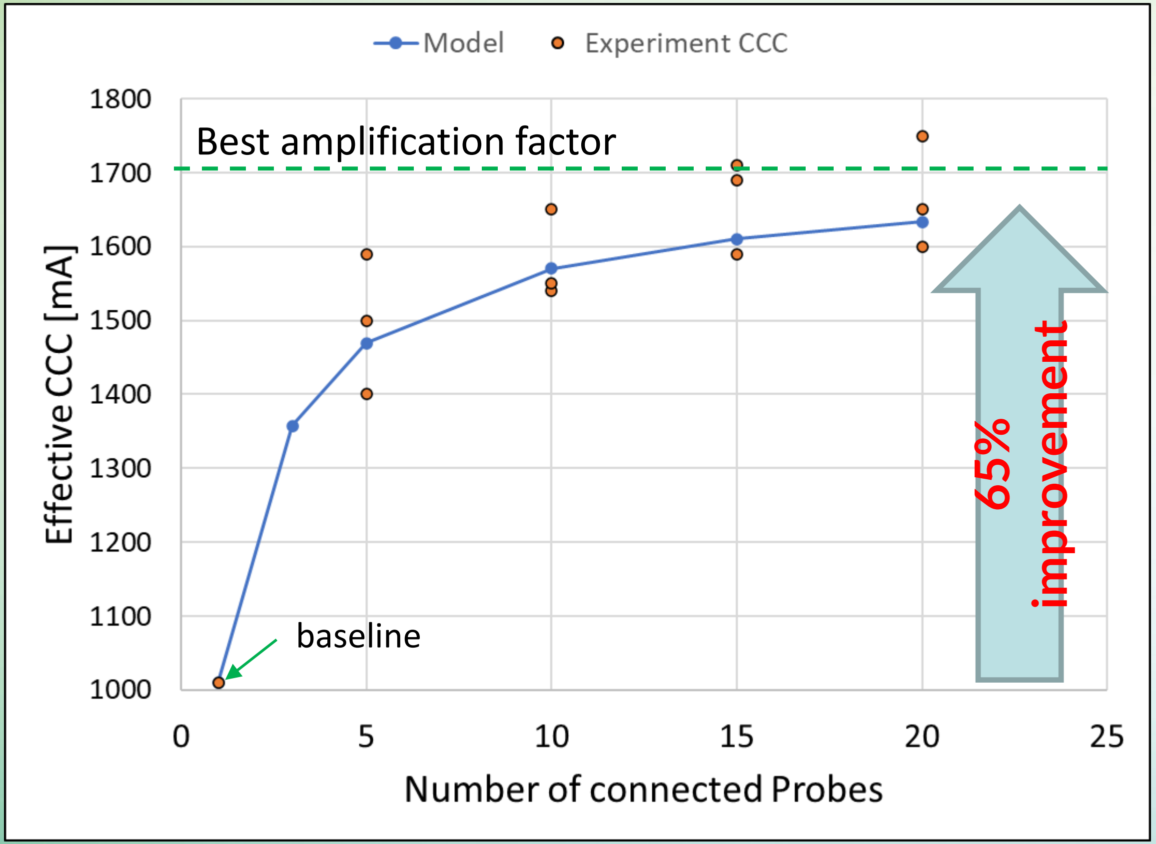




$1 + \frac{r_b}{r_c}$ **is the best CCC amplification factor one can get.**

rb: Probe body + DE Cres
rc : Tip-MeGP Contact resistance
rtr: Trace resistance
N: Number of probes

Validation using measured CCC and True MeGP CRES data



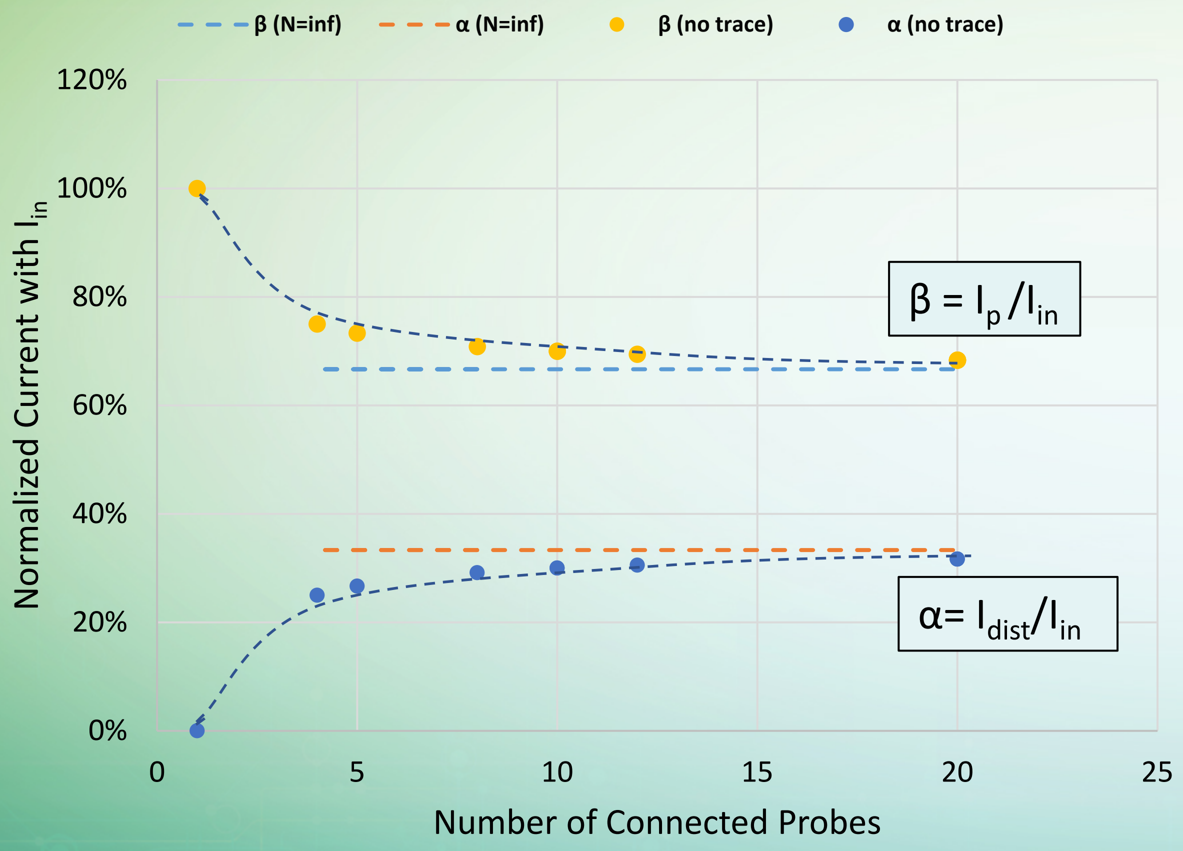
Effective CCC

$$ECCC = I_{probe}\left(1 + \frac{r_b}{r_c + R_{dist}}\right)$$

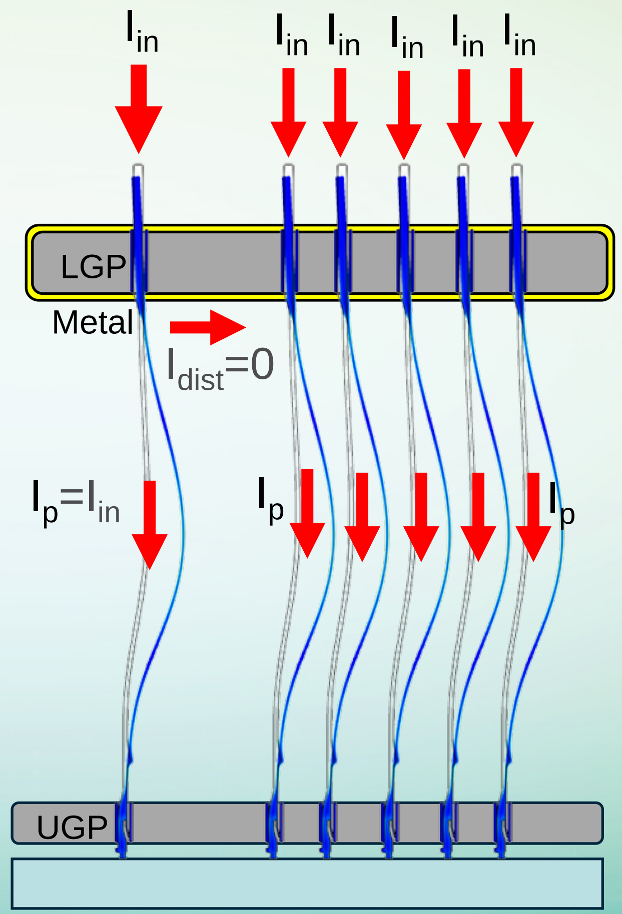
amplification factor

- Excellent agreement between model and experiment was achieved.
- ECCC showed a <u>65%</u> average improvement for 20 connected probes.

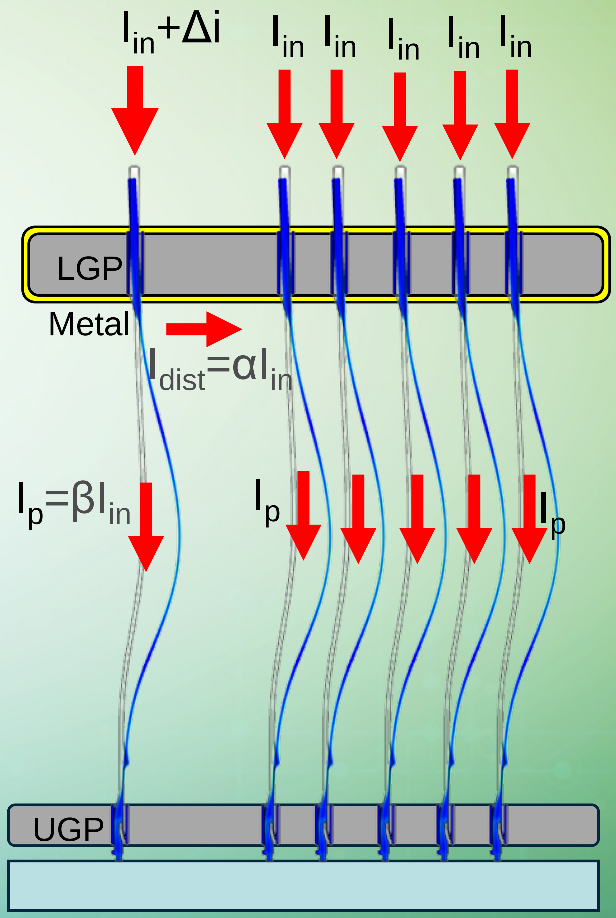
Model Extension to real cases – Current Spike events



Ideal case with no current variation

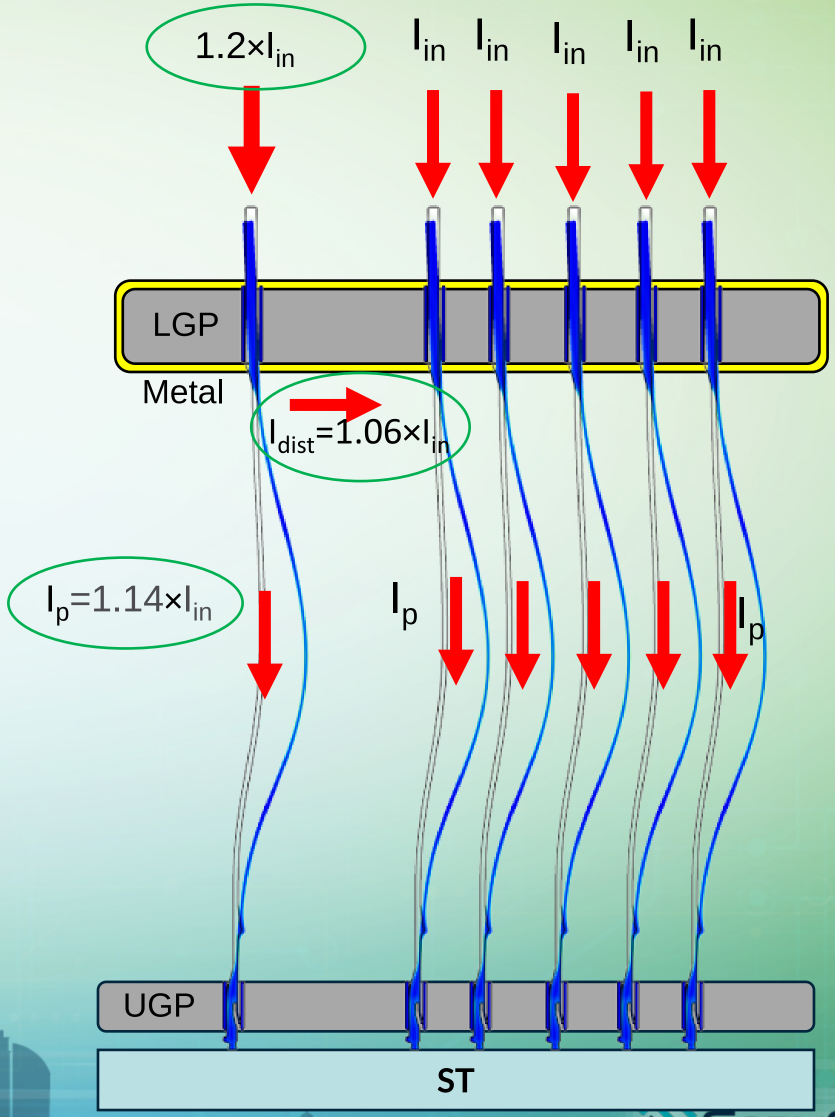


Current spike event



Numerical example

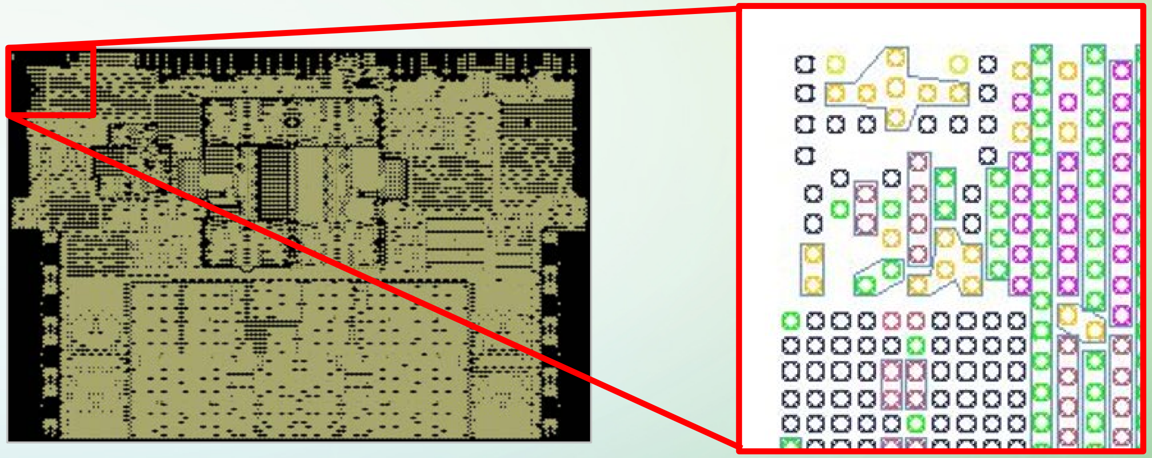
- For a 20-ganged probes with negligeable trace resistance, α = 32% and β = 68%.
- A 20% increase in nominal current (I_{in}), translates to 6.4% increase in I_{dist} and 13.6% in I_{probe}.



MeGP Design Challenges

- Challenge: Design of the MeGP is difficult due to the number of nets and probes involved.
  - A design error could be fatal in the yield of the MeGP leading to shorts from VDD to GND
  - Design complexity could significantly
- Solution: Automated Design and DFM rule implementation
  - Eliminates mistakes from manual design
  - Decreases design cycle time to a few hours

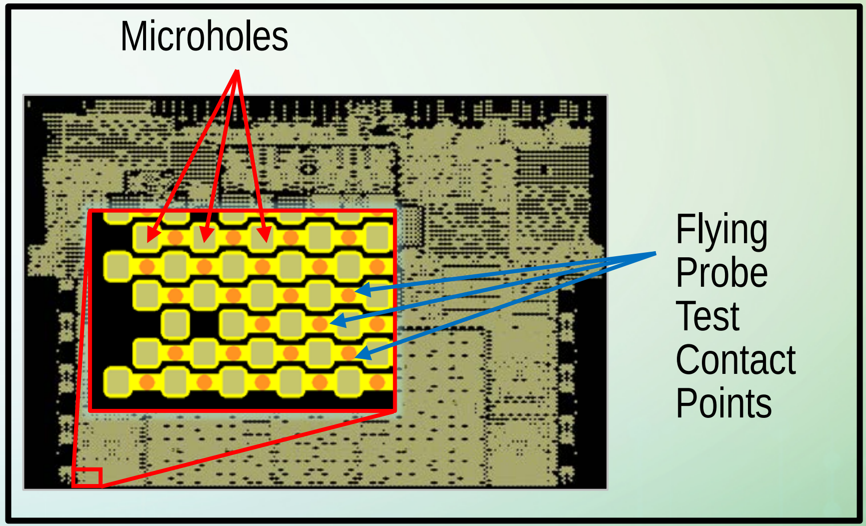
Design Automation Improves Design Cycle Time and Reduces Errors



MeGP Verification Challenges

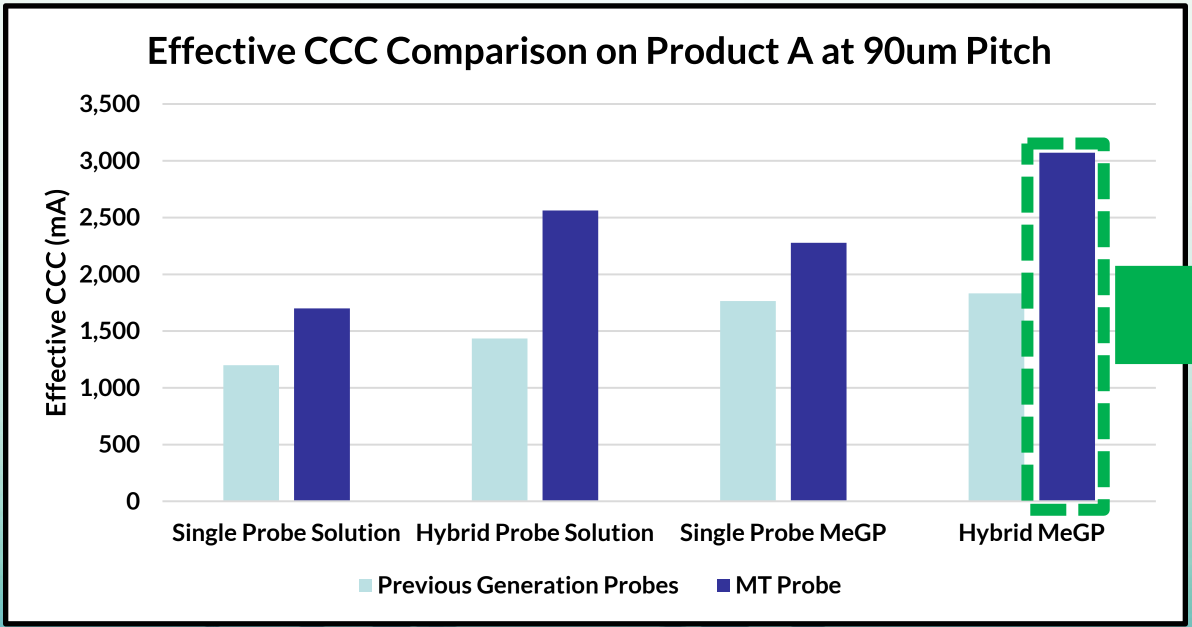
- Challenge: MeGP needs to be verified for shorts before stitching the probes and completing assembly of the Probe Card
  - POR process flow verifies electrical continuity with PRVX
    - If short is found the Probe Head would need to be disassembled and fixed
      - Long Cycle times at the last step of the manufacturing process
- Solution: Implementation of Flying Probe Test after MeGP Plating
  - Allows rework of GPs if needed
  - Ensures high quality through manufacturing process

Flying Probe Test Contact Points



Maximizing Effective CCC

- MeGP Improves Effective CCC by 65% depending on the probe architecture
- FFI has achieved the first >3A CCC Probe card at 90um pitch using Next generation MT Probes, Hybrid probes, and Metallized Guide Plate
  - Short Cycle Time and Excellent quality guaranteed through Design Automation and Outgoing Flying Probe Test



MT Hybrid with MeGP provides Best Effective CCC >3A

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Thank You!!