SWTEST

PROBE TODAY, FOR TOMORROW

2023 CONFERENCE

Challenges and Improvement Actions for HPC Wafer Testing

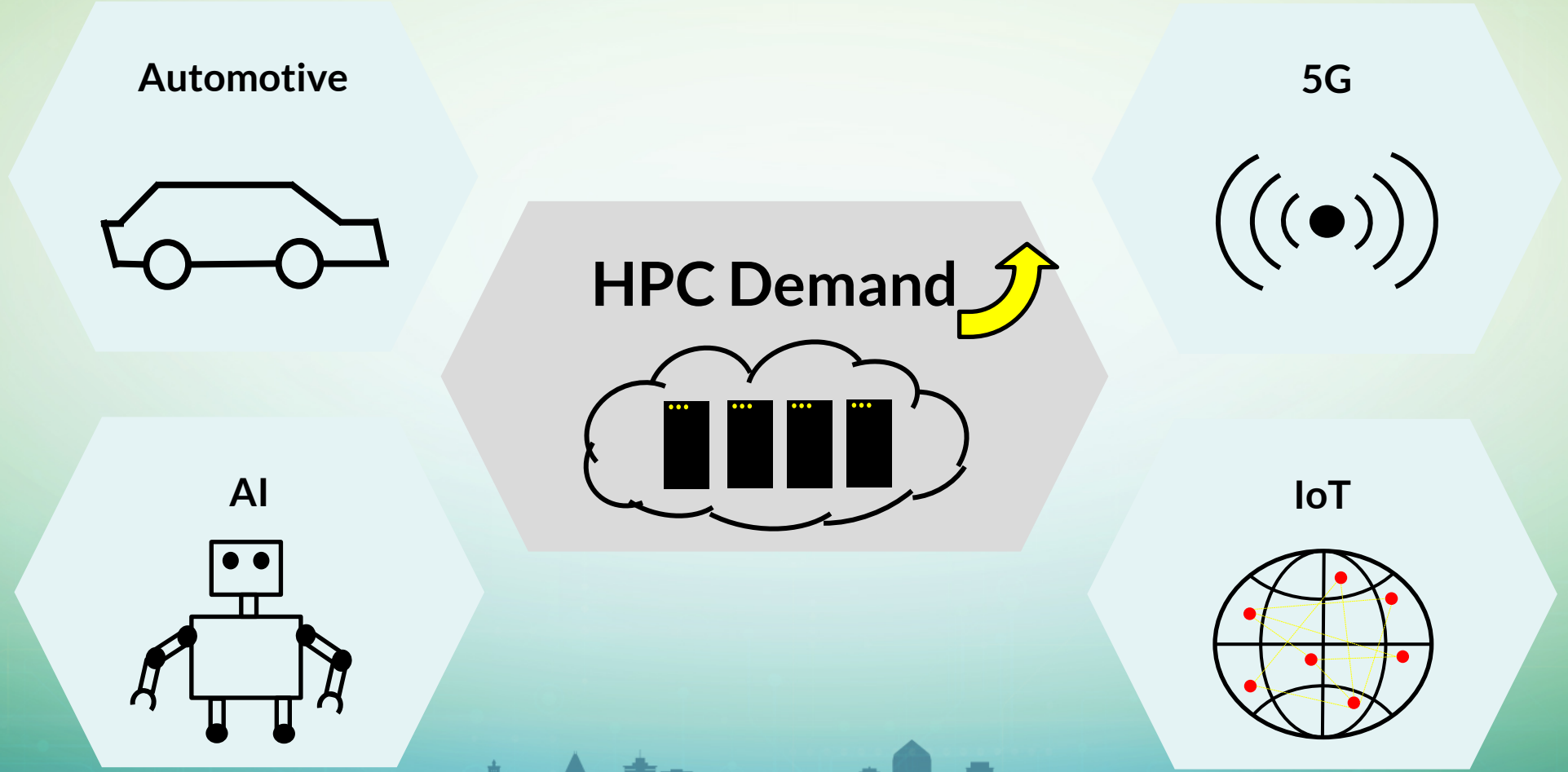
Kenny Tang
TSMC

Overview

- Introduction
- HPC Challenges and Improvement Action
  - High Force
  - High Power
  - High Temperature
- Summary

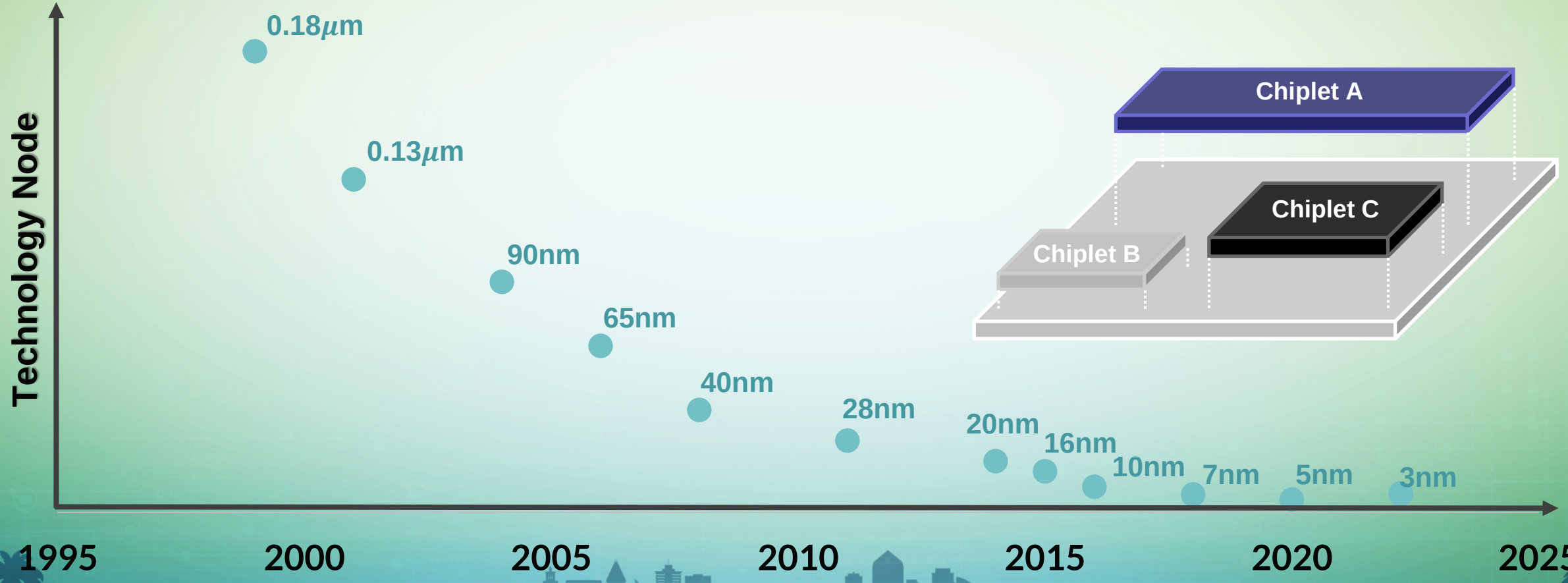
HPC Demand

- The demand for HPC (High Performance Computing) growth rapidly.



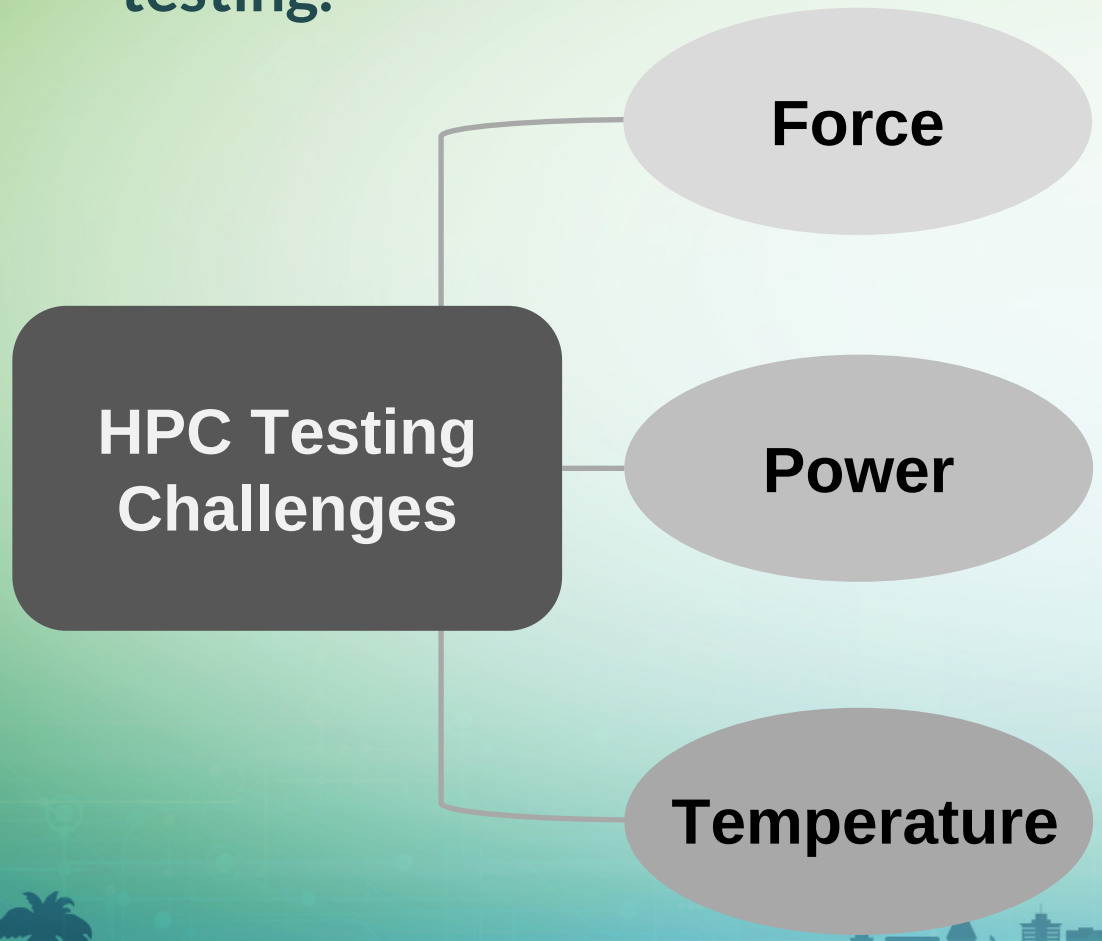
HPC Testing Challenges

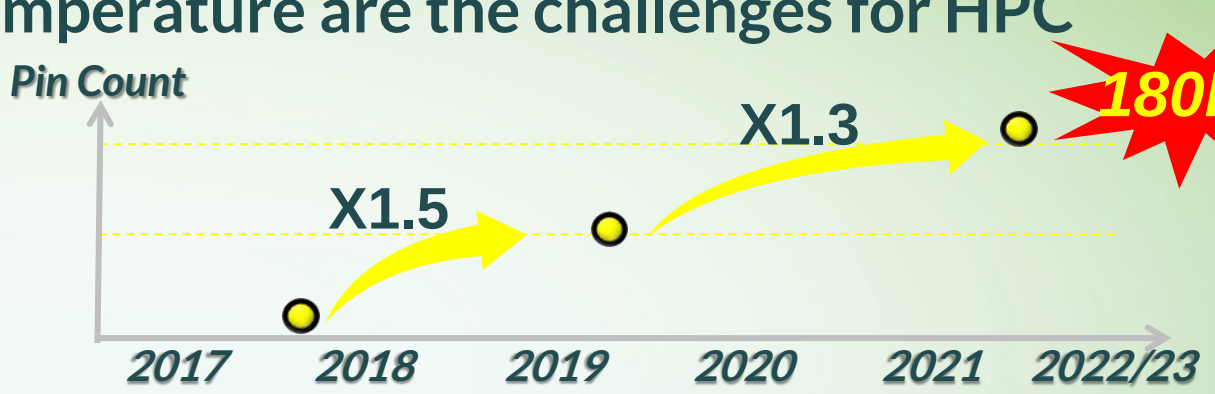
- With the development of silicon node technology and advanced integration process, the device complexity increase.

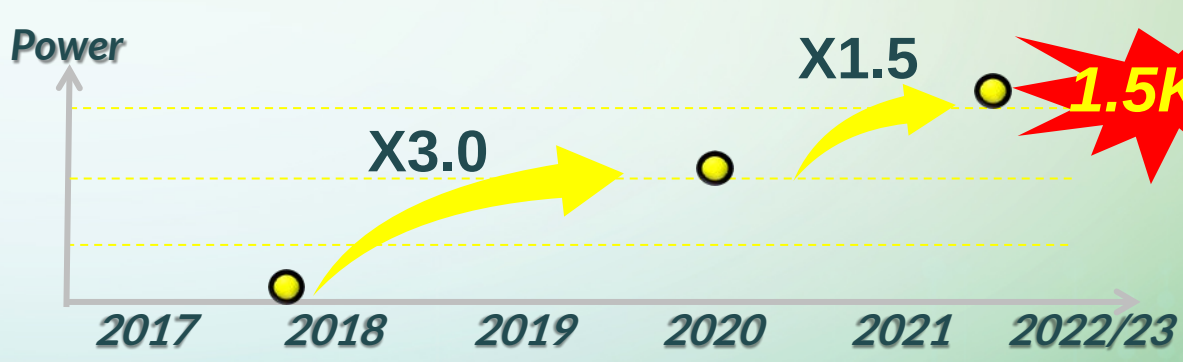


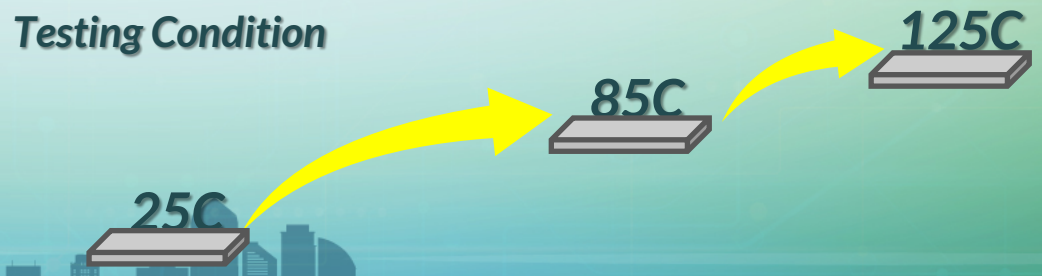
HPC Testing Challenges

- High Force, High Power, and High Temperature are the challenges for HPC testing.



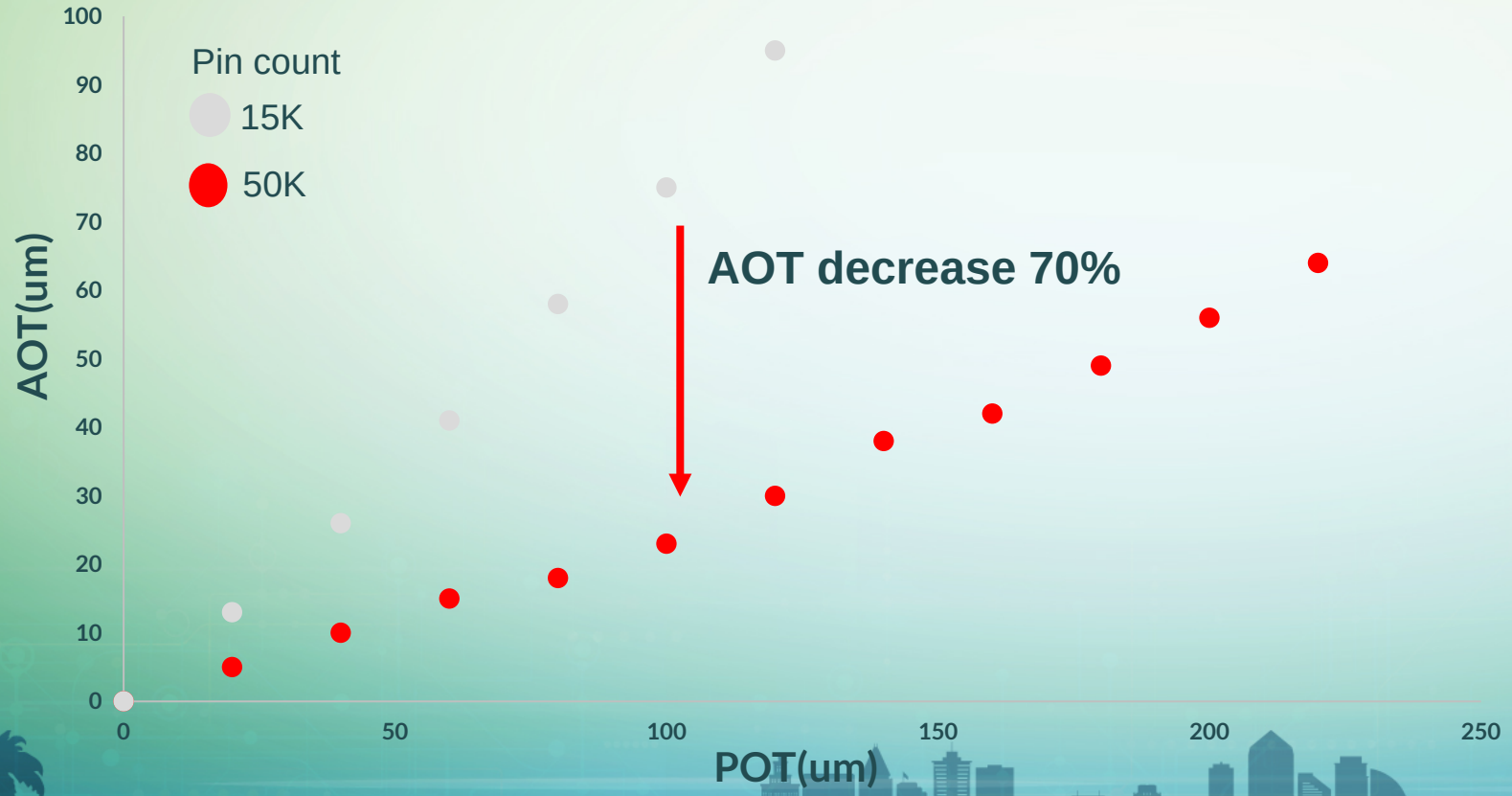


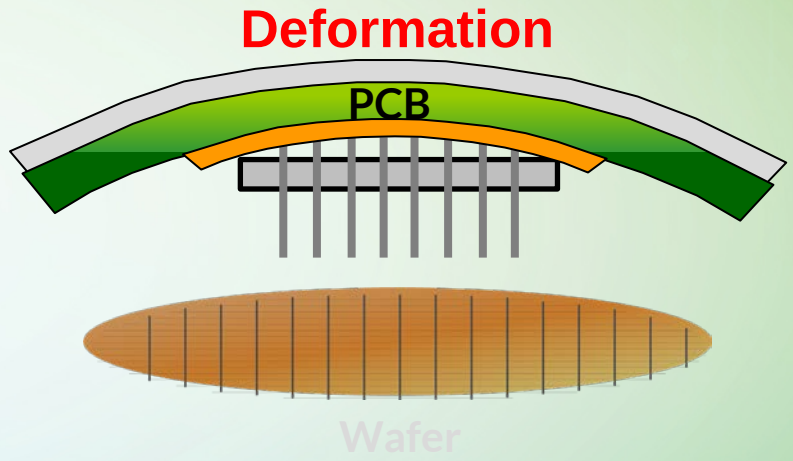




HPC Testing Challenges – High Force

- **Observation**
  - For high pin count probe card, the significant decrease in AOT is caused by PCB deformation.





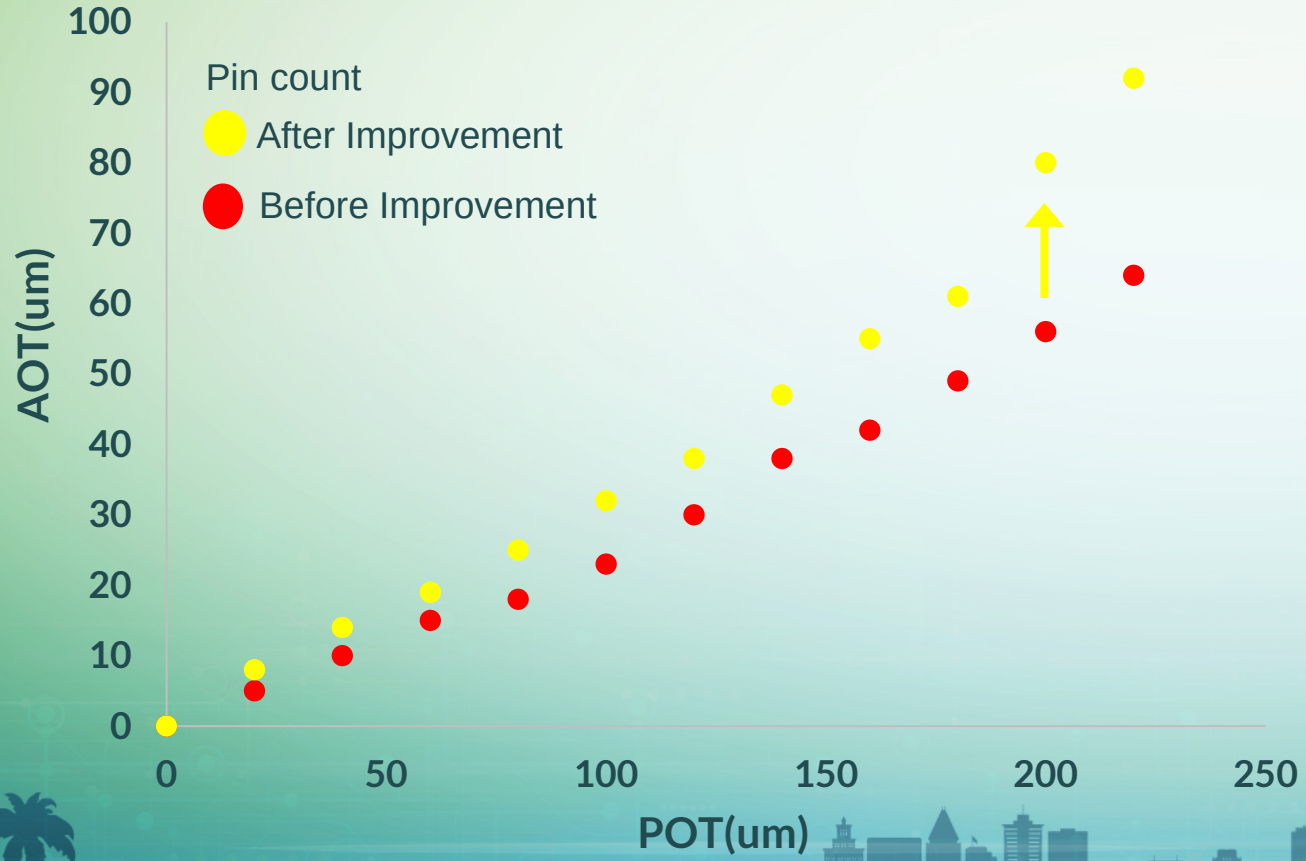
Pin Count/ Force ↑

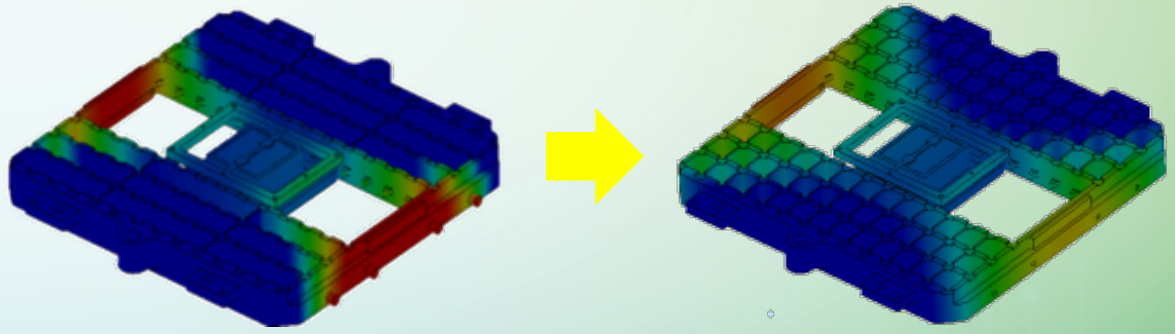
➡ PCB Warpage ↑

➡ AOT ↓

HPC Testing Challenges – High Force

- **Improvement Action**
  - **Improve AOT/POT ratio to 43% from 30% by (1) Stiffener Structure Enhancement (2) Material Enhancement.**

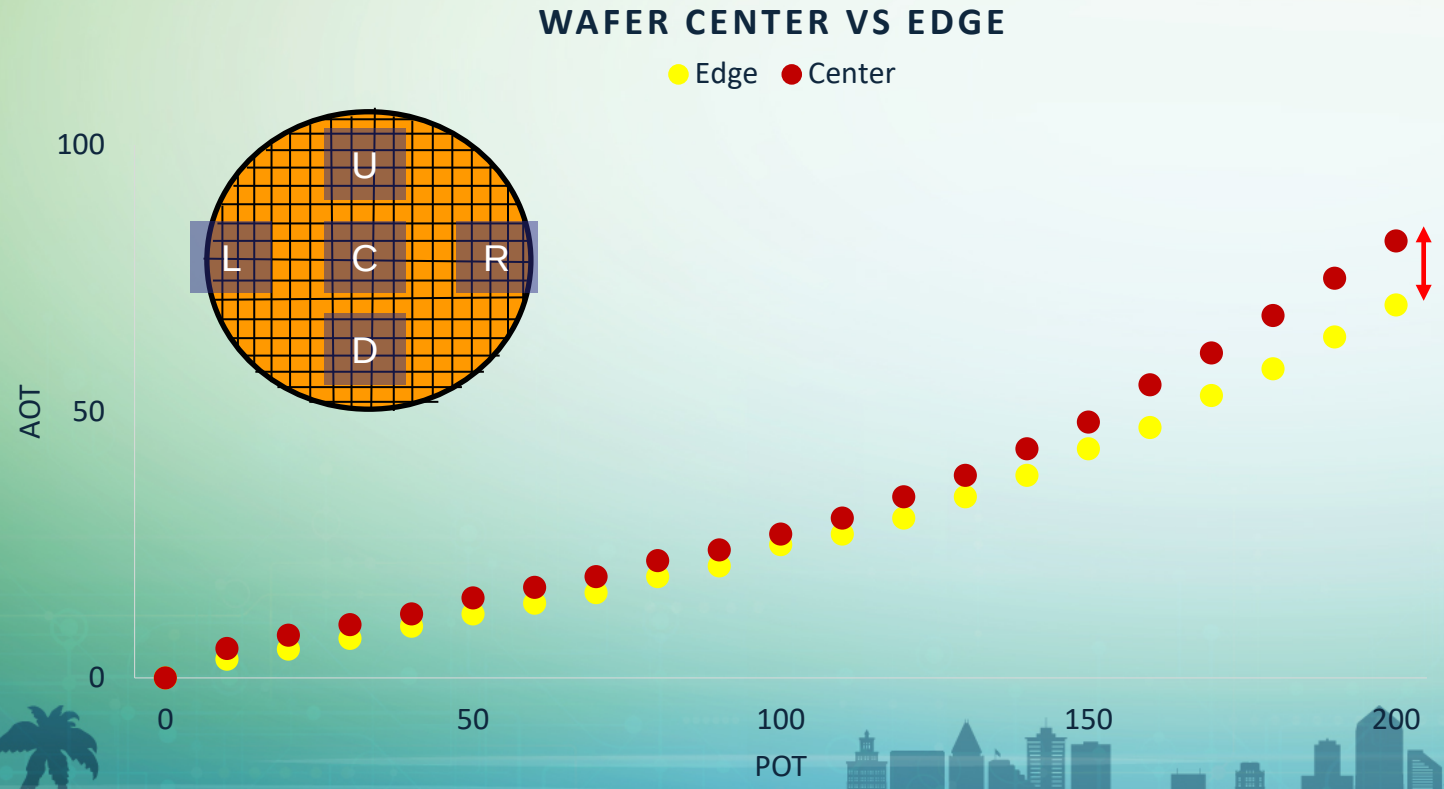




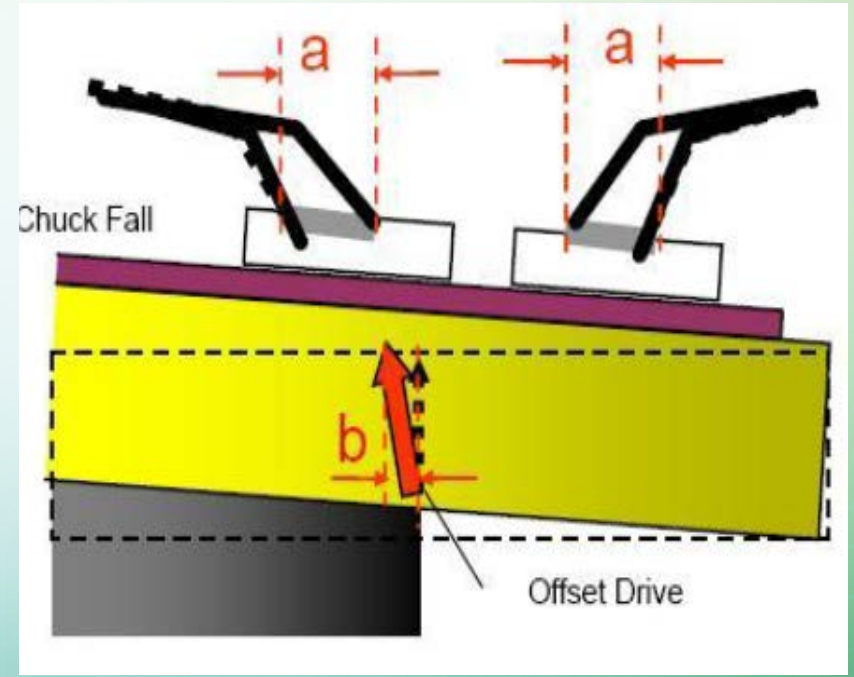
HPC Testing Challenges – High Force

- **Observation**
  - **The non-uniform AOT is observed with high pin count testing.**

Difference of AOT is observed with high pin count P/C

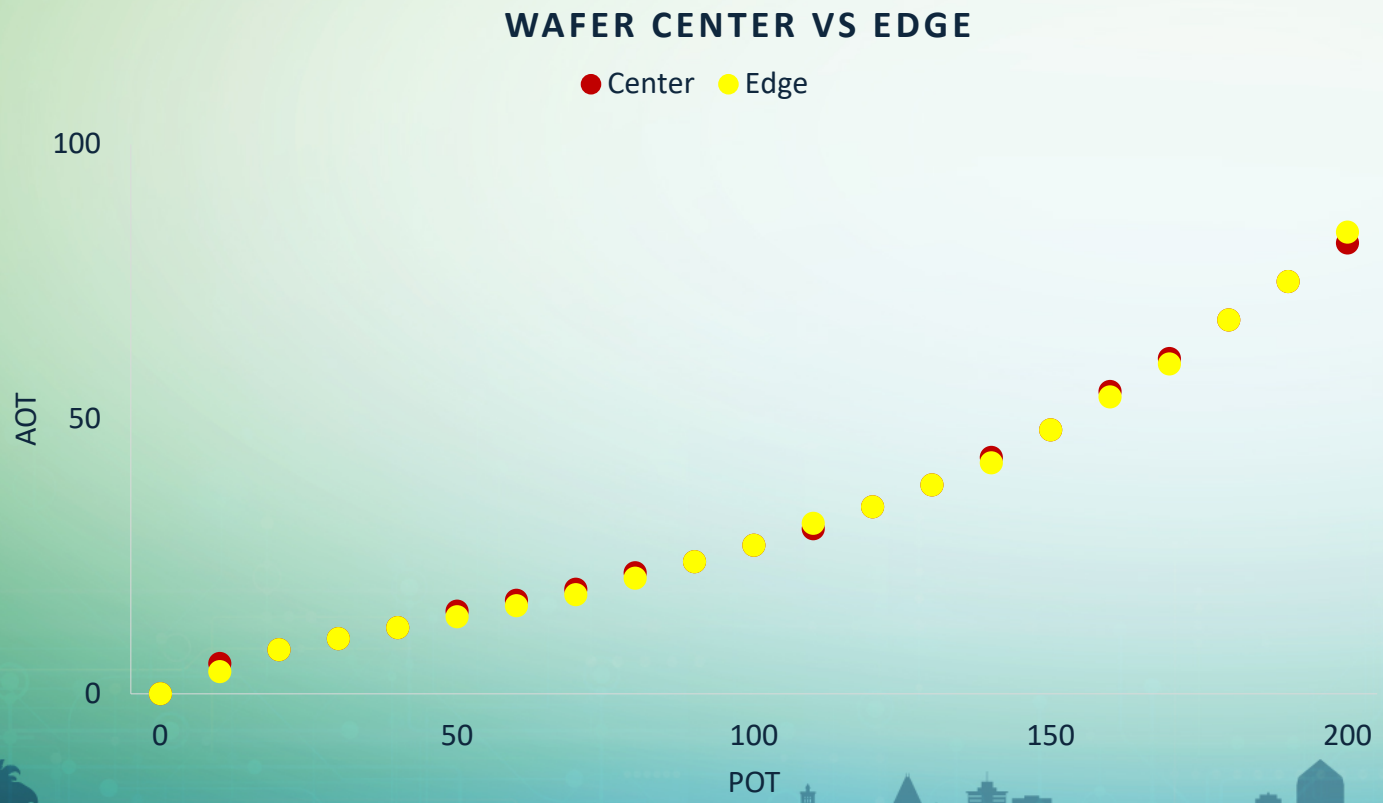


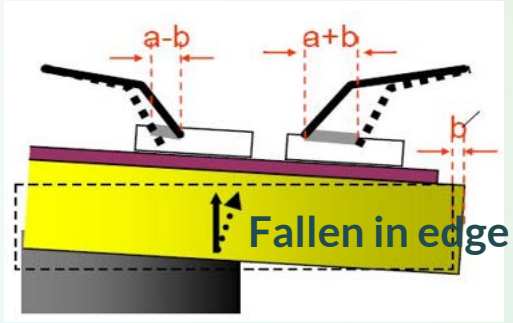
Chuck Deflection issue

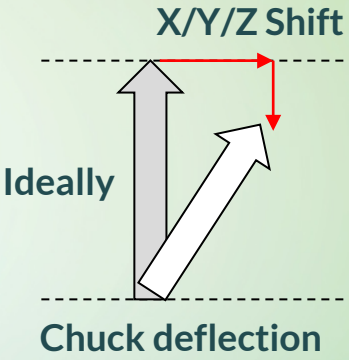


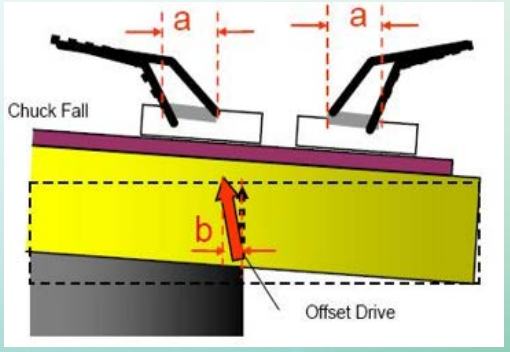
HPC Testing Challenges – High Force

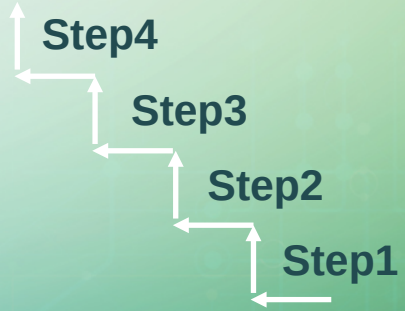
- **Improvement Action**
  - ➢ **Enable 3D offset function to compensate chuck bending issue.**







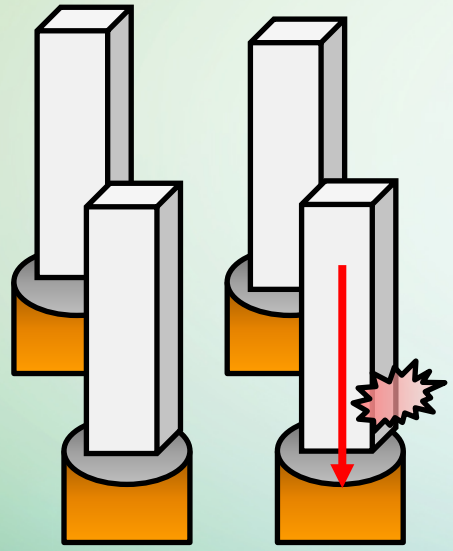


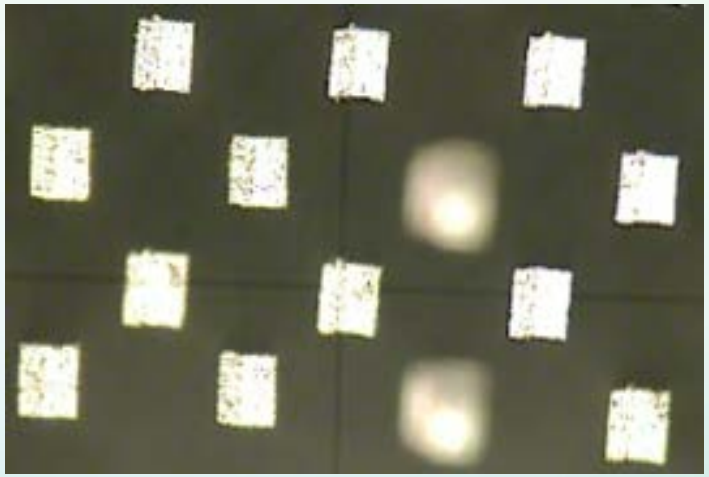


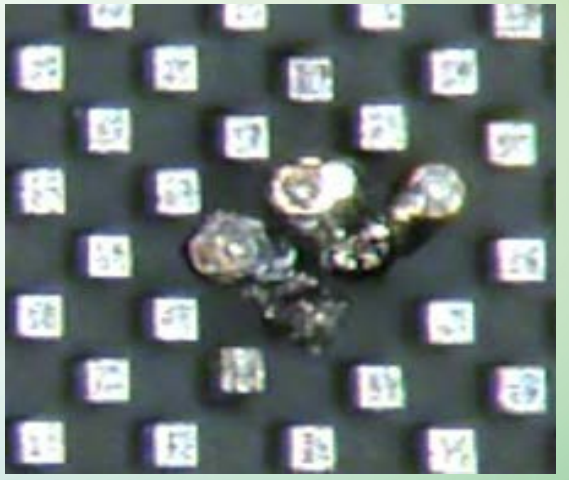
Move opposite direction compensate shift

HPC Testing Challenges – High Power

- **Observation**
  - The higher tip burnt rate is observed in HPC testing.





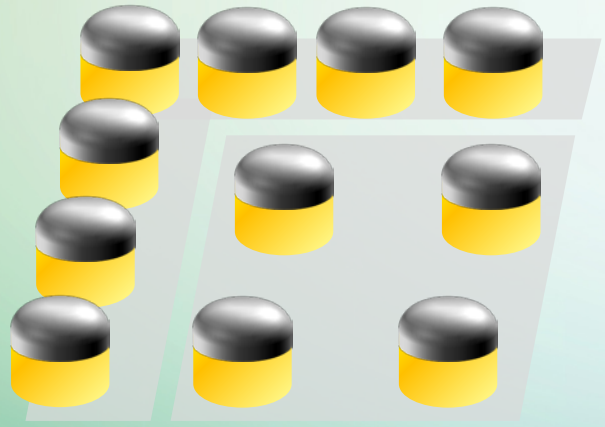


Current **> CCC (Current Carrying Capability)**

HPC Testing Challenges – High Power

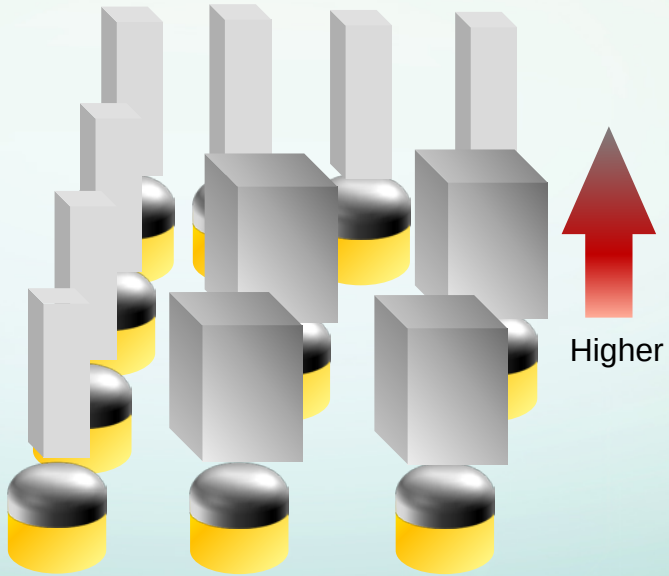
- **Improvement Action**
  - Hybrid probing: The probe with higher CCC is used in pitch > 100um.

Fine Pitch IO < 100um

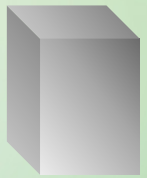


Loose Pitch > 100um

- Power, GND



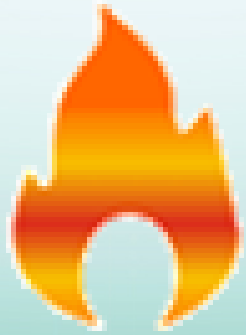
Hybrid Probing

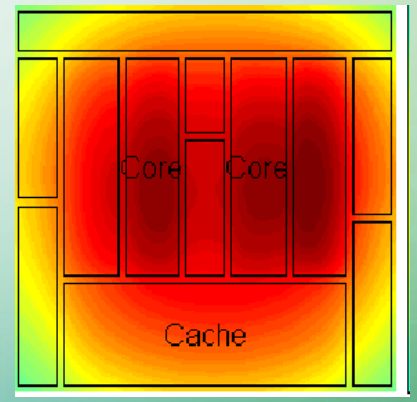
Probe type		
Pitch(um)	< 100	> 100
CCC	1.0X	***1.39X***

HPC Testing Challenges – High Power

- **Observation：**
  - A thermal challenge comes from high current and high-power consumption testing, so heat dissipation and temp. control accuracy become very challenging and critical.

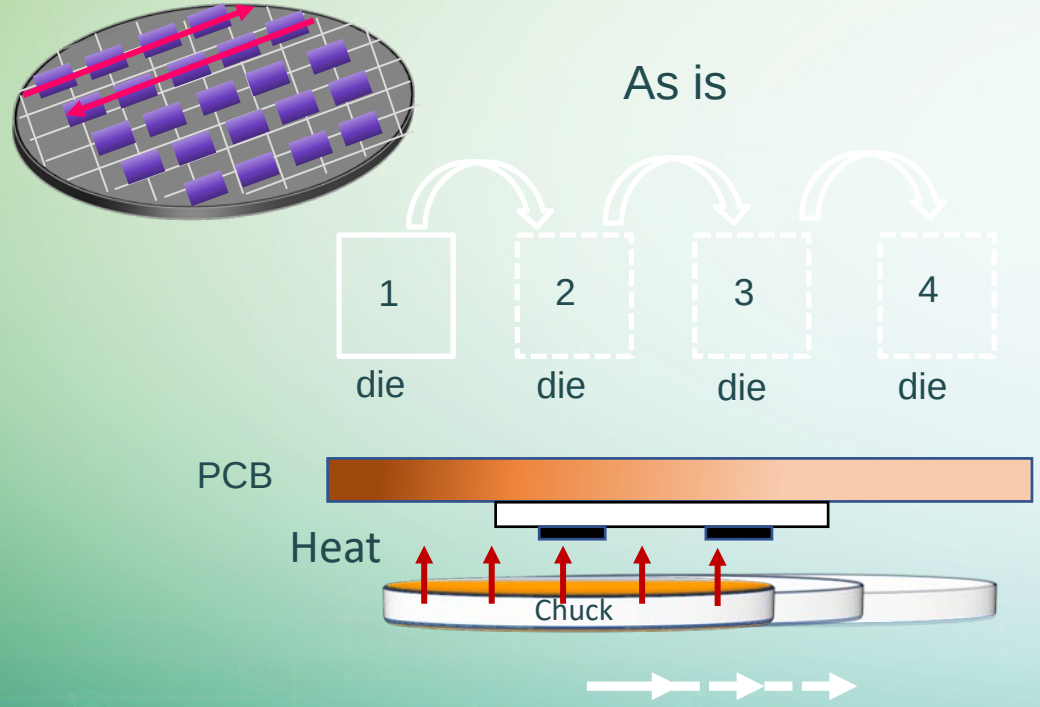
High Current (>10A) + **High Power Consumption (>600W)** = **Temperature issue**



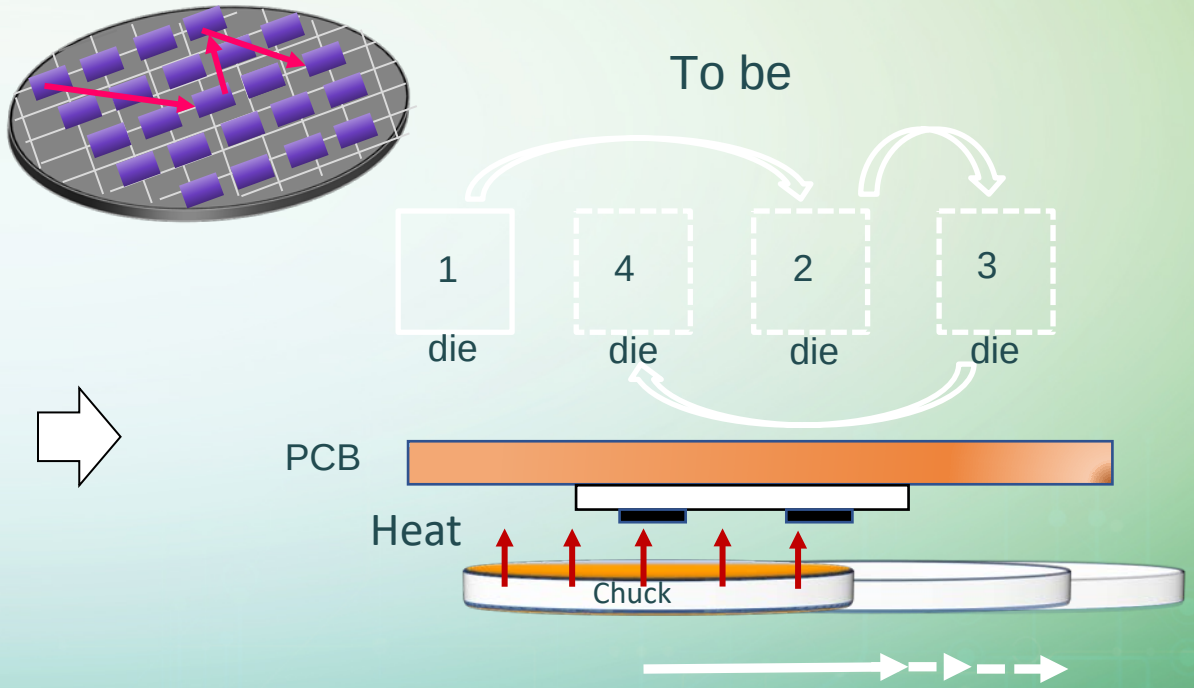


HPC Testing Challenges – High Power

- **Improvement Action**
  1) **Index move optimization: Index move is changed from short distance to long distance to improve PCB temperature uniformity.**



Index Move with short distance

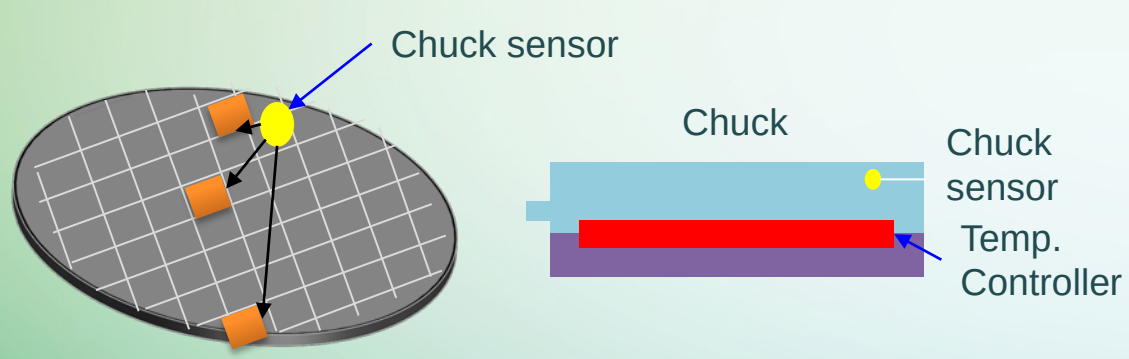


Index Move with long distance

HPC Testing Challenges – High Power

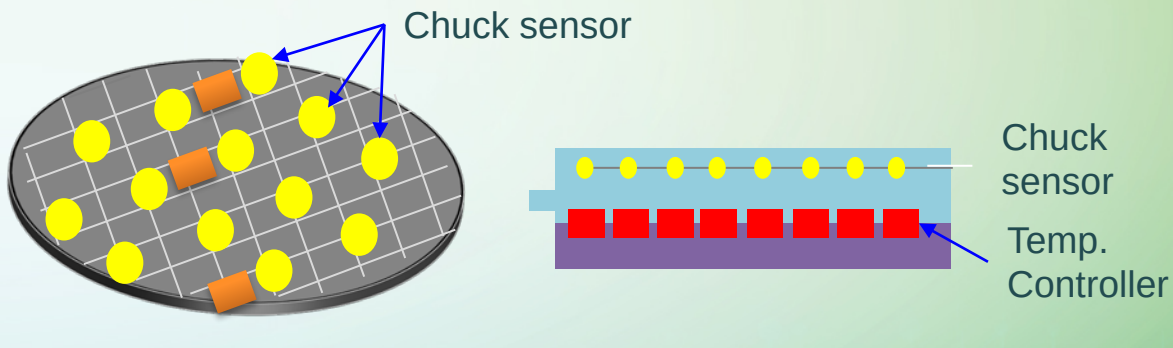
- **Improvement Action**
  2) **To enhance temp. control accuracy, the multiple sensor chuck has individual temp. controller.**

As is



One sensor chuck
Temp. control from 1 point temp.

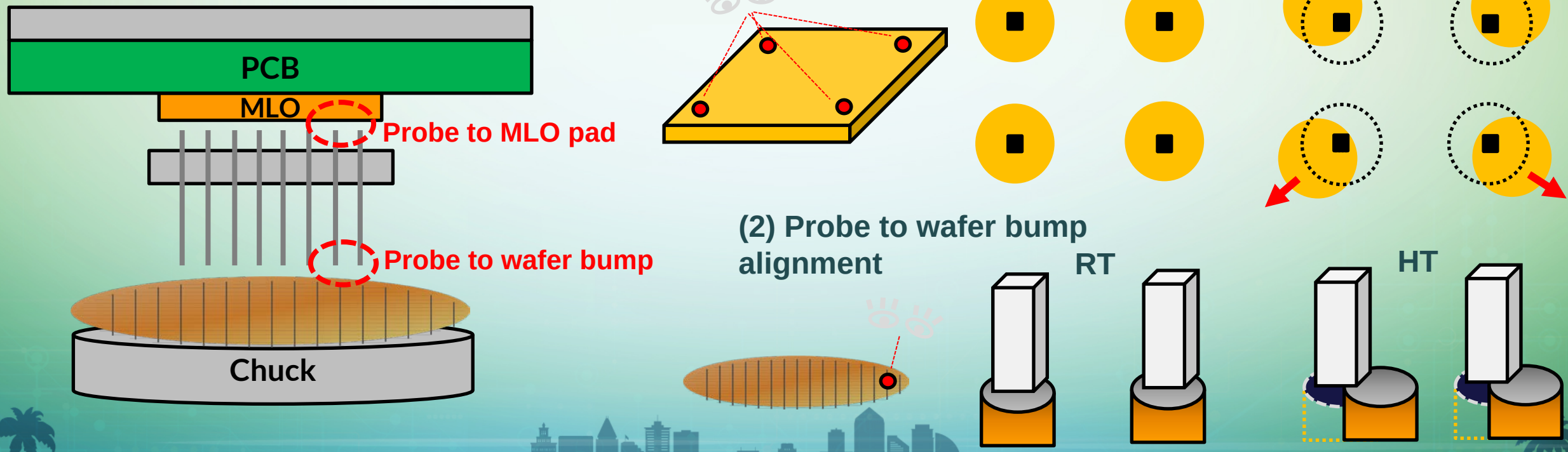
To be



Multi sensor chuck
Temp. control with individual area

HPC Testing Challenges – High Temp.

- Observation
  - Due to the CTE(Coefficient of Thermal Expansion) difference of materials, the alignment of the Probes with MLO pad and wafer bump shifts in high temperature conditions.



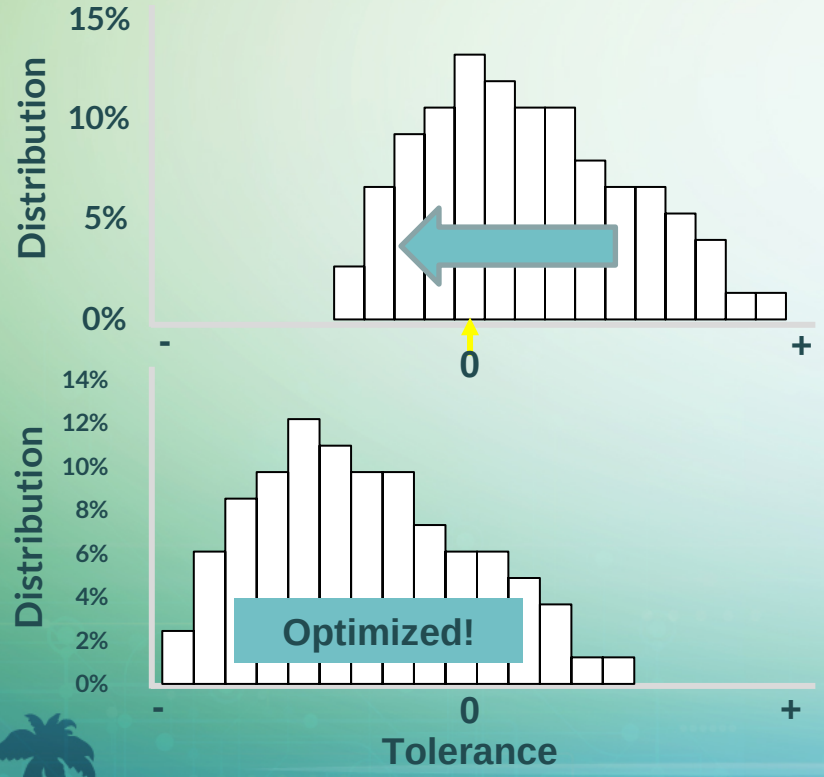
HPC Testing Challenges – High Temp.

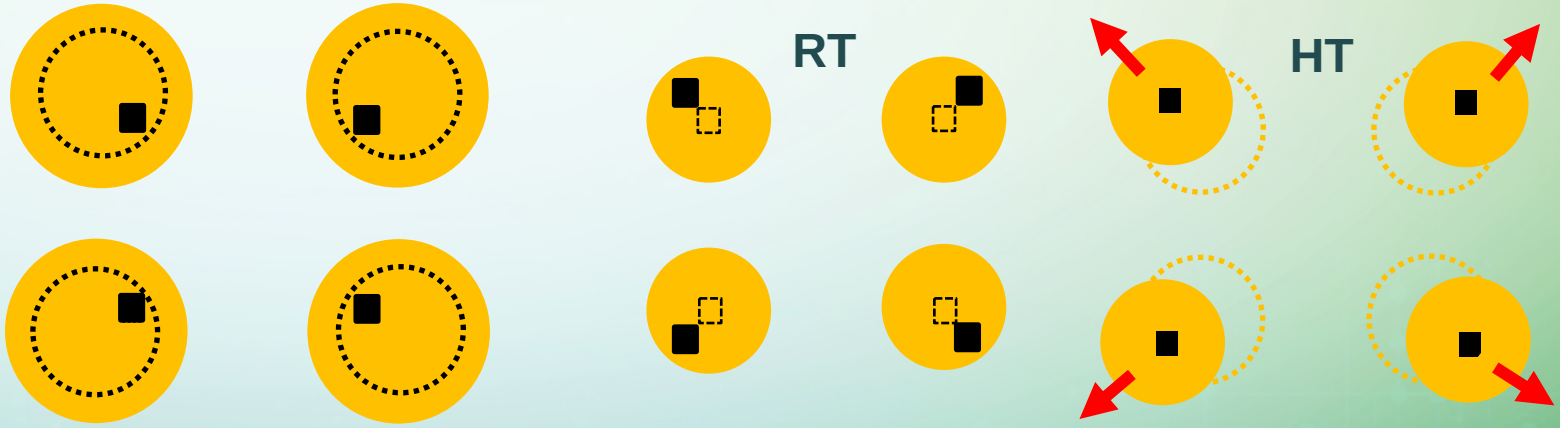
- Improvement Action
  - To improve the alignment, we can optimize below factors.

Parts	Key Factors	Controllable
MLO	Pad size	O
	Manufacture Tolerance	O
	CTE	X
Probe Head	Scaling	O
	CTE	X
Wafer	Probing Area	O
	Pitch	X
	CTE	X
	Testing temperature	X
	Bump size	X
Prober/ Chuck	CTE	X
	Alignment Technology	O

HPC Testing Challenges – High Temp.

- Improvement Action for (1) *Probe to MLO pad* alignment
  1) Control the scaling of MLO dimension toward negative tolerance.
  2) Enlarge MLO Pad size to prevent contact issue.
  3) Design scaled UD to compensate MLO thermal expansion.





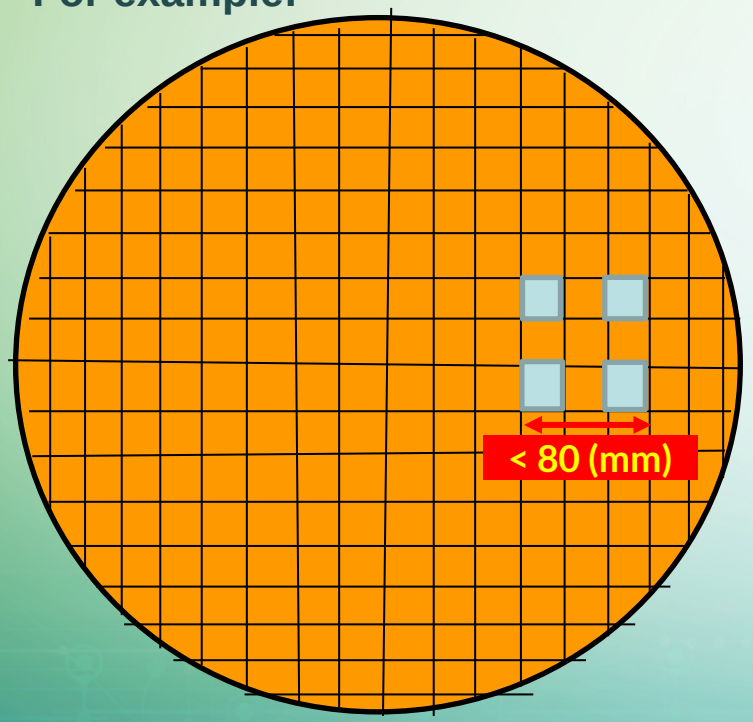
Enlarge pad size

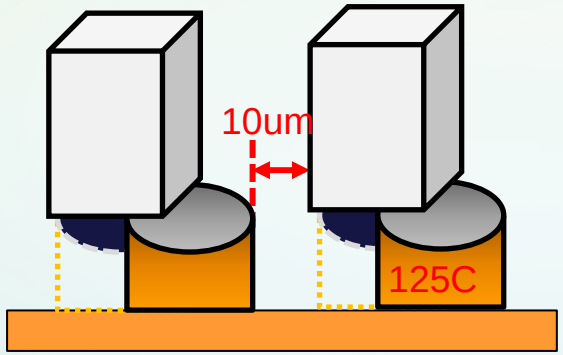
Design scaled UD to compensate

HPC Testing Challenges – High Temp.

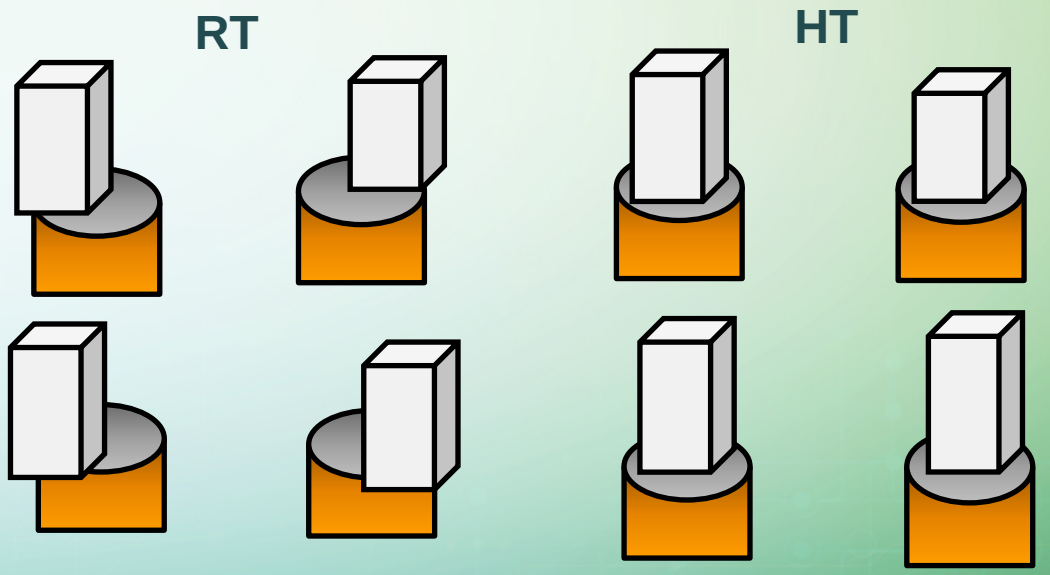
- **Improvement Action for (2) *Probe to wafer bump* alignment**
  1) **Constrain probing area.**
  2) **Design scaled LD to compensate wafer thermal expansion.**

For example:





Temperature: 125C
Pitch: 80um
Bump diameter: 50um
Probe dimension: 50 x 50
Probe alignment accuracy: 10um
Silicon CTE: 2.5 ppm
Thermal expansion: 20um

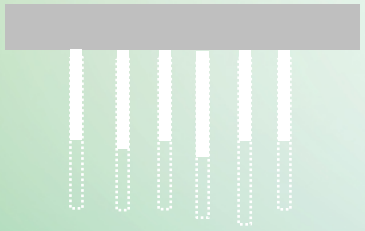


Constrain probing area

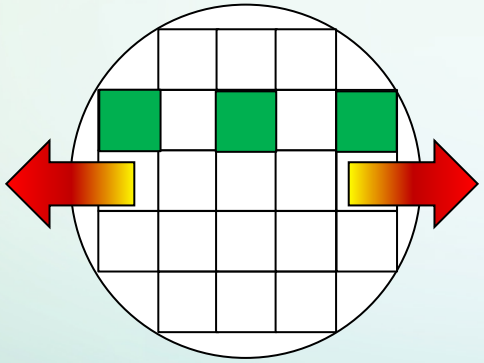
Design scaled LD to compensate

HPC Testing Challenges – High Temp.

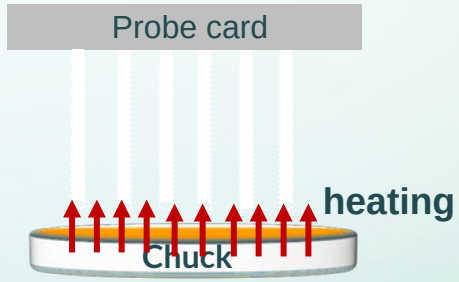
- **Improvement Action for (2) *Probe to wafer bump* alignment**
  3) Execute preheat function and total alignment before testing to make sure needle height and wafer position are stable after thermal expansion.



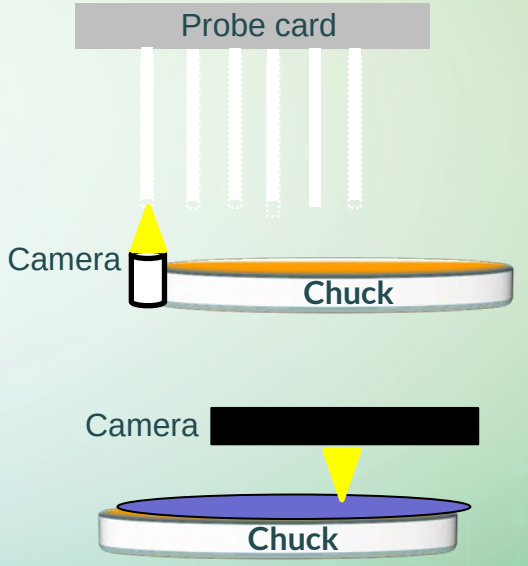
Needle expansion



Wafer expansion



Preheat
(Contact preheat)

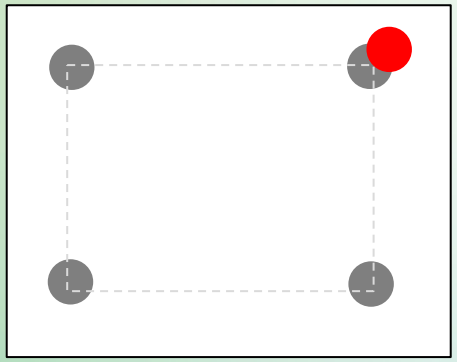


Alignment after preheat
(Needle & Wafer alignment)

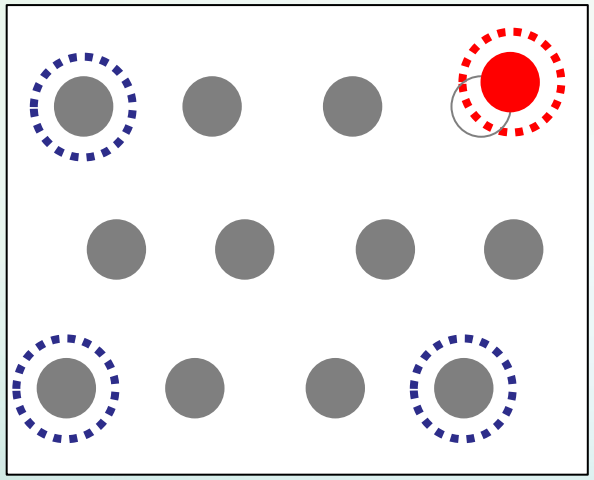
HPC Testing Challenges – High Temp.

- **Improvement Action for (2) *Probe to wafer bump* alignment**
  4) Enable PTPA(Pad to Pin alignment) function to make sure precise alignment.

AS IS
(4 pin alignment)

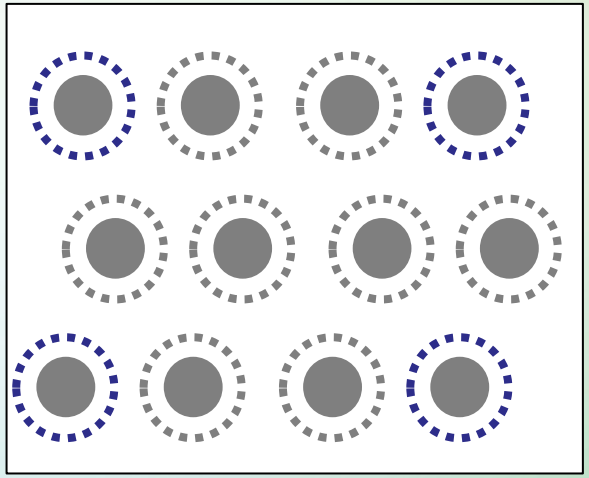


If 1 pin shift have
Probe Mark Shift Risk



Default Pin

TO BE(> 4 pins alignment)
PTPA - Pad to Pin alignment



Default Pin

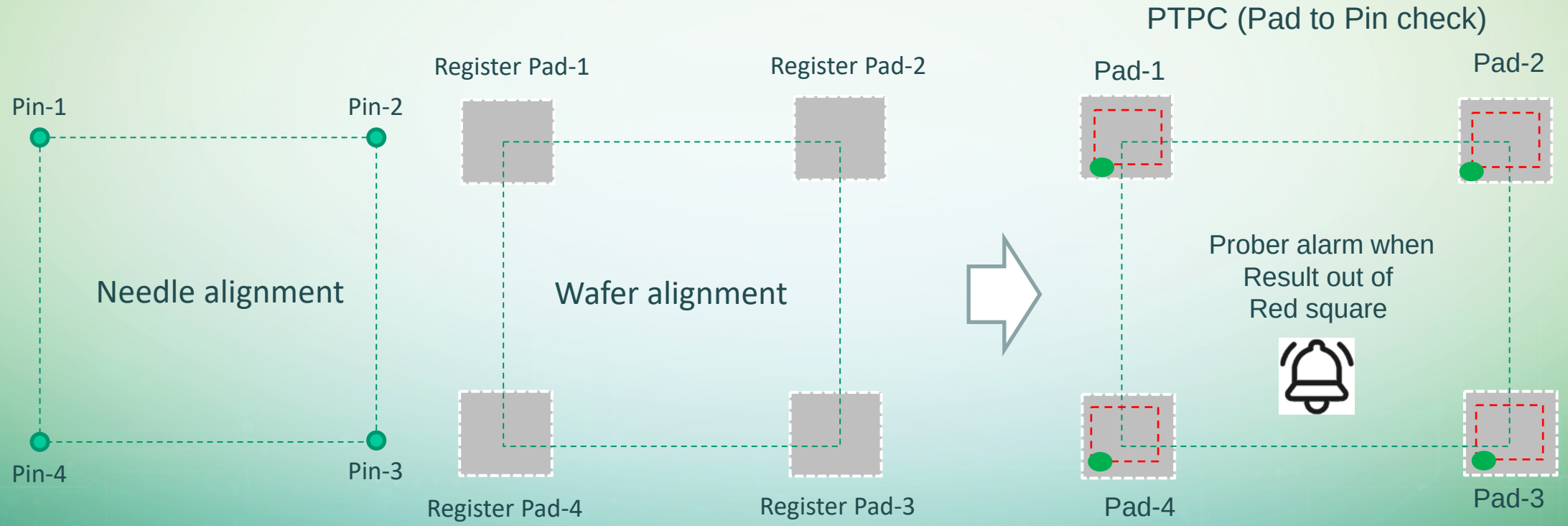
Additional Pin

Probe Center (θ) = Pin data angle(θ) + Card angle(θ) + PTPA Offset(θ)

HPC Testing Challenges – High Temp.

- **Improvement Action for (2) *Probe to wafer bump* alignment**

  5) Enable PTPC(Pad to Pin check) function to forecast contact position and pre-alert before production.



Summary

- The demand of HPC chip increase significantly.
- The challenges and improvement actions are studied.

HPC Characteristics	Challenges	Improvement Actions
Force	PCB Deformation	Enhance stiffener structure
	Chuck Bending	Enable 3D offset function
Power	Tip burnt	Hybrid probe
	Temperature control	Index move optimization
		Multiple sensor and control zones
Temperature	Probe to MLO Pad alignment	Control the scaling of MLO dimension
		Enlarge MLO Pad size
		Design scaled UD
	Probe to bump alignment	Constrain probing area
		Design scaled LD
		Enable PTPA(Pad to Pin alignment)
		Enable PTPC(Pad to Pin check)